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Linearity Improvement Algorithms of Multi-bit ΔΣ DA Converter –DWA, Self-Calibration and Their Combination

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Abstract. This paper presents several linearity improvement algorithms for multi-bit ΔΣ digital-to-analog converters (DACs), utilizing digital signal processing (DSP) techniques. The ΔΣ DACs are used for electronic measurement and automatic test equipment as well as audio systems, for their easy implementation of high resolution. However, their multi-bit configuration causes overall DAC non-linearity due to characteristics mismatches among multiple unit cells, even though they can be implemented with small hardware and power. Therefore we investigate several algorithms, Data-Weighted Averaging (DWA) algorithm and self-calibration as well as their combination, which improve their DAC linearity as well as their simulation results. We have simulated a ternary (three values: -1, 0, +1) DAC as well as a binary (two values: 0, +1) DAC. From these simulations, we have found that for the low-pass (LP) signal band, DWA (type I) is effective in case of both ternary and binary DACs; for the high-pass (HP) signal band, DWA (type I) is effective in the case of the ternary, whereas DWA (type II) is effective in the case of the binary. The proposed algorithms use DSP techniques and hence they are easy to implement.

1. Introduction

A ΔΣ DA converter consists of mostly digital circuits, and it is frequently used for electronic measurement and test equipment as well as audio systems because it can produce highly linear DC and low frequency signal with high resolution. A multi-bit DAC has three merits. (i) High Signal-to Quantization Noise Ratio (SQNR) with the same oversampling ratio. (ii) Improvement of loop stability for high order modulators. (iii) Following analog filter requirements are relaxed [1, 2].

Notice that a single-bit DAC is inherently linear, whereas the multi-bit configuration causes overall DAC non-linearity due to characteristics mismatches among multiple unit cells, even though the multi-bit ΔΣ DAC can be implemented with small hardware and power [3, 4, 5, 6, 7, 8, 9, 10, 11]. Therefore we have investigated the data weighted averaging (DWA) algorithm and digital self-calibration technique and their combination which improve their DAC linearity. Also we consider the case of ternary digital values (-1, 0, +1) [12], besides binary digital case (0 or +1). We show MATBAB simulation results for low-pass (LP) and high-pass (HP) ΔΣ DA modulators in14-bit resolution case.

2. ΔΣ DA modulator

2.1 ΔΣ DA modulator configuration

A LP ΔΣ DA modulator consists of all digital circuits with feedback configuration using an integrator and a comparator (Fig. 1). The error signal is accumulated at the integrator, and its output is compared by a comparator. The comparator output (0 or 1) is the ΔΣ modulator output. Also the comparator output is fed back to the input. It is known in [1, 2] that the output power spectrum is

noise-shaped; quantization noise is reduced at low frequency while increased at high frequency (Fig. 2).

Similarly, Fig. 3 shows a HP ΔΣ DA modulator. Compared with the LP ΔΣ DA modulator (Fig. 1), plus and minus signs at the feedback summation are reversed. Fig. 4 shows that the output power spectrum is noise-shaped; the quantization noise is reduced in the high frequency regions, while it is increased at the low frequency regions.

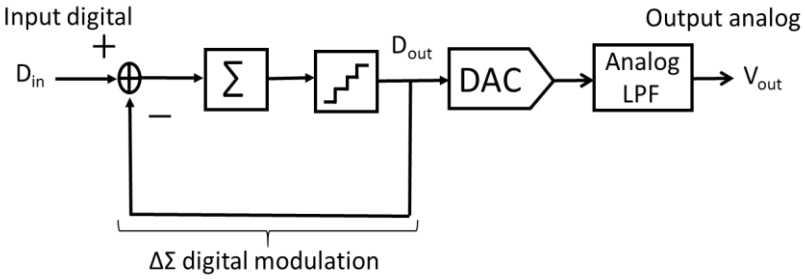


Fig. 1. Block diagram of the first-order LP ΔΣ DA converter.

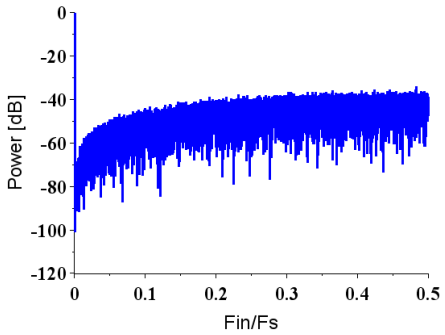


Fig. 2. Power spectrum of the LP ΔΣ modulator output.
(Input sine wave amplitude: 1, normalized frequency: 1)

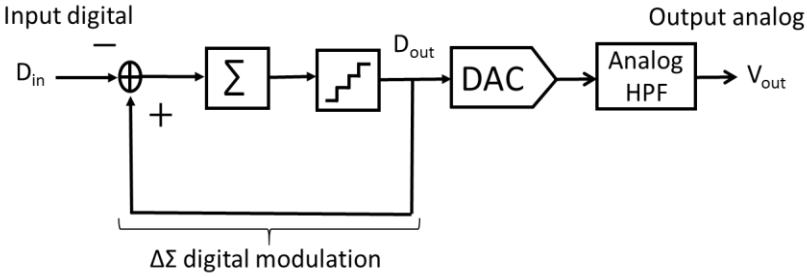


Fig. 3. Block diagram of the first-order HP ΔΣ DA converter.

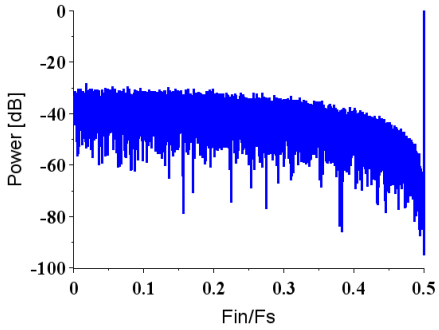
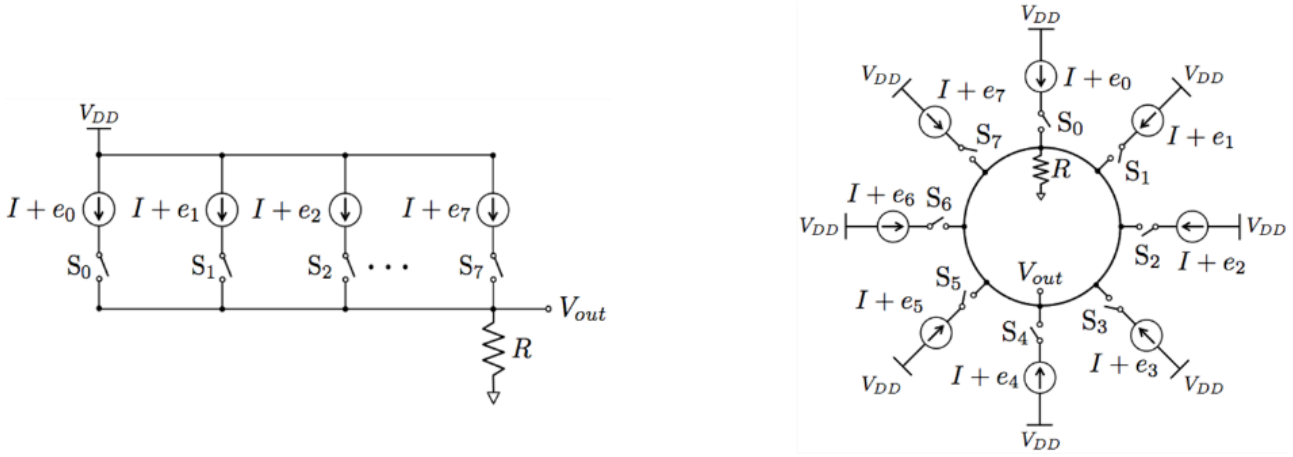


Fig. 4. Power spectrum of the HP ΔΣ modulator output.
(Input sine wave amplitude: 1, normalized frequency: 1)

2.2 Unit current cell mismatches of segmented DAC

We assume that a DAC which follows the modulator has 9-level resolution; its digital input takes the values of 0, 1, 2, ..., 6, or 7 (Fig. 5). Though ideally all currents should be equal, in reality they can be slightly different due to such as process variation inside an IC chip. e_k in Fig. 5 indicates current mismatch of I_k. In case of Fig. 5(a), the mismatch effects cause almost flat power spectrum in the entire band as well as harmonic distortions.



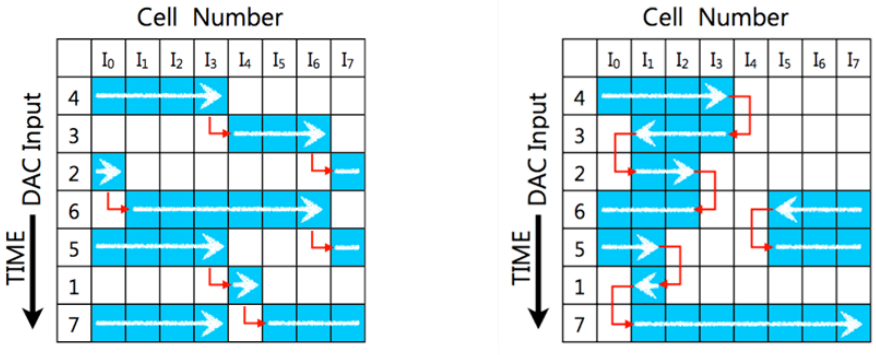
(a) An 8-unit segmented current steering DAC. (b) Its ring configuration.

Fig. 5. Current DAC

2.3 DWA algorithm

Now let us consider to use a DWA DAC (Fig. 5(b)) for linearity improvement [3, 5, 8, 9, 10, 11]. The DWA DAC storing the position with a pointer P(n) controls to rotate current supply, which leads to nonlinearity errors of the multi-bit DAC to be noise-shaped. (Averaged error around DC is zero.) Fig. 6 shows unit-current-cells of ON when input data is 4, 3, 2…. In Fig. 6(a), first, current cells (0, 1, 2, 3) are selected when the digital input data is +4. Next, current cells (4, 5, 6) are selected when the digital input data is +3. In Fig. 6(b), first, current cells (0, 1, 2, 3) are selected when the digital input data is +4. Next, current cells (3, 2, 1) are selected when the digital input data is +3.

In the case of the binary, the methods with DWA (type I) and DWA (type II) are effective for LP and HP ΔΣ modulators respectively [5]. However, we found that the DWA (type I) method is effective for HP ΔΣ modulator in the case of the ternary. Here we have simulated using DWA (type I) for all circuits.



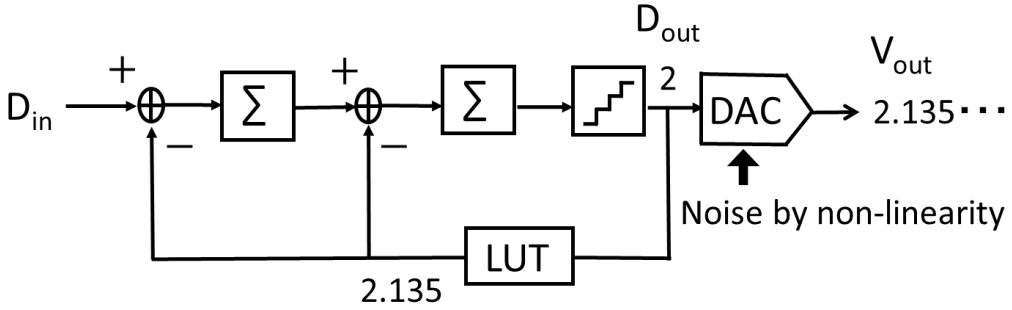
(a) DWA type I (b) DWA type II

Fig. 6. Selection method of current cells with DWA.

2.4 Self-calibration algorithm

In Fig. 7, DAC output is 2.135 due to nonlinearity of the multi-bit DAC when the modulator output is 2. Self-calibration is this '2.135', which is fed-back to the input [5]. We use Look Up Table (LUT) in order to realize the self-calibration. LUT data are created to measure the feedback values with a high linear and high resolution ADC in advance, and LUT output data is selected corresponding to LUT input. It is not necessary to calculate data every time, so a processor is able to reduce calculation load and efficiently execute processing.

For example, suppose that digital output for D_{out} is 2 and the DAC output is 2.135 due to their nonlinearity in Fig. 7. Then the digital values of 2.135 (digital) obtained from LUTs are fed-back to the input.

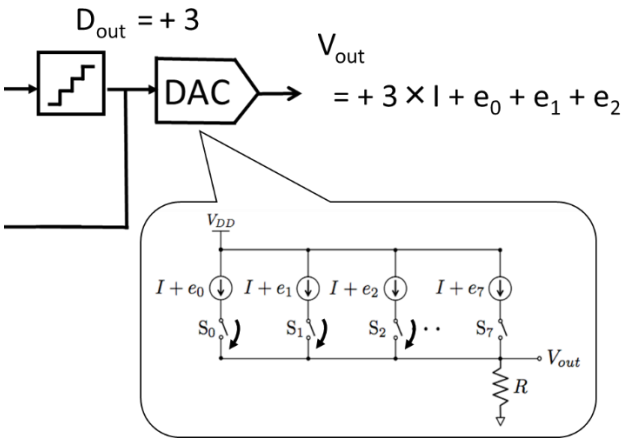


DAC	Input LUT	Output LUT
LUT	2	2.135

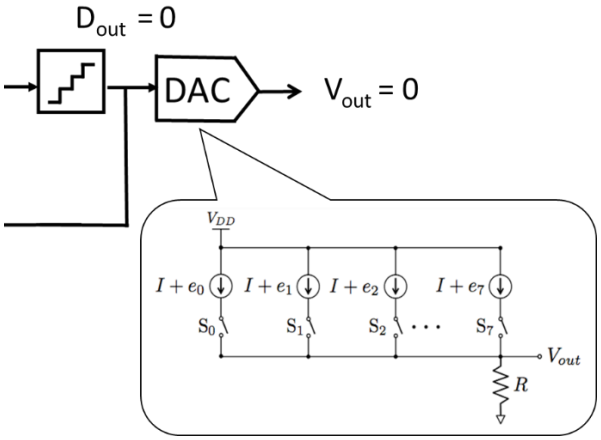
Fig. 7. Circuit with LUT block.

2.5 3 cases of the digital values (-1, 0, +1)

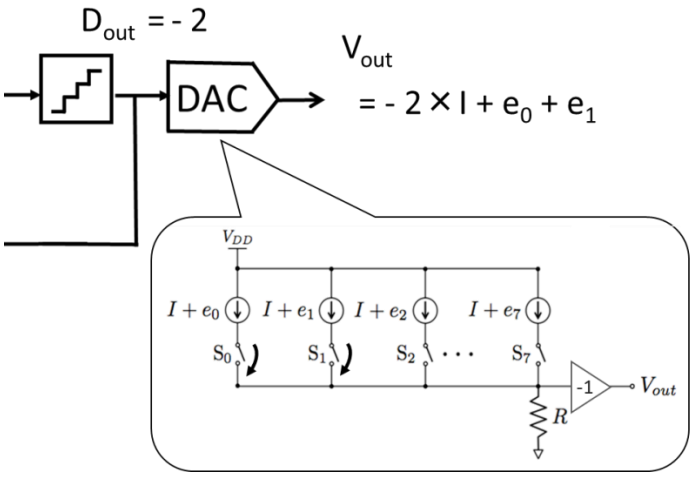
We consider the ternary values case (-1, 0, +1) (Fig. 8) [12]. For example, V_{out} is a positive voltage when D_{out} is +3 (Fig. 8(a)). In contrast, V_{out} is a negative voltage when D_{out} is -2 (Fig. 8(c)). Of course, V_{out} is 0 when D_{out} is 0 (Fig. 8(b)). On the other hand, in the conventional binary digital, they are 0 or +1.



(a) In the case that D_{out} is positive.



(b) In the case that D_{out} is zero.



(c) In the case that D_{out} is negative.

Fig. 8. Digital values cases; -1, 0, +1.

3. Simulation results

3.1 Configuration of simulation circuit

The previous sections have investigated the techniques using DWA (type I) and self-calibration algorithm. We compare 4 circuits (the conventional circuit, DWA, self-calibration and its combination), and verify the linearity improvement. Figure 9, 10 show ④ circuits. They are different from DWA (type I), self-calibration and its combination.

① 2nd-order (LP or HP) ΔΣ DA modulator + nonlinearity DAC
② 2nd-order (LP or HP) ΔΣ DA modulator + nonlinearity DAC + DWA (type I)
③ 2nd-order (LP or HP) ΔΣ DA modulator + nonlinearity DAC + self-calibration
④ 2nd-order (LP or HP) ΔΣ DA modulator + nonlinearity DAC + DWA (type I) + self-calibration

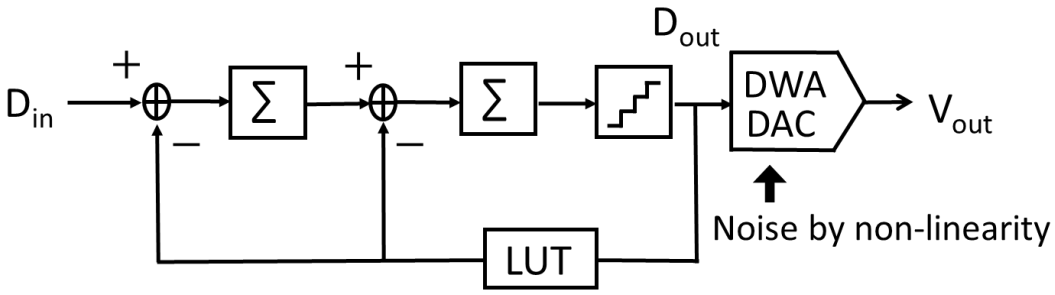


Fig. 9. Proposed LP model circuit with DWA (type I) and self-calibration.

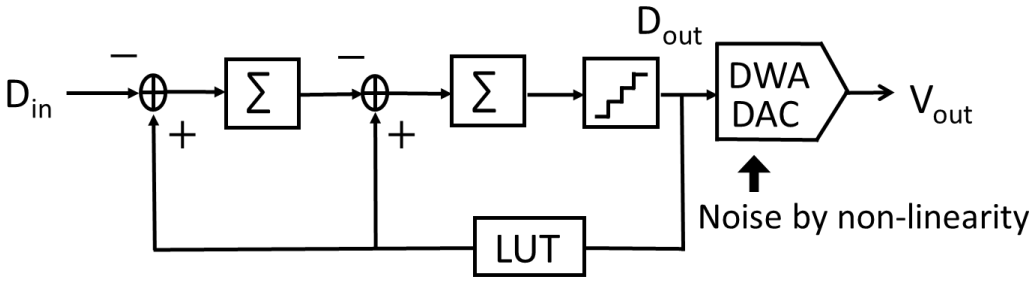


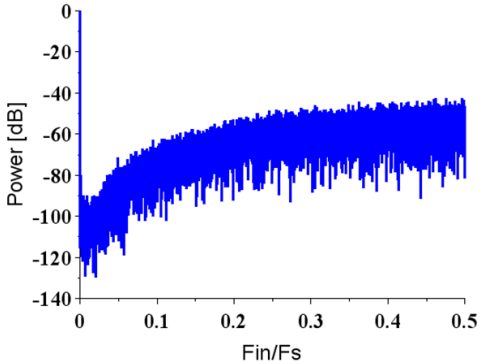
Fig. 10. Proposed HP model circuit with DWA (type I) and self-calibration.

3.2 SNDR evaluation

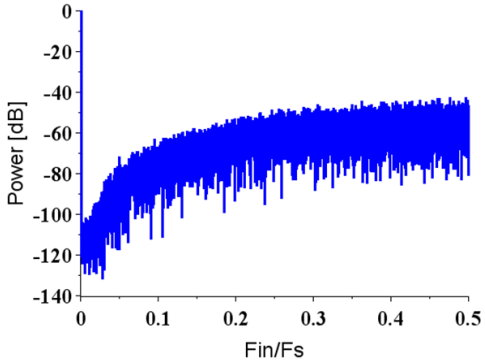
Signal to Noise and Distortion Ratio (SNDR) is one of the DAC performance indices; it is the ratio of the signal component power to the generated noise power. The DAC performance becomes better as its SNDR is improved.

3.3 SNDR improvement (LP model)

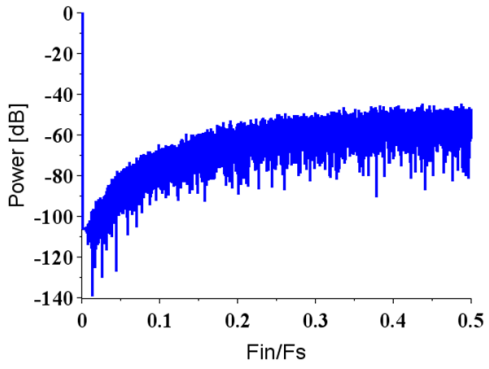
We have verified the effectiveness of the proposed technique using DWA (type I) and self-calibration (Fig. 9). We use a sinusoidal signal input (D_{in}) whose period is 14K-point and its amplitude is 7.5 and center values are zero. Unit-current-cells have some errors. Fig. 11 shows power spectrums for circuits ① to ④. Fig. 11④ indicates that noise of the low frequency band is reduced. On the other hand, in Fig. 11①, ②, ③, the noise power is larger than that of Fig.11④ in the low frequency region. Fig. 12 shows SNDR comparison; mismatch standard deviation: σ is varied. SNDRs are averaged values among 5 sets of the unit-current-cells. We see that the SNDR values of the proposed circuit ④ is higher than other circuit ① to ③. SNDR values of the circuits ② to ④ in Fig. 12(d) are similar because the mismatch is relatively small; its state is close to ideal.



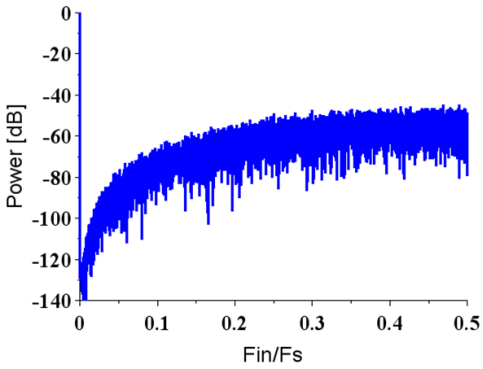
① w/o DWA & self-calibration



② w/ DWA, w/o self-calibration

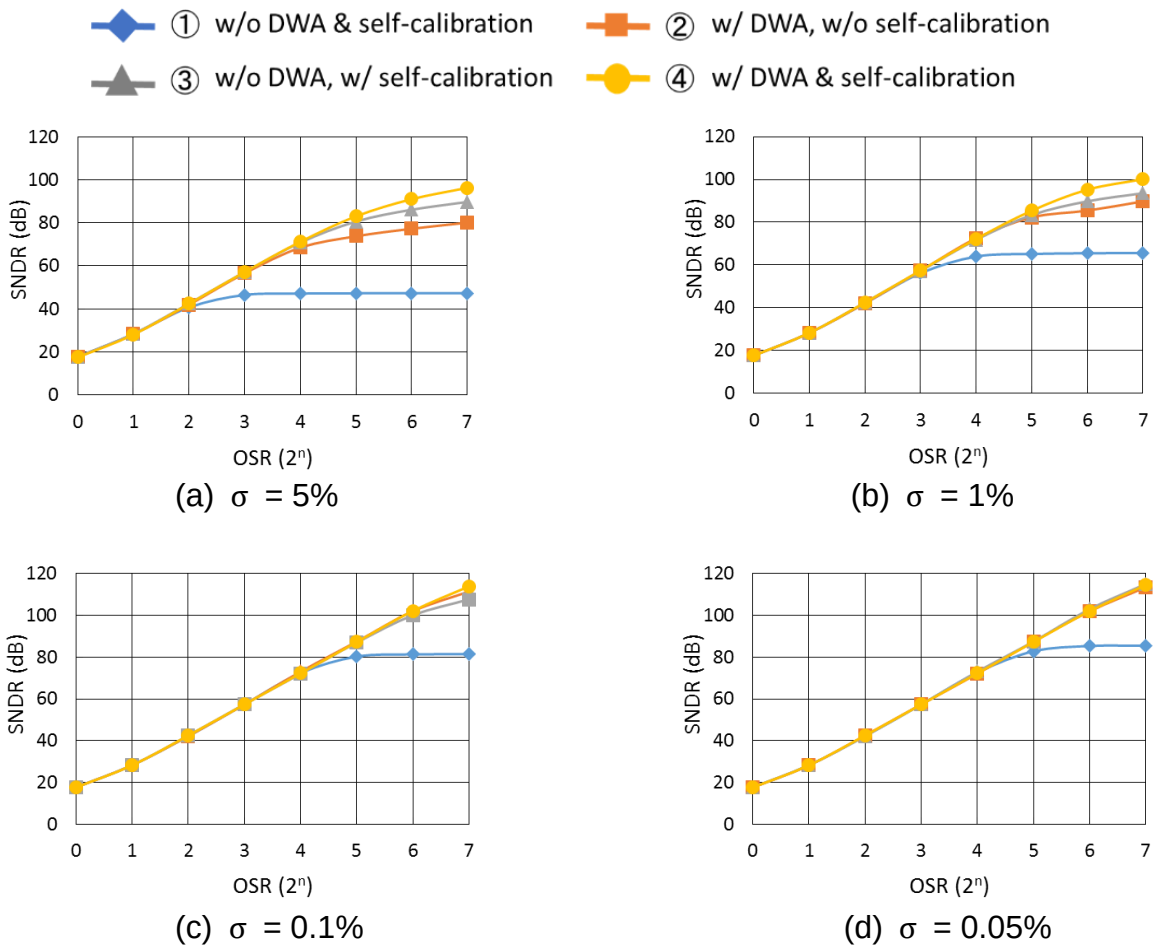


③ w/o DWA, w/ self-calibration



④ w/ DWA & self-calibration

Fig. 11. Power spectrum of LP model circuits in case that the standard deviation is 1.0%.



(a) σ = 5%　　(b) σ = 1%

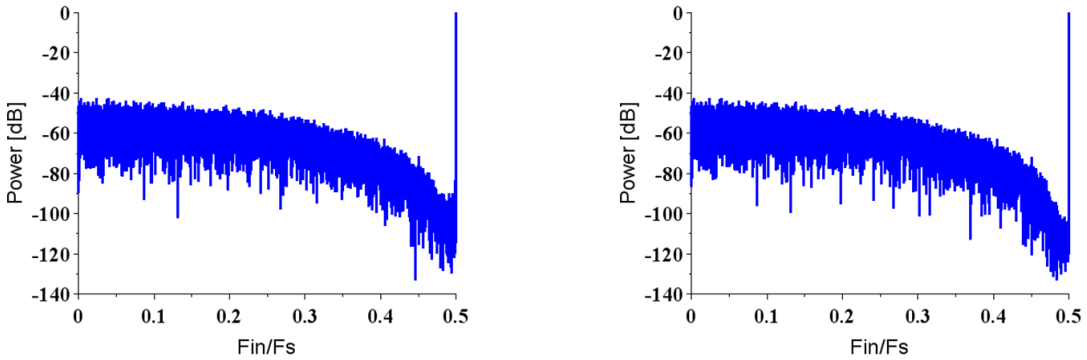
(c) σ = 0.1%　　(d) σ = 0.05%

Fig. 12. SNDR comparison in LP model.

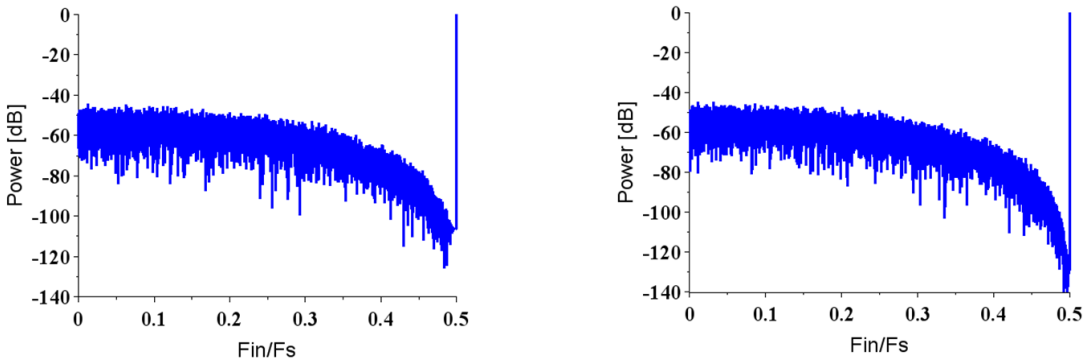
3.4 SNDR improvement (HP model)

In a similar manner, we confirm the effectiveness of the proposed HP model circuit using DWA (type I) and self-calibration (Fig. 10). Fig. 13④ indicates noise of the high frequency band is reduced. On the other hand, in Fig. 13①, ②, ③, noise power is larger than that of Fig.13④ in the high frequency. Fig. 14 shows SNDR comparison and the SNDR values of the proposed circuit ④ is higher than other circuits ① to ③. In like 3.2 chapter, SNDR values of the circuits ② to ④ in Fig. 14(d) are similar because their states are close to ideal.

In the case of the binary, the method using DWA (type II) is effective for HP model circuit [5]. However, in the case of the ternary, we have found and verified the effectiveness of the using DWA (type I) for HP modulator circuit. For going forwards and back with DWA (type II), the errors of the plus and minus are accumulated in the case of the ternary. Consequently, quantization noise is not reduced at high frequency. On the other hand, there are not errors of the minus in the case of the binary, so DWA (type II) is effective for HP model circuit.

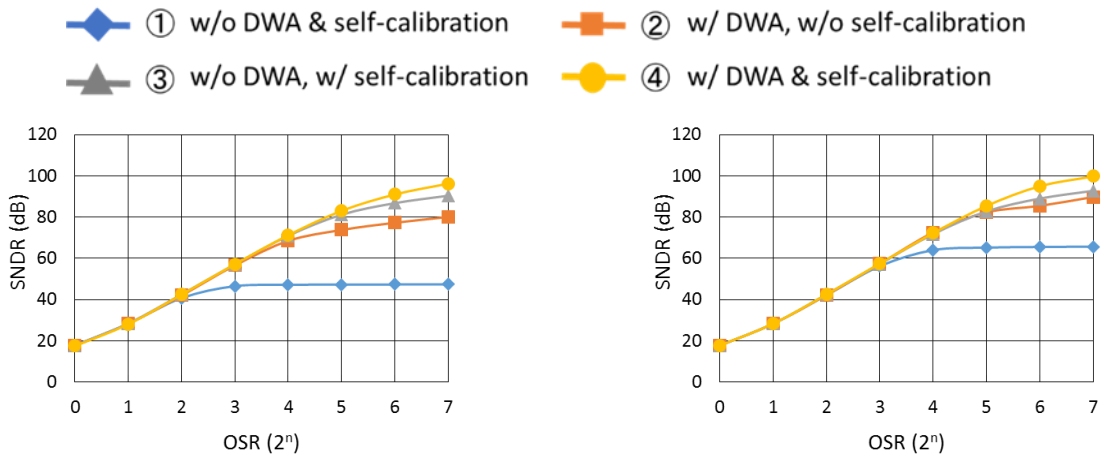


① w/o DWA & self-calibration ② w/ DWA, w/o self-calibration

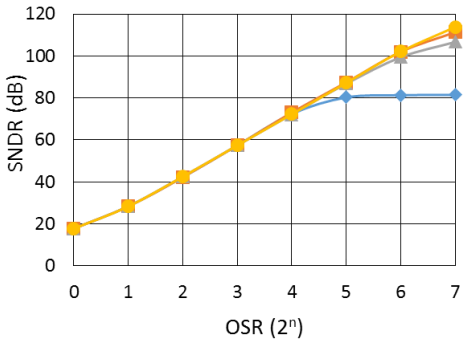


③ w/o DWA, w/ self-calibration ④ w/ DWA & self-calibration

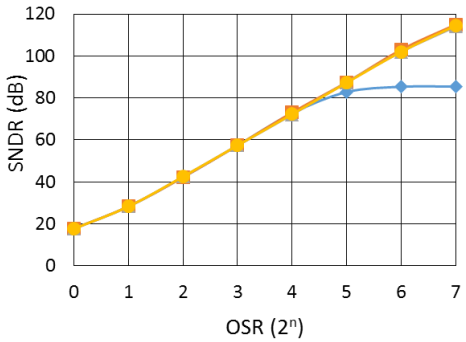
Fig. 13. Power spectrum of HP model circuits in case that the standard deviation is 1.0%.



(a) σ = 5% (b) σ = 1%



(c) σ = 0.1%



(d) σ = 0.05%

Fig. 14. SNDR comparison in HP model.

4. Conclusion

We have investigated digital techniques for linearity improvement in multi-bit ΔΣ DA converters for three values digital; values are -1, 0, +1. We have derived DWA and self-calibration algorithms, as well as their combination, and validated their effectiveness with MATLAB simulation. The proposed circuits using DWA and self-calibration can achieve higher SNDR values than the conventional. When the mismatches of the DWA are relatively large, the proposed method is effective. In addition, we have found and verified that DWA (type I) is effective for HP model in the case of the ternary (three values; -1, 0, +1) although DWA (type II) is effective for HP model in the case of the binary (two values; 0, +1). The proposed systems consist of mostly digital and they can be easily implemented.

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