Time-to-Digital Converter Architecture Using Asynchronous Two Sine Waves with Different Frequencies

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Abstract This paper proposes a time-to-digital converter (TDC) architecture using two asynchronous sine waves with different frequencies; each starts oscillation at different cycle at the rising timing of the corresponding input timing signal. We show here that by counting their oscillation start phase difference using digital counters, a highly linear stable time digitizer circuit can be realized. We present its configuration/operation and simulation verification.

1. Introduction

A time-to-digital converter (TDC) measures the timing difference between two clock signals and provides its output as a digital value. In many cases, it uses analog delay lines. However, their characteristics vary due to power supply voltage, temperature and process variations, and its overall linearity may degrade [1-8]. Then their compensation circuits are often required. This paper introduces a TDC architecture which employs two trigger circuits [9, 10] using two asynchronous sine waves with different frequencies, but without analog delay lines, and it can obtain high linearity with simple circuit.
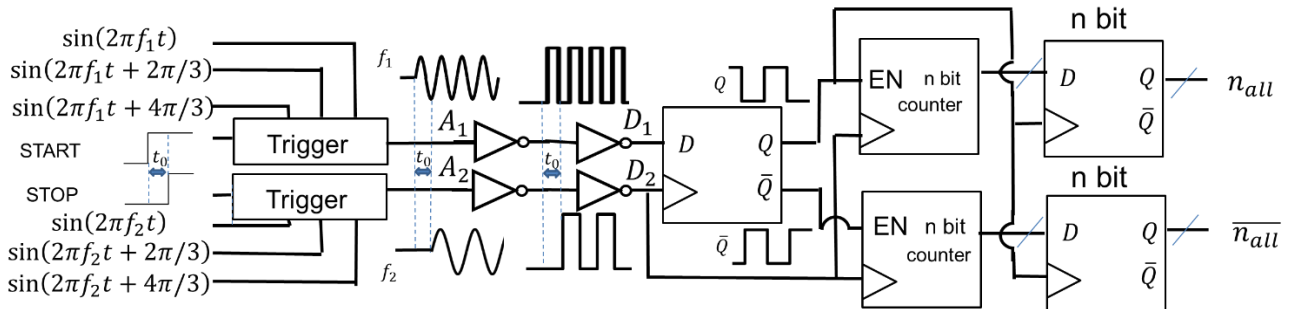
2. Proposed TDC Architecture

Fig. 1. Proposed TDC Architecture

Fig. 1 shows our proposed TDC which consists of two trigger circuits, inverters, DFFs and two binary up-counters. The two step signals 'START' and 'STOP' have different start phases, and their start phase difference (or their oscillation start timing difference) is represented by $t_0 (> (1/2f_1))$. First, the oscilloscope trigger circuits [9,10] convert sine waves of three-phase alternating current to A_1 and A_2 (Fig. 2). A_1 and A_2 are expressed as follows:

$$A_1 = \frac{3\sqrt{3}}{2}\sin(2\pi f_1 t) \tag{1}$$

$$A_2 = \begin{cases} 0 & (0 \le t \le t_0) \\ \dfrac{3\sqrt{3}}{2}\sin\{2\pi f_2(t - t_0)\} & (t_0 < t) \end{cases} \tag{2}$$

Fig. 2 shows a three-stage trigger circuit [10], where the input is a step signal and also sine waves of three-phase alternating voltages are provided. The output signal starts to oscillate at the rising timing of the step input with the same frequency as the three-phase alternating voltages. Its operation in each mode is as follows:

Track mode:

$$V_{out} = \sin(2\pi ft + 4\pi/3)\{\sin(2\pi ft) - \sin(2\pi ft + 2\pi/3)\}$$
$$+ \sin(2\pi ft)\{\sin(2\pi ft + 2\pi/3) - \sin(2\pi ft + 4\pi/3)\}$$
$$+ \sin(2\pi ft + 2\pi/3)\{\sin(2\pi ft + 4\pi/3) - \sin(2\pi ft)\} = 0$$

Hold mode:

$$V_{out} = \sin(2\pi ft + 4\pi/3)\{\sin(2\pi ft_0) - \sin(2\pi ft_0 + 2\pi/3)\}$$
$$+ \sin(2\pi ft)\{\sin(2\pi ft_0 + 2\pi/3) - \sin(2\pi ft_0 + 4\pi/3)\}$$
$$+ \sin(2\pi ft + 2\pi/3)\{\sin(2\pi ft_0 + 4\pi/3) - \sin(2\pi ft_0)\} = \frac{3\sqrt{3}}{2}\sin\left(2\pi f(t - t_0)\right)$$
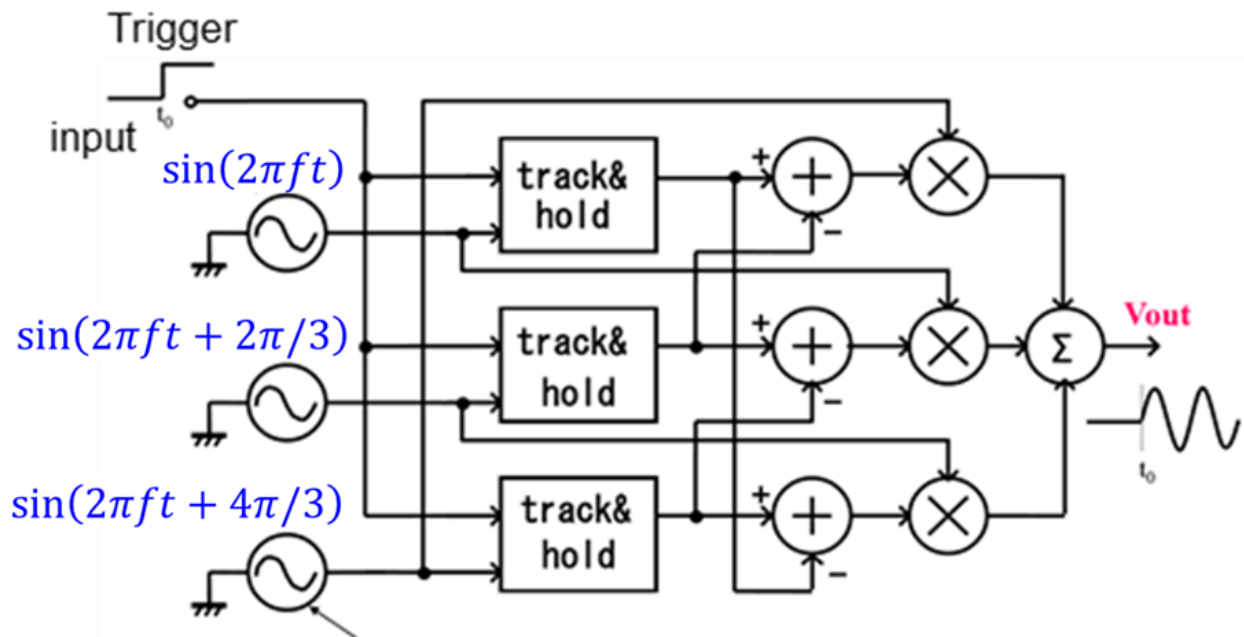

Fig. 2. Three-stage configuration trigger circuit

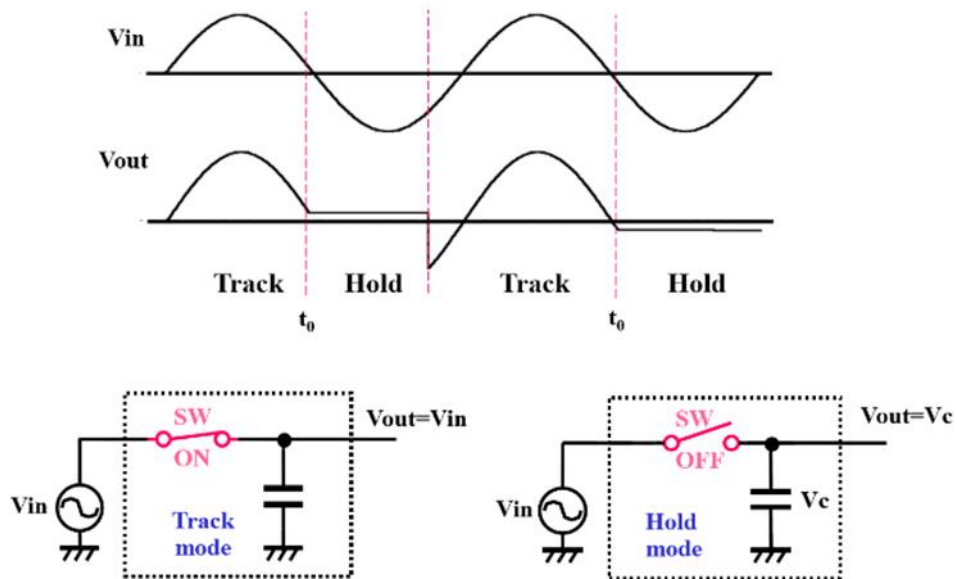Fig. 3 shows a sample & hold circuit used in the trigger circuit.

Fig. 3. Track and hold circuit

Fig. 4 and 5 show the CMOS circuit and simulation results of the trigger circuit. When the trigger input is low, the output is in track mode, and when the trigger input is high, the output is in hold mode.
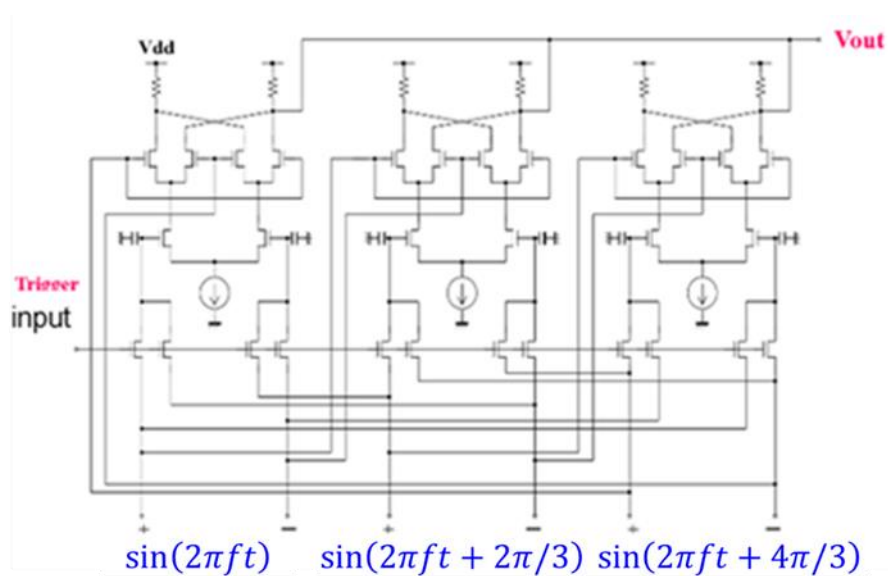

$$\sin(2\pi ft) \quad \sin(2\pi ft + 2\pi/3) \quad \sin(2\pi ft + 4\pi/3)$$

Fig. 4. CMOS configuration of three stage trigger circuit
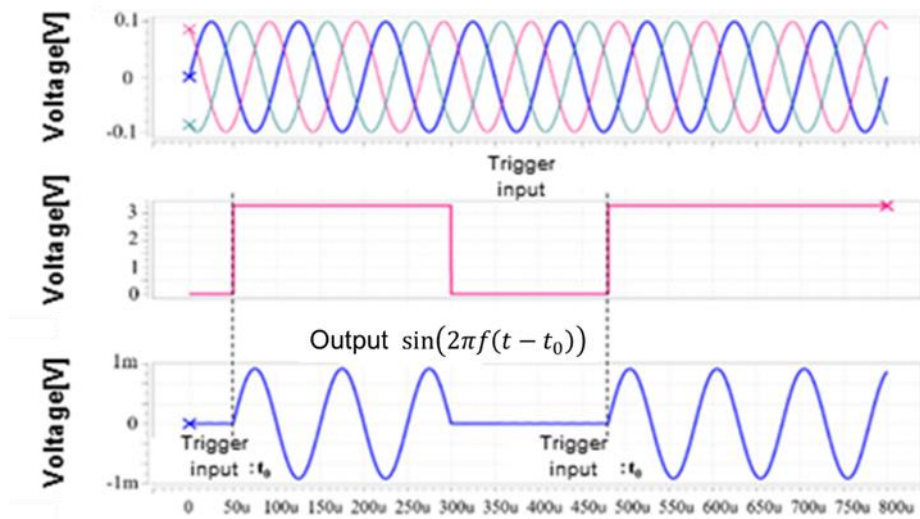
Fig. 5. simulation results

The inverters convert A_1 and A_2 to D_1 and D_2 respectively, and they are shown as follows:

$$D_1 = \begin{cases} 1 & (A_1 > 0) \\ 0 & (A_1 \leq 0) \end{cases} \tag{3}$$

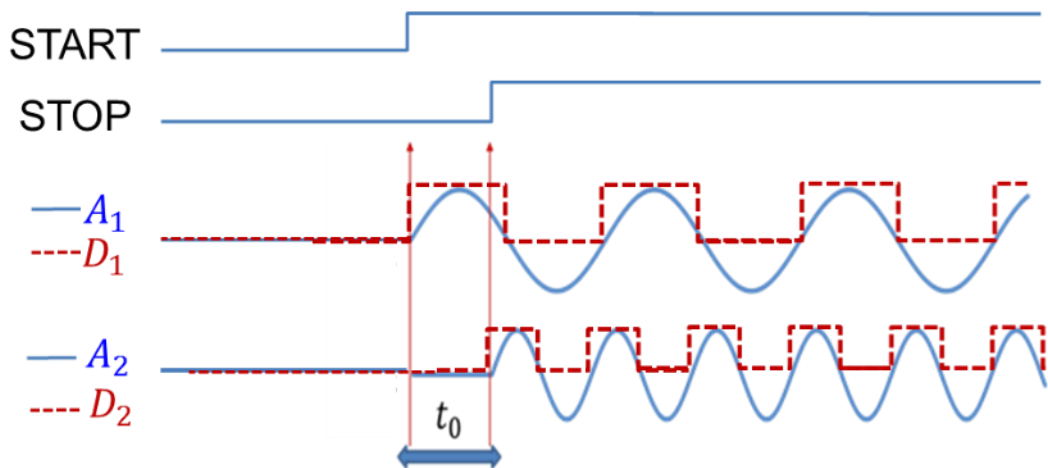$$D_2 = \begin{cases} 1 & (A_2 > 0) \\ 0 & (A_2 \leq 0) \end{cases} \tag{4}$$

Fig. 6. A_1, A_2, D_1 and D_2 start to oscillate with different frequencies at the rising timing edges of START and STOP signals respectively.

D_1 is fed to D in a DFF, whereas D_2 is provided as a clock. f_1 and f_2 are defined as the frequencies of A_1 and A_2 respectively ($f_1 \neq f_2$). Fig. 7 shows the DFF latches the value of D_1 at the clock rising timing. $n_{all}(= n_1 + n_2 \ldots)$ represents the number of 1's , and $\overline{n_{all}}$ ($= \overline{n_1} + \overline{n_2} \ldots$) represents the number of 0's.
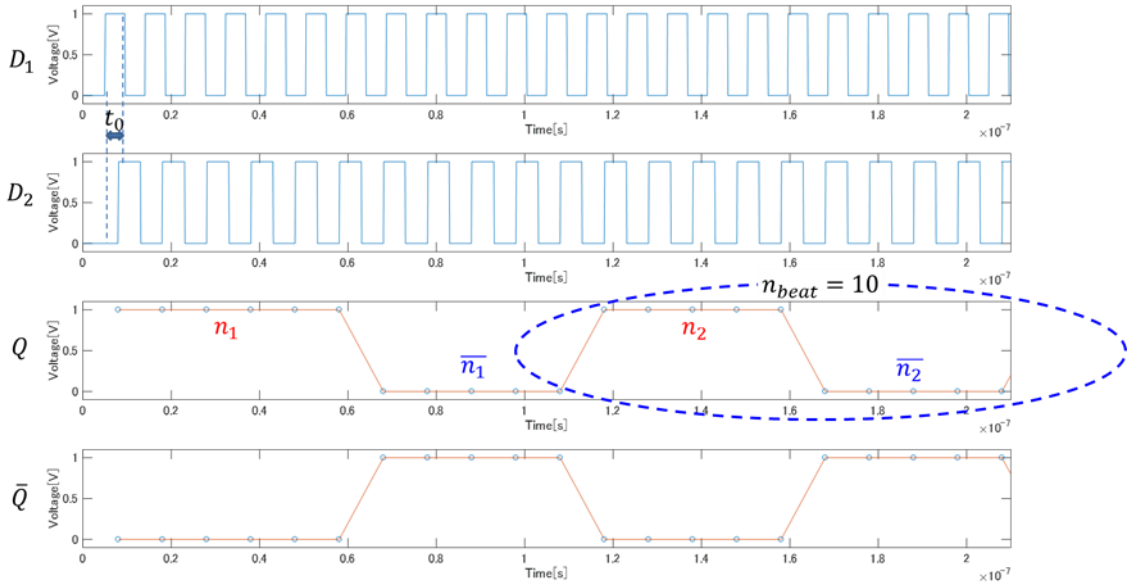
Fig. 7. Beat wave which D_1 sample by clock D_2.

In the proposed circuit, we can finally obtain n_{all} and $\overline{n_{all}}$. Q is a beat wave, which consists of D_1 sampled by clock D_2. These are waves with the frequency of $|f_2 - f_1|$. n_{beat} is the number of points included by Q's one period. The more n_{beat} is present, the higher linearity is obtained. n_{beat} is defined as follows:

$$n_{beat} = \frac{f_2}{|f_2 - f_1|} \tag{5}$$

A binary up-counter increments its output value every clock when the enable signal is 1, whereas its output value holds its current value when the enable signal is 0. Finally, we use n-bit registers with clock Q. By using Q as a clock, a fixed value can be obtained at any time when the operation is ended.

Fig. 8 and Fig. 9 show the configuration and simulation results of the binary counter. When the input is Q of the flip-flop in Fig.1, the number of n_{all} is counted, whereas in the case of $\bar{Q}$, the number of $\overline{n_{all}}$ is counted. The number of points to be measured determine the number of required full adders and DFFs.

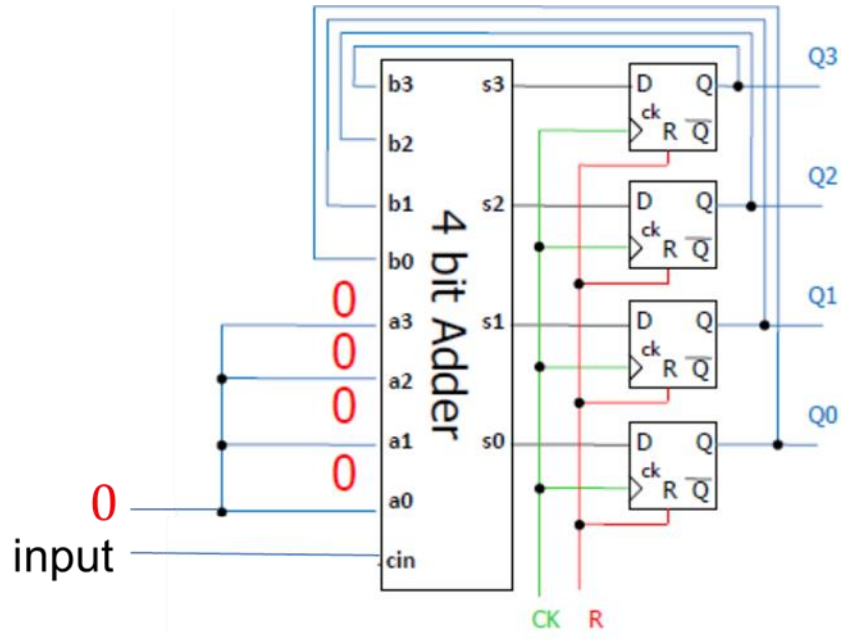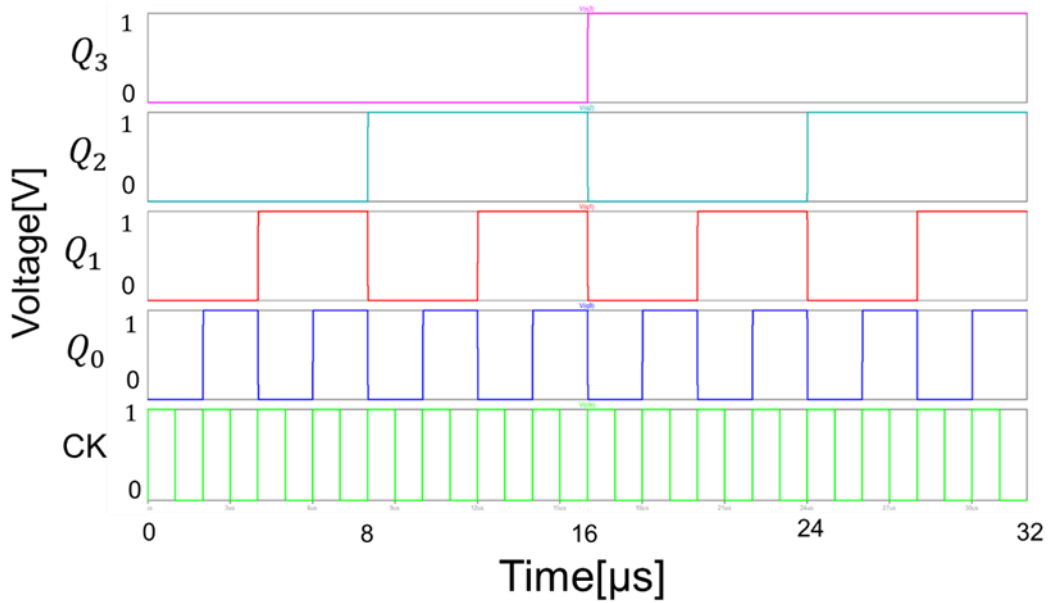Fig. 8 Binary up counter

Fig.9 Binary up counter simulation results (LT spice)

3. Measurement logic

D_1 and D_2 have different periods from one rising timing to another rising timing. It can be expressed as t' as follows (Fig. 10) :

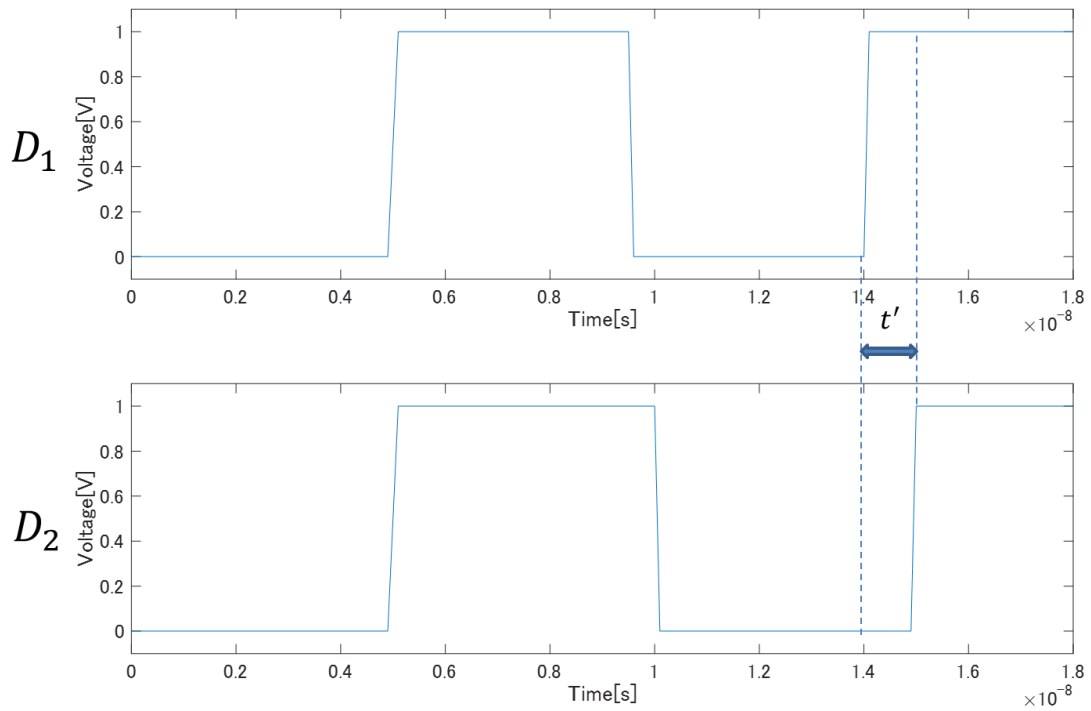$$t' = \left| \frac{1}{f_2} - \frac{1}{f_1} \right| \tag{6}$$

Fig. 10. period difference between D_1 and D_2

Fig. 11 and Fig. 12 show some examples of the deviation points when t_0 are 0[s] and 3[ns]. When this deviation is expressed by n_{all}, $\overline{n_{all}}$ and n_{beat}, deviation and t' give t_0 as follows :

$$t_0 = \begin{cases} (\overline{n_{all}} - n_{all})t' & \text{(in case } f_1 > f_2) \\ \{n_{beat}/2 - (\overline{n_{all}} - n_{all})\}t' & \text{(in case } f_1 < f_2) \end{cases} \tag{7}$$
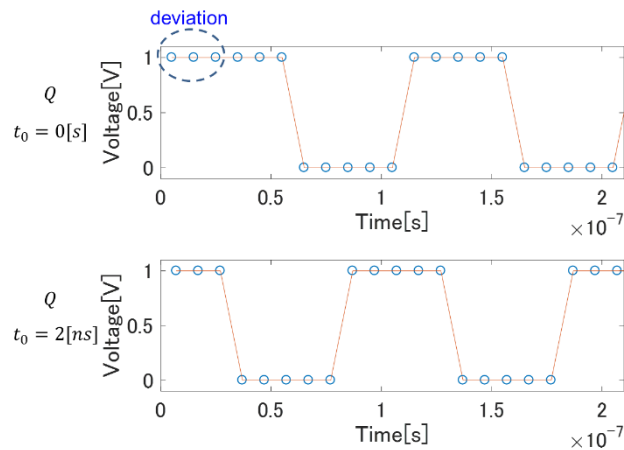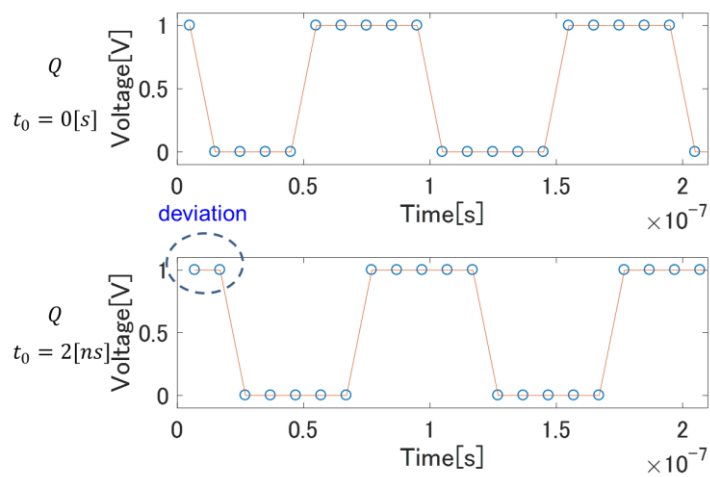

Fig. 11. One example of deviation of points $f_1 > f_2$

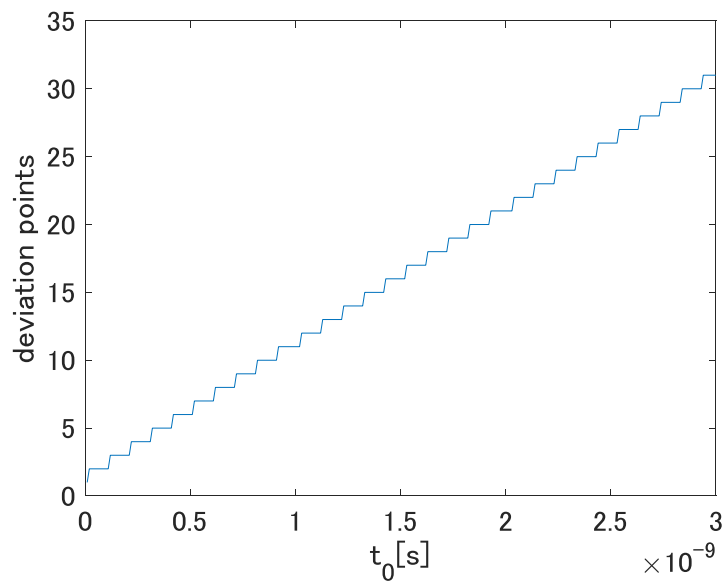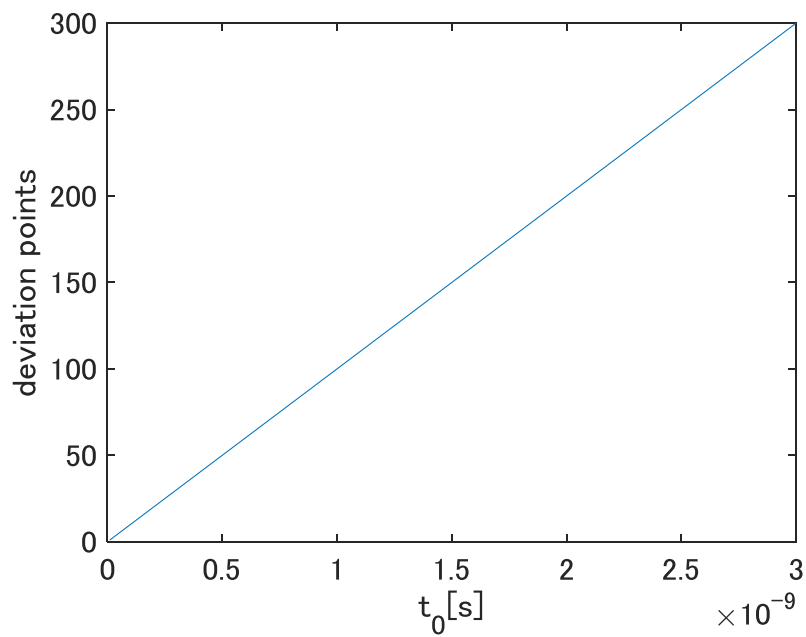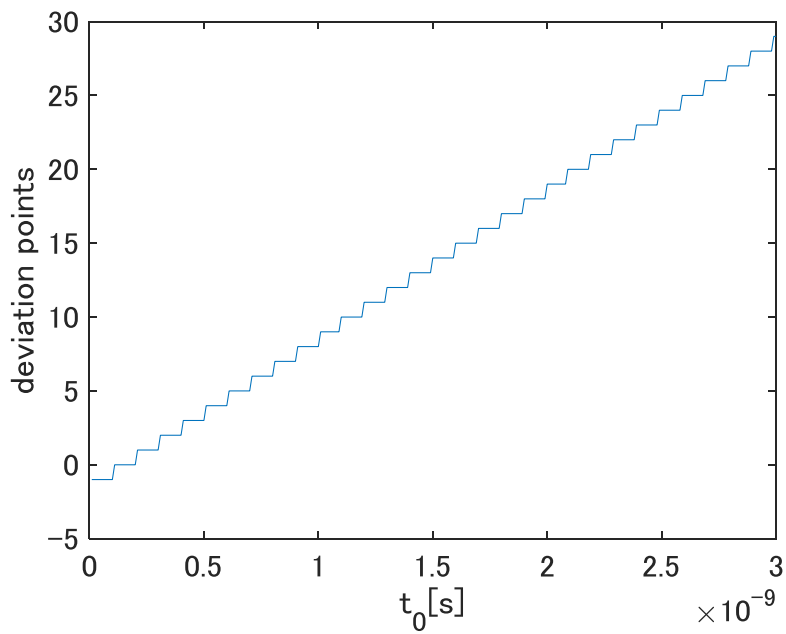Fig. 12. Another example of deviation of points $f_1 < f_2$

Fig. 13 shows the TDC linearity for given frequencies. f_2 is a clock frequency. f_2 and f_1 become closer, t' becomes smaller, so that the time resolution becomes finer and the TDC linearity can be maintained.
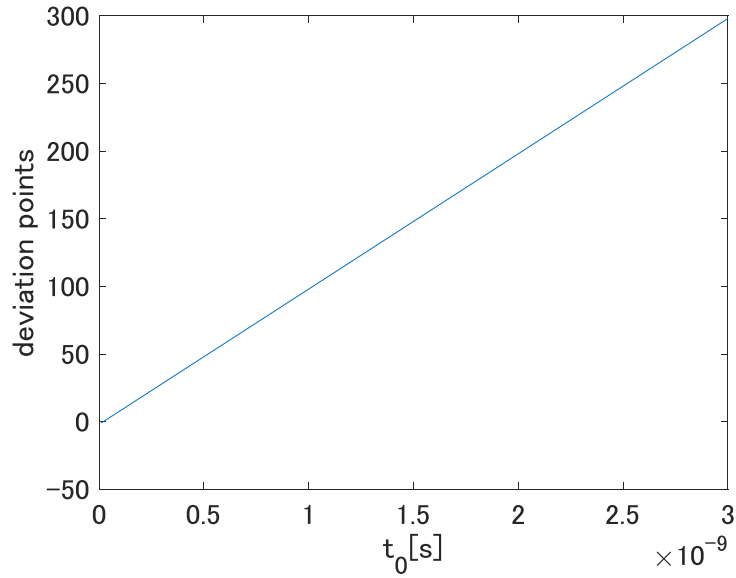

$(a) f_1 = 99[MHz],\ f_2 = 100[MHz]$

(b)$f_1 = 99.9[MHz], f_2 = 100[MHz]$

(c)$f_1 = 101[MHz], f_2 = 100[MHz]$

(d)$f_1 = 100.1[MHz], f_2 = 100[MHz]$
Fig.13. Linearity of TDC with given frequencies

Fig. 14 shows the RMS (Root Mean Squared) error of t_0 with respect to the number of $n_{beat}/2$. RSM error shows as follow:

$$\text{RMS error of } t_0 = \sqrt{\frac{1}{n_{beat}/2} \sum_{i=1}^{n_{beat}/2} (t_i)^2} \tag{8}$$

t_i shows deviation between set t_0 and calculated t_0. Fig. 15 is a logarithmic representation of Fig. 14. As the number of $n_{beat}/2$ increases, the error of t_0 becomes smaller. We see that the proposed TDC linearity can be improved as the number of $n_{beat}/2$ increases. The simulation conditions are as follows;

(a) $f_1 = f_2 \frac{2N+1}{2N} [Hz], f_2 = 100[MHz], t_0 = 1[ns]$
(b) $f_1 = f_2 \frac{2N-1}{2N} [Hz], f_2 = 100[MHz], t_0 = 1[ns]$
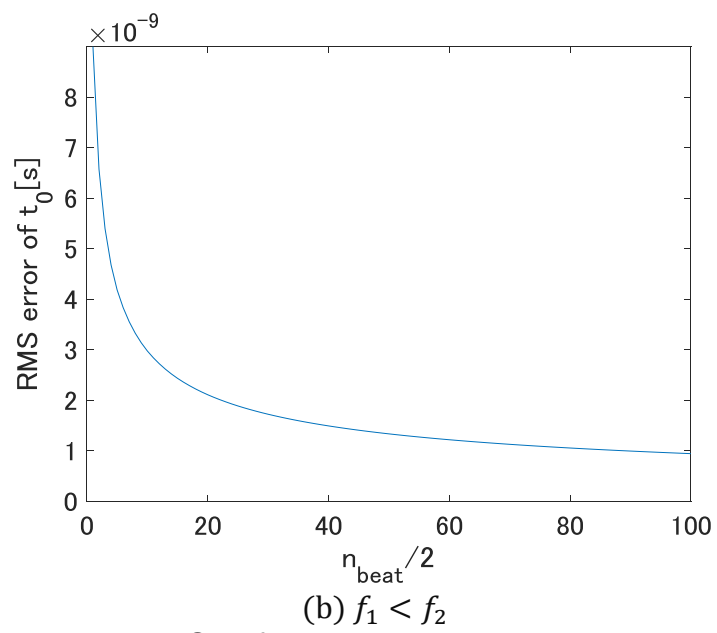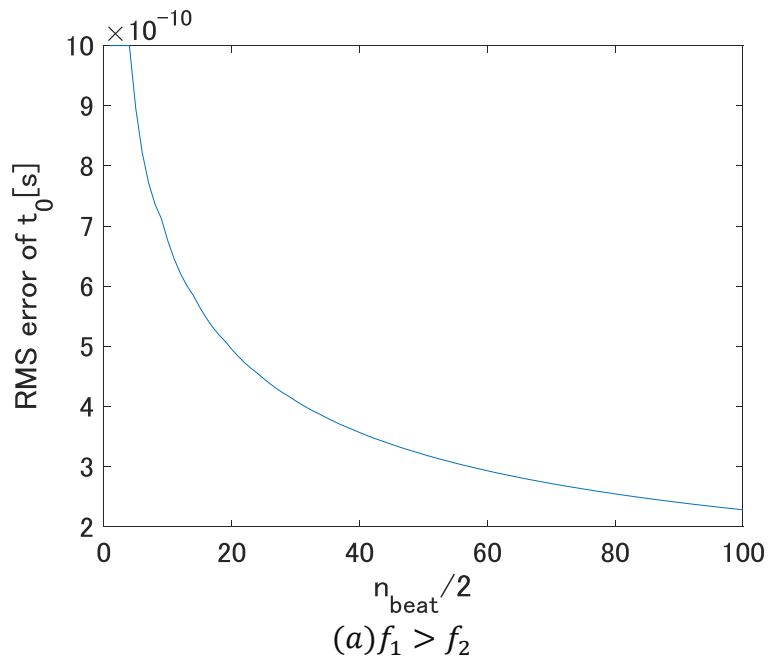
$(a) f_1 > f_2$

(b) $f_1 < f_2$

Fig. 14. RMSE of t_0 with respect to the number of $n_{beat}/2$
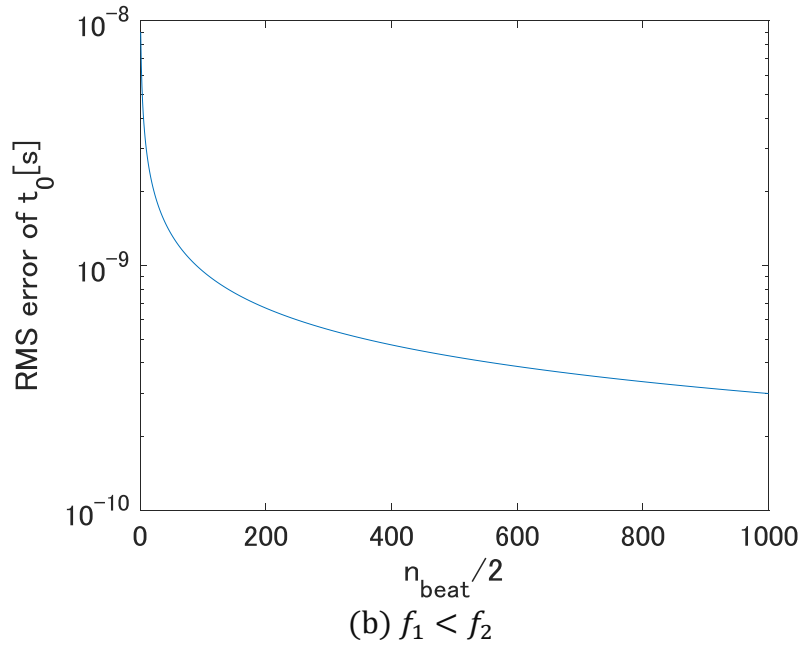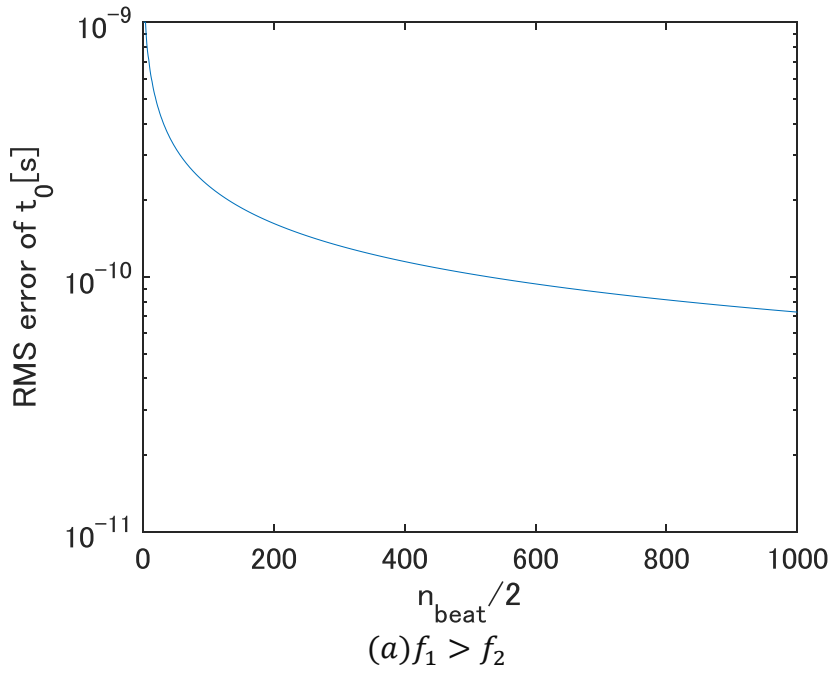
$(a) f_1 > f_2$

(b) $f_1 < f_2$
Fig. 15. Logarithmic graph of Fig. 8

4. SPICE Simulation verification of proposed TDC

We have performed simulations of the proposed TDC by means of LT spice. We used ideal voltage sources instead of trigger circuits. The settings used for the simulation are as follows.

$$f_1 = 99[MHz], f_2 = 100[MHz], t_0 = 1[ns]$$

Fig. 16 shows n_{all} and $\overline{n_{all}}$ measured by the proposed circuit. Q_n represents each values. n = 0 is LSB, and n = 7 is MSB. From Fig. 16, it can be seen that the binary up counters operate normally.
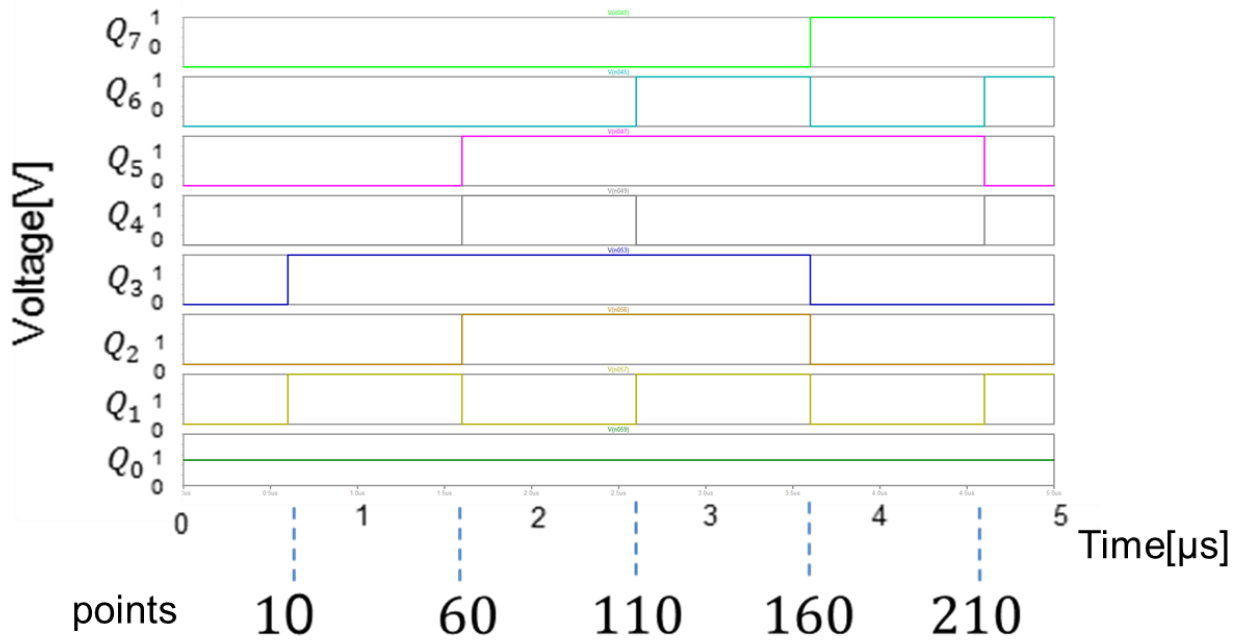
(a) n_{all}
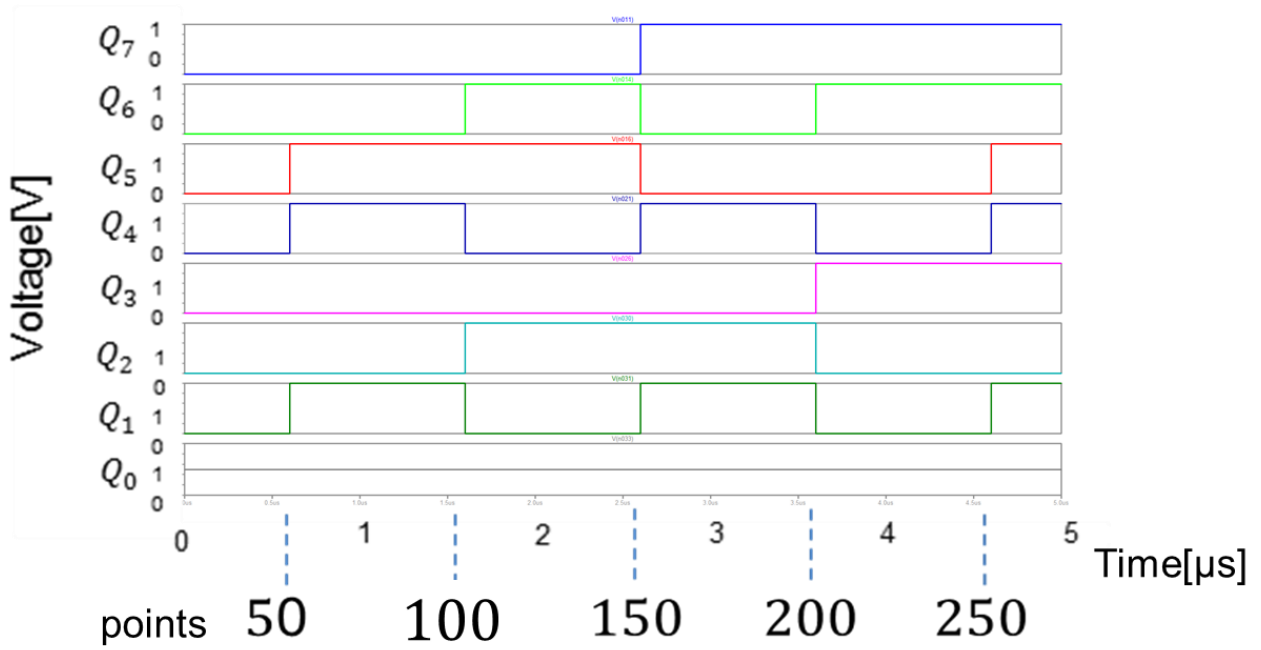
(b) $\overline{n_{all}}$

Fig. 16. Simulated output of (a)n_{all} and (b)$\overline{n_{all}}$

Calculating $\overline{n_{all}} - n_{all}$, we need n_{all} and $\overline{n_{all}}$. For example, if $\overline{n_{all}}$ is 250 and n_{all} is 210, then $\overline{n_{all}} - n_{all}$ is 40. This result is the same in other cases. We see from these results that the target points can be obtained regardless of the sampling time of n_{all} and $\overline{n_{all}}$ values by simulation using the beat wave as the clock. From Eq. 7, since $t_0 = 1.01[ns]$, error is 1[%].

5. Conclusion

This paper describes a TDC architecture with fine time resolution and high linearity; it employs trigger circuits. Some simulation results validate our proposed TDC architecture. We could obtain the start phase difference of the sine wave with different frequencies from the simulation results using the proposed circuit. In this circuit, we do not have to use analog delay array like conventional TDC architecture, so that the proposed TDC linearity can be easily secured. Future tasks are to perform simulations of the entire proposed TDC including the trigger circuits.

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