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Invited Paper

A Low Switching Loss 40 V Dual RESURF LDMOS Transistor with Low Specific On-Resistance

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Abstract. This paper describes a 0.18 μm CMOS compatible low switching loss 40 V dual RESURF LDMOS transistor with low specific on-resistance for automotive applications. The proposed device improved from a conventional dual RESURF LDMOS transistor is designed to reduce the Miller capacitance with a grounded field plate and to decrease the specific on-resistance. Simulations verified that the proposed device has a low figure of merit (gate charge × on-resistance) FOM = 48.2 mΩ·nC which is about one third that of the conventional device, and a state-of-the-art level characteristic of specific on-resistance $R_{on}A$ = 40.9 mΩ·mm^2 at breakdown voltage BV_{DS} = 62 V. The proposed device also has no drain current expansion for a drain voltage range $V_{DS} \leqq$ 40 V at the maximum gate voltage rating V_{GS} = 4 V, leading to a wide SOA. Furthermore the proposed device would likely be able to have high hot carrier endurance due to the enhanced RESURF effect around the gate-side drift region edge.

1. Introduction

Lateral double-diffused MOS (LDMOS) transistors are widely used as switching devices of power converters for not only consumer but also automotive applications. Automotive applications require a much wider safe operating area (SOA) and higher reliability for hot carriers than consumer applications. However the conventional LDMOS transistor generally has a narrow SOA due to drain current expansion (CE) caused at high drain and gate bias voltages [1,2], and low hot carrier endurance due to high impact ionization generated near the gate-side drift region edge. In order to overcome these problems, a 30-50V LDMOS transistor having a dual reduced surface field (RESURF) drift structure was proposed [3,4,5]. The transistor has a wide SOA and high hot carrier endurance, but it has a large switching loss. Therefore the reduction of the switching loss for the conventional device is required.

In this paper, we improved the 30-50V LDMOS transistor to reduce the switching loss with a grounded field plate, and verified the characteristics by using a device simulator, DESSERT (Sample version) developed by AdvanceSoft Corporation [6]. In the following sections, the conventional and the proposed LDMOS transistor structures are introduced. Simulation results indicate the superiority of the proposed device in terms of the switching loss, the characteristic of specific on-resistance vs. breakdown voltage, SOA, and the reliability for hot carriers.

2. Device structures

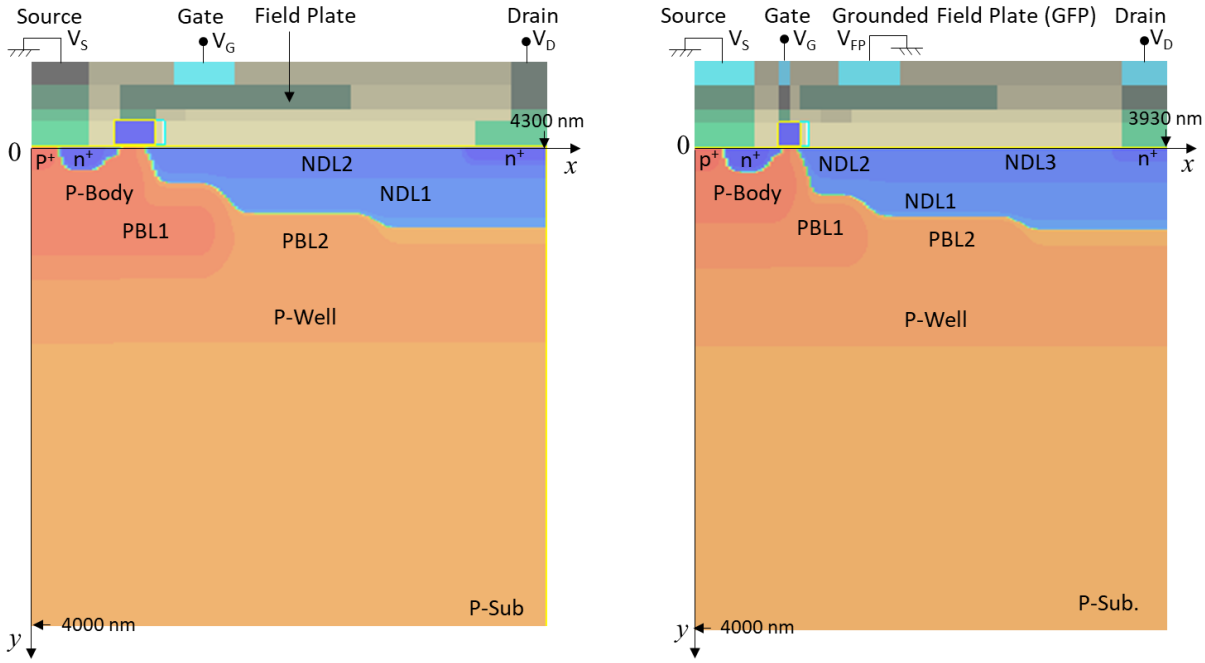
2.1 Conventional LDMOS transistor

Fig. 1(a) shows a cross-sectional view of the conventional LDMOS transistor based on 0.35 μm CMOS process [5]. The conventional device has two p-type buried layers (PBL1 and PBL2). PBL1 enhances the RESURF effect near the gate-side drift edge, and PBL2 contributes to the uniformity of

the electric field in the drift region. PBL2 has an opening under the drain to avoid premature breakdown between the drain and the substrate. The drift region consists of two n-type layers (deep NDL1 and shallow NDL2). NDL2 increases the doping concentration in the shallow drift region, leading to enlargement of SOA due to CE suppression [7]. The field plate (FP) connected to the gate complements the RESURF effect, but increases the switching loss due to the Miller capacitance.

2.2 Proposed LDMOS transistor

Fig. 1(b) shows a cross-sectional view of the proposed LDMOS transistor based on 0.18 μm CMOS process. The x-direction cell pitch of the proposed device (3.555 μm) is 0.17 μm shorter than that of the conventional device. One cell size of the proposed device for the simulation is 3.555 μm × 0.3 μm. The lengths of the drift region and the FP over the drift region of the proposed device are the same as those of the conventional device, respectively. The proposed device has a grounded field plate (GFP) in order to reduce the Miller capacitance. However the GFP increases the on-resistance because it repels the electrons in the drift region in the on-state. In order to reduce the on-resistance, the proposed device further has an n-type layer (NDL3) in the shallow drift region except the close of the gate-side drift region. NDL3 also suppresses CE.



(a) Conventional LDMOS transistor (b) Proposed LDMOS transistor

Fig. 1. Cross-sectional views of the conventional and the proposed LDMOS transistors.

3. Simulation Results

3.1 I_{DS}-V_{DS} characteristics

Fig. 2 shows characteristics of drain current I_{DS} vs. drain voltage V_{DS} of the proposed LDMOS transistor. The proposed device does not have CE for $V_{DS} \leqq 40$ V at the maximum gate voltage rating $V_{GS} = 4$ V and for $V_{DS} \leqq 45$V at an operating gate voltage $V_{GS} = 3.3$V. Therefore the SOA of the proposed device is wide enough for 40V operation. It is also obtained from Fig. 2 that specific on-resistance $R_{on}A$ of the proposed device is 40.9 mΩ·mm^2 at V_{GS} = 3.3 V. The value of the proposed device is about 10% lower than that of the conventional device ($R_{on}A$ = 44.8 mΩ·mm^2 at V_{GS} = 5 V) [5].

3.2 Breakdown characteristics

Fig. 3 shows an I_{DS}-V_{DS} characteristic at V_{GS} = 0 V of the proposed LDMOS transistor. From this, breakdown voltage BV_{DS} is 62 V. The value of BV_{DS} is high enough for 40 V operation. Fig. 4 shows the electric field distribution upon breakdown for the proposed device. High electric field locations causing breakdown are all in the bulk, leading to less damage to the gate oxide and the surface. Therefore the proposed device would have good electric static discharge (ESD) performance, if it is used as ESD devices to ground the gate.

3.3 $R_{on}A$-BV_{DS} characteristics

Fig. 5 shows $R_{on}A$-BV_{DS} characteristics for the conventional device, the proposed device, and the state-of-the-art device presented by UMC [8]. Fig. 5 states that the proposed device is improved, and is comparable to the state-of-the-art device.

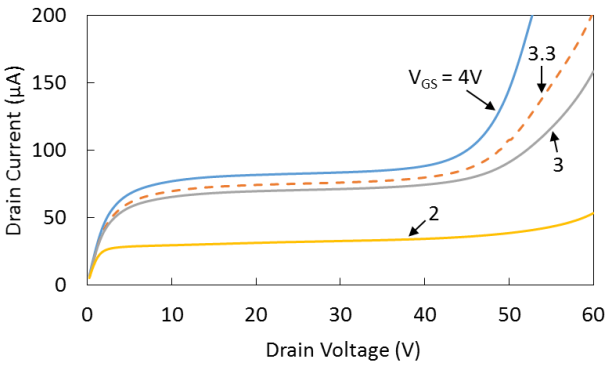


Fig. 2. I_{DS}-V_{DS} characteristics of the proposed LDMOS transistor (one cell).

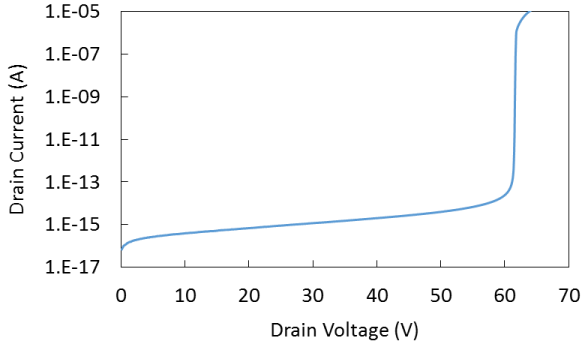


Fig. 3. An I_{DS}-V_{DS} characteristic at V_{GS} = 0 V of the proposed LDMOS transistor (one cell).

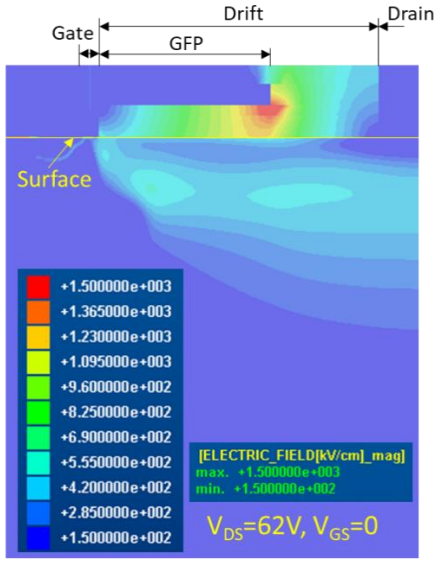


Fig. 4. Electric field distribution upon breakdown of the proposed LDMOS transistor.

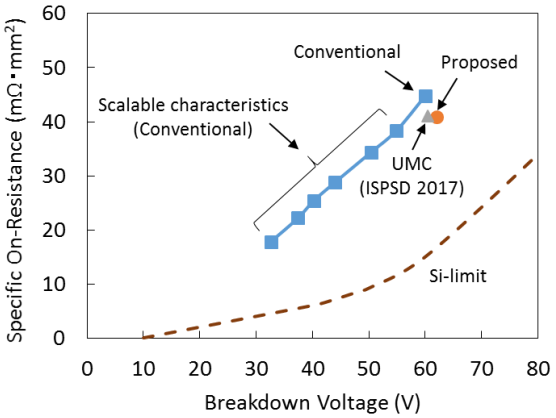


Fig. 5. $R_{on}A$-BV_{DS} characteristics.

3.4 Hot carrier endurance

The hot carrier endurance for LDMOS transistors would largely degrade due to drain avalanche hot carriers (DAHC) when V_{GS} is about half of the maximum gate operation voltage, in this case V_{GS}

≒2 V, and the intrinsic MOSFET operates in the saturation mode. Thus we go over the state of the intrinsic MOSFET at V_{GS} = 2 V. The pinch-off (or saturation) voltage V_P of the intrinsic MOSFET at V_{GS} = 2 V is 0.6 V using the following equation [9].

$$V_P = \frac{(V_{GS} - V_T)}{\alpha} \tag{1}$$

Here, V_T is the threshold voltage, and α is expressed as the following equation.

$$\alpha = 1 + \frac{\gamma}{2\sqrt{\phi_0}} \tag{2}$$

Here, γ is the back-gate coefficient, and ϕ_0 is as follows.

$$\phi_0 = 2\phi_F + 6\Delta_{th} \tag{3}$$

Here, ϕ_F is the Fermi potential, Δ_{th} is the thermal voltage. Fig. 6 shows the dependence of the drain voltage of the intrinsic MOSFET $V_{DS,INT}$, the surface potential at the drain-side gate edge, on V_{DS} at V_{GS} = 2 V. From Fig. 6, V_P (= $V_{DS,INT}$) = 0.6 V corresponds to V_{DS} = 1.9 V. Therefore I_{DS} for V_{DS} ≧ 1.9 V is in the saturation region. Fig. 2 shows that a characteristic of I_{DS} at V_{GS} = 2 V saturates for V_{DS} ≧ 2 V, indicating that the intrinsic MOSFET biased at V_{GS} = 2 V is in the saturation state for V_{DS} ≧ 2 V due to pinch-off, and the high electric field around the gate-side drift region edge might degrade hot carrier endurance.

Fig. 7 shows profiles of the electric field in the x-direction E_x along the surface for the proposed device biased at V_{GS} = 2 V with changing V_{DS} as a parameter. E_x has a peak near the gate-side drift region edge, x ≒ 1000 nm. The peak tends to saturate with increasing V_{DS} due to the RESURF effect enhanced by PBL1, resulting in the suppression of DAHC caused by impact ionization. Therefore the proposed device would likely be able to have high hot carrier endurance.

Fig. 7 also shows that E_x has another peak in a region of 2500 nm ≦ x ≦ 2700 nm due to the electric field concentration at the edges of GFP and PBL2. This high electric field causes impact ionization, but the location of the impact ionization is in the bulk (not shown). Therefore the hot carriers generated in this region would not cause damage to the surface.

3.5 Switching loss and total power dissipation

Fig. 8 shows the circuit for obtaining turn-on characteristics of the conventional and the proposed LDMOS transistors. Time variations of the gate voltage and the gate current during turn-on of the proposed LDMOS transistor are obtained from this circuit (see Fig. 9). From Fig. 9, the gate charge density Q_g/A stored in the gate capacitance during turn-on is 1.18 nC/mm^2. Therefore a figure of merit (FOM) of $R_{on}Q_g$, specific on-resistance × gate charge density, is 48.2 mΩ·nC. The FOM value of the proposed device is about one third lower than that of the conventional device (141 mΩ·nC) [5]. The lower value is due to the smaller Miller capacitance and the lower gate voltage of the proposed device.

The total power dissipation is also obtained from Fig. 8. The total power dissipation for the LDMOS transistor in this circuit consists of (1) the gate driving loss, (2) the switching loss, and (3) the conduction loss. The gate driving loss is caused by charging and discharging the gate capacitance through a resistor connected to the gate. The switching loss is due to the power dissipation of the LDMOS transistor during turn-on and turn-off (see Fig. 10). The conduction loss is due to the power dissipation of the LDMOS transistor during the steady state (see Fig. 10).

Fig. 11 shows the comparison between the conventional and the proposed LDMOS transistors in terms of the switching frequency f dependence of the total power dissipation density P_{DT} with changing the duty ratio D_{ON} as a parameter. In a low switching frequency region for f ≦ 1 MHz,

P_{DT} of the proposed device is almost the same as that of the conventional device for all D_{ON} (= 0.1, 0.5, 0.9). However in a high switching frequency region for f > 1 MHz, P_{DT} of the proposed device is much lower than that of the conventional device with increasing f. Therefore the proposed device is superior to the conventional device in terms of low power dissipation at high switching frequencies.

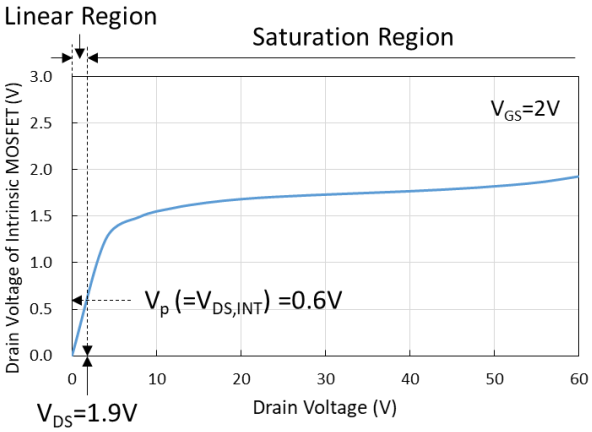


Fig. 6. Drain voltage of the intrinsic MOSFET vs. drain voltage of the proposed LDMOS transistor.

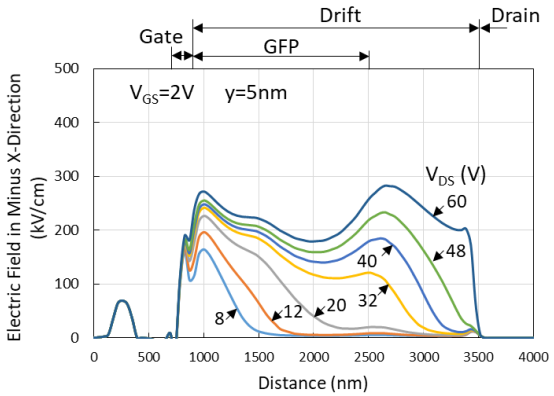


Fig. 7. Profiles of the electric field in the x-direction along the surface of the proposed LDMOS transistor.

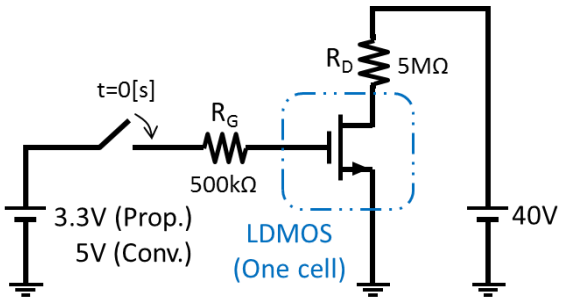


Fig. 8. The circuit for obtaining turn-on characteristics of the conventional and the proposed LDMOS transistors.

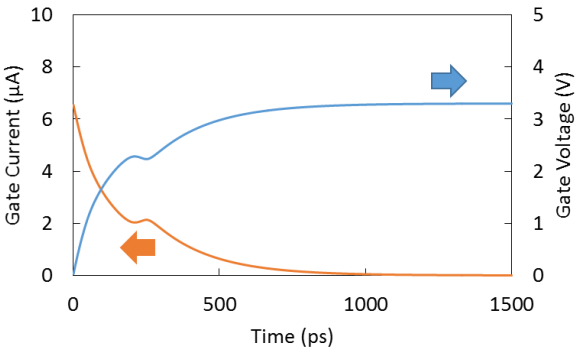


Fig. 9. Time variations of the gate voltage and the gate current during turn-on of the proposed LDMOS transistor (one cell).

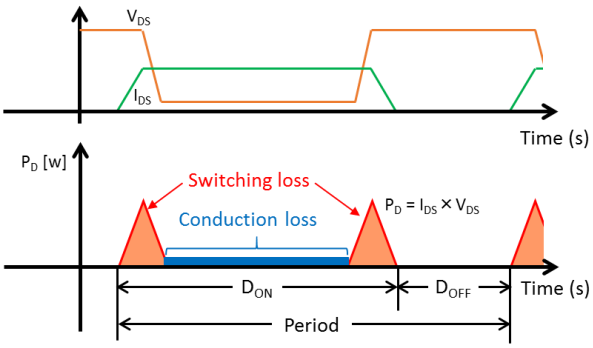


Fig. 10. Switching and conduction losses.

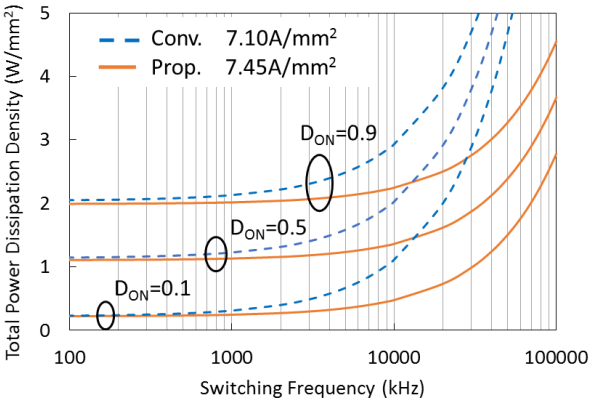


Fig. 11. Switching frequency dependence of the total power dissipation density for the conventional and the proposed LDMOS transistors.

4. Conclusion

The proposed LDMOS transistor used as switching devices in power converters has much lower power dissipation with increasing the switching frequency than the conventional device. This is because the proposed device has the lower Miller capacitance due to the GFP structure. The proposed device also has a state-of-the-art level characteristic of specific on-resistance vs. breakdown. Furthermore the proposed device has a wide SOA enough for 40 V operation, and would likely be able to have high reliability for hot carriers due to the enhanced RESURF effect around the gate-side drift region edge. Therefore the proposed device can be adequately applied to harsh environment automotive applications.

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References

[1] C.-C. Cheng, H. L. Chou, F. Y. Chu, R. S. Liou, Y. C. Lin, K. M. Wu, Y. C. Jong, C. L. Tsai, C.L. Jun Cai, and H. C. Tuan, “Investigation of Parasitic BJT Turn-on Enhanced Two-stage Drain Saturation Current in High-voltage NLDMOS”, 23rd International Symposium on International Power Semiconductor Devices & IC's, ISPSD, pp.208–210, 2011.

[2] S. Poli, S. Reggiani, R. K. Sharma, M. Denison, E. Gnani, A. Gnudi, and G. Baccarani, “Optimization and Analysis of the Dual n/p-LDMOS Device”, IEEE Trans. Electron Devices, Vol. 59, No. 3, pp. 745-753, 2012.

[3] J. Matsuda, M. Kamiyama, N. Tsukiji and H. Kobayashi, “A Proposal of High Reliability LDMOS Structure”, EDD-15-066, SPC-15-148, pp. 11-16, 2015.

[4] J. Matsuda, J. Kojima, M. Kamiyama, N. Tsukiji and H. Kobayashi, “A Proposal of High Reliability Dual RESURF Nch-LDMOS with Low On-resistance”, The 63rd JSAP Spring Meeting, Tokyo Institute of Technology, 20a-S422-11, 2016.

[5] J. Kojima J. Matsuda, M. Kamiyama, N. Tsukiji, and H. Kobayashi, “Optimization and Analysis of High Reliability 30-50V Dual RESURF LDMOS”, in *Proc. ICSICT*, Hangzhou, China, S25-3, 2016.

[6] K. Yamaguchi, M. Harada, T. Kuwabara, and Y. Ohkura, "Device Simulation", Advance Simulation (AdvanceSoft Corporation), Vol. 21, pp. 39-69, 2015.

[7] P. L. Hower, J. Lin, and S. Merchant, “Snapback and Safe Operating Area of LDMOS Transistors”, Technical Digest of International Electron Devices Meeting, IEMD’99, pp. 193–196, 1999.

[8] H.-L. Liu, Z.-W. Jhou, S.-T. Huang, S.-W. Lin, K.-F. Lin, C.-T. Lee, and C.-C. Wang, “A Novel High-Voltage LDMOS with Shielding Contact Structure for HCI SOA Enhancement”, 29th International Symposium on International Power Semiconductor Devices & IC's, ISPSD, pp.311–314, 2017.

[9] Y. Tsividis and C. McAndrew, “Chapter 4 in Operation and Modeling of the MOS Transistor Third Edition”, Oxford University Press, New York (2011).