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A Novel Approach for Velocity Saturation Calculations of 90nm N-channel MOSFET

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Abstract. The drain current equations in the saturation region are the key to characterize and simulate MOSFET devices. It is difficult to obtain so-called pinch-off currents, $\mathrm{I_{ds,sat}}$, accurately, for saturation current characterizations. In this research, we propose an extraction method for the velocity saturation parameter, ν_{sat}, by using drain-to-source currents versus voltages measurement of an N-channel MOSFET with 90 nm process. As far as we have investigated, there is only one paper which describes ν_{sat} extraction for early CMOS process devices; however this is not applicable to advanced fine CMOS device. We show that the extracted ν_{sat} using our proposed method reasonably agrees with measured data without using global optimization functions.

1. Introduction

In characteristic analysis of field-effect transistors (e.g. MOSFETs as well as high-voltage LDMOS transistors and GaN compound transistors used in automotive electronic circuits), it is important to calculate accurately a transition point from the triode to saturation operation regions in its drain current characteristic. This point is so-called pinch-off, and the corresponding current and voltage are called I_{ds_sat} and V_{ds_sat}, respectively. The majority carrier velocity is saturated at the maximum electric field. This velocity saturation parameter is denoted as v_{sat}, and this parameter is a very important physical parameter for the accurate device modeling of the field-effect transistor in most cases.

According to our knowledge, only the reference [1] is the previously published method about velocity saturation extraction without considering series resistance. However, this method is difficult to apply for the device which has double diffusion layers in sub-micron and nanometer technology MOSFETs. The reason is that the diffusion layer with lightly doping acts as a bias dependent resistance, whereas a fixed resistance which the method [1] assumes. The shorter the channel length of transistor is, the larger error we have. Based on these considerations, we proposed an improvement method of varying overdrive voltage through the use of the channel length linearly depending on $L_{m,int}/(1/I_{ds,sat})$ [2]. By following the method, the voltage saturation was estimated to be larger than the actual value. In this paper, we have found that the high accuracy modeling by considering its series resistance using the formulas in BSIM4 [3] circuit simulation model which is one of the sufficiently accurate compact models.

2. Derivation of ν_{sat} in Nanometer MOSFET

Saturation voltage in the long channel MOSFET excluding bulk charge is equal to $\mathbf{V_{gs} - V_{th}}$, and the drain current is proportional to $((V_{gs} - V_{th}) * V_{ds} - V_{ds}^2)/2$. When the bulk charge is taken into account, $V_{ds,sat}$ and I_{ds} in deep sub-micron and nanometer processes are derived by inversion charge calculations in BSIM4 model to satisfy the following equations:

$$V_{ds,sat} = \frac{V_{gst}}{A_{bulk}} \tag{1}$$

$$I_{ds} = \frac{W_{eff}}{L_{eff}} \mu_{eff} C_{ox} \left(V_{gst} \cdot V_{ds} - \frac{1}{2} A_{bulk} V_{ds}^2 \right) \tag{2}$$

Here, A_{bulk} is an internal variable about bulk, in equations (1) and (2), and it is given as follows;

$$A_{bulk} = \left(1 + \frac{K_1}{2\sqrt{(\emptyset_s - V_{bs})}} \left\{ \frac{(A_0 L_{eff})}{L_{eff} + 2\sqrt{X_j X_{dep}}} \cdot \left(\left[1 - A_{gs} V_{gst} \left(\frac{L_{eff}}{L_{eff} + 2\sqrt{X_j X_{dep}}} \right)^2 \right] \right) + \frac{B_0}{W_{eff} + B_1} \right\} \right) \cdot \frac{1}{1 + K_{ETA} V_{be}} \tag{3}$$

In equation (3), K_1, A_0, A_{gs}, B_0, and B_1 are model parameters. W_{eff} is the effective channel width, L_{eff} is the effective channel length, X_j is the junction depth, and X_{dep} is the depletion layer width. According to the BSIM4 model manual, A_{bulk} can be approximated to one when L_{eff} is sufficiently small. Hence, the saturation current, $I_{ds,sat}$, at the pinch off voltage $V_{ds,sat}$ is provided as follows**:**

$$I_{ds,sat} = W_{eff} C_{ox} (V_{gst} - A_{bulk} V_{ds,sat}) \nu_{sat} \tag{4}$$

$$V_{gst} = V_{gs} - \mathrm{V_{th}} \tag{5}$$

Based on equations (4) and (5), the velocity saturation, ν_{sat}, is obtained as follows;

$$\nu_{sat} = \frac{I_{ds,sat}}{W_{eff} C_{ox} (V_{gst} - V_{ds,sat})} \qquad (L_{eff} < 90\ \ nm) \tag{6}$$

3. Velocity Saturation Extraction Method with Measurements

In our experiments, 90 nm N-channel MOSFETs have been fabricated. Where, the oxide film thickness (T_{ox}), the mask channel length (L_{mask}), and the mask channel width (W_{mask}) are 2.5 nm, 0.1 µm, and 10 µm, respectively.

Derivation of ν_{sat} is based on the effective channel length, L_{eff}, the gate capacity per unit area C_{ox}, the threshold voltage V_{th}, the pinch-off voltage $V_{ds,sat}$, the pinch-off current $I_{ds,sat}$, and the gate source voltage V_{gs} at the pinch off. The three internal variables W_{eff}, C_{ox} and V_{th} are constants in each transistor. The derivation procedure of $V_{ds,sat}$, $I_{ds,sat}$, V_{gs}, is shown below.

I_{ds} — V_{ds} graph (Fig.1) in 90 nm N-channel MOSFET was used for measurement. In Fig. 1, I_{ds} graph was differentiated twice with respect to V_{ds} to obtain each pinch-off point as shown in Fig. 2. Intersection points of the interpolation lines with the above calculations using the measured curves are named as $V_{ds,sat1}$ through $V_{ds,sat5}$. The total number of $V_{ds,\ sat}$ values (five) are the number of V_{gs} steps.

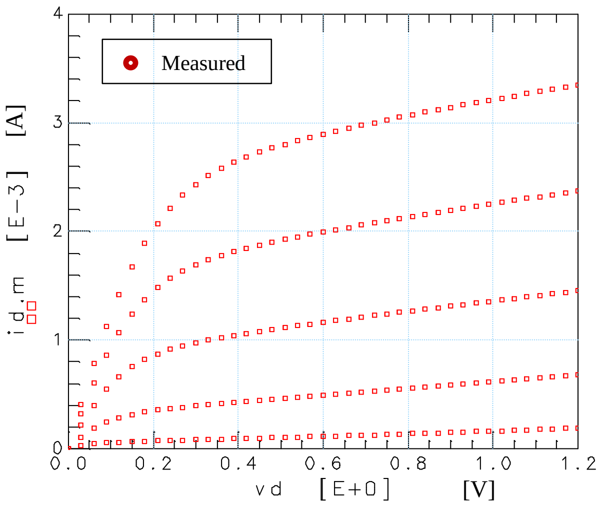

Fig. 1. I_{ds} — V_{ds} measurement of the 90 nm N-channel MOSFET (L_{mask} = 0.1 μm, W_{mask} = 10μm).

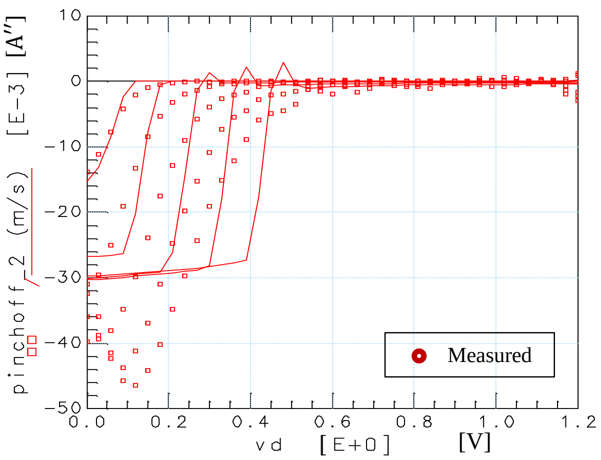

Fig. 2. Second-order derivative of the I_{ds} — V_{ds} characteristics.

The saturation current is named as $I_{ds,sat1}$ for $V_{ds,sat1}$, and it is named as $I_{ds,sat2}$ for $V_{dsa,sat2}$, and so on. A curve which interpolates these 5 points was obtained by fitting with function formulas that we developed for $V_{ds,sat}$ and $I_{ds,sat}$, respectively (see Fig. 3).

$$V_{ds,sat} = PEAKV - ANG * BASE^{V_{gs}} \tag{7}$$

$$I_{ds,sat} = ANGI * \exp(BASE * V_{gs}) - PEAKI \tag{8}$$

In equation (7), $V_{ds,sat}$ converges to a constant value PEAKV with increase of V_{gs}. The peak value is named as $V_{ds,sat}$, at $V_{gs} = 2.68\text{V}$. Also we have assigned the peak value to equation (8), and then obtained the $I_{ds,sat}$ value.

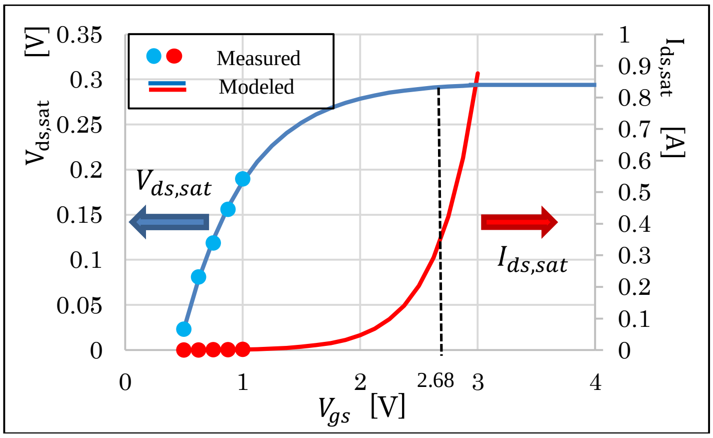

Fig. 3. The fitting with the peak function result of $V_{ds,sat}$ and $I_{ds,sat}$.

Based on the above steps, we have obtained $V_{ds,sat}$, $I_{ds,sat}$, V_{gs}, and other necessary values for the calculation of v_{sat} from the fitting functions. Velocity saturation is calculated by equation (6) with these values as $\mathbf{v_{sat}} = \mathbf{706\ Km/s}$. The $\mathbf{v_{sat}}$ value is defined as a model parameter of BSIM4. We optimized and extracted other DC drain current model parameters, precisely, in advance of v_{sat} extraction. Simulated data in Fig. 4 is the result of our SPICE compatible simulator called MDW-SPICE using the extracted v_{sat}. It is observed that there are some discrepancies between the simulated and the measured data. We, therefore, will describe its remedy in the next section.

4. Correction by Source Drain Series Resistance

In this N-channel MOSFET of 90 nm process, the contact resistance part between the probe needle and a pad at the measurement and the bias dependence resistance of LDD diffusion layer are in series. These resistances cause some voltage drops which decrease $V_{ds,sat}$ inside of the device.

Sum of the source and drain contact resistances is defined as R_X. Intrinsic resistances of the diffusion and LDD layer are defined as RDSW, which is a resistance model parameter of the unit channel width resistance of the BSIM4 model.

Referring to the BSIM4 model equations, we have the following:

$$\boldsymbol{V_{ds,sat\_new} = V_{ds,sat} - (RDSW[Vgs = 2.68V] \cdot W_{eff} \cdot 100 + R_X) \cdot I_{ds,sat}} \quad (9)$$

V_{ds,sat_new} obtained from equation (9) is re-assigned to equation (6). We have calculated v_{sat}, again, and then obtained $\boldsymbol{v_{sat} = 115}$ $[\mathbf{Km/s}]$. By applying the $\mathbf{v_{sat}}$, we have simulated with MDW-SPICE using the same conditions described in Fig. 4. The simulation results are shown in Fig. 5, and we see that simulated I_{ds} agrees with the measurement result, accurately.

5. ν_sat Verification with Measurements

Comparison between simulation with our ν_{sat} extraction result ($\nu_{sat} = 706$ [Km/s]) and the measured data is shown in Fig. 4. They agree well for small I_{ds}, however, error increases with an increase of I_{ds}. As mentioned in previous sections, this error is caused by the voltage drop of the series resistances. After taking it into account and re-calculate the equation (9), the improved result, $\nu_{sat} = 115$ [Km/s], is obtained. Fig. 5 shows the simulation and measurement results. They agree well compared to the data in Fig. 4.

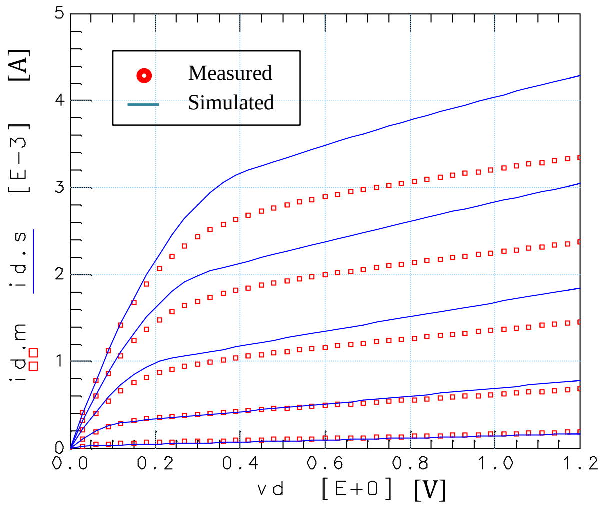

Fig. 4. I_{ds}—V_{ds} characteristics based on the new model before correction.

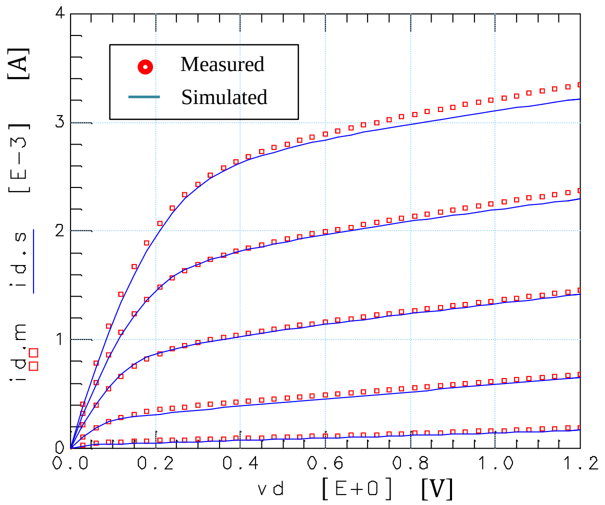

Fig. 5. I_{ds}—V_{ds} characteristics based on the new model corrected by series resistance.

6. Conclusion

In this paper, we have proposed a novel extraction method of ν_{sat}. In our experiments using measured data of nanometer MOSFETs, we have obtained the accurate extraction result. This method is based on BSIM4 model, and is applicable to recent advanced processes and devices. The extraction method is expected to be highly effective for many kinds of field-effect transistors besides MOSFETs.

We also plan to make a study on the resistance extraction method inside the channel with high degree of precision, which enables highly accurate correction with gate bias voltage dependence.

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