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Self-adjustable Notch Frequency in Noise Spectrum of Pulse Coding DC-DC Converter for Communication Devices

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Abstract. This paper proposes a novel EMI spread spectrum technology with the adjustable notch frequencies using the automatic setting the notch frequency with the pulse coding method of the DC-DC switching converter for the communication equipment. In the communication devices, it is desired to be little noise around the frequency of the receiving signal. We have proposed having the notch characteristics in the noise spectrum of the switching pulse using pulse coding method. In this paper, the notch frequency is automatically set to that of the received signal by adjusting the clock frequency using the equation Fn=(N+0.5)Fck. We have examined the theoretical notch frequency which is adjustable in the Pulse Width Coding (PWC) controlled converter using the equation $Fn=N/(W_1-W_2)$.

1. Introduction

In recent years, the circuit of the communication devices has been accelerated to be higher density packaging. The power of the switching converter has become large and large and the fluctuation of the switching noise has strongly spread in the wide frequency range. So it is very important to reduce an Electro Magnetic Interference (EMI) noise by suppressing the peak levels at the fundamental frequency and its harmonic frequencies [1,2].

On the other hand, for the communication equipment including the radio receiver, it is very important to reduce the radiation noise at the specific frequencies, such as the receiving frequency, by suppressing diffusion of power supply noise. We have proposed the pulse coding technique to have the notch characteristics at the random frequency in the noise spectrum of the switching converter [3,4].

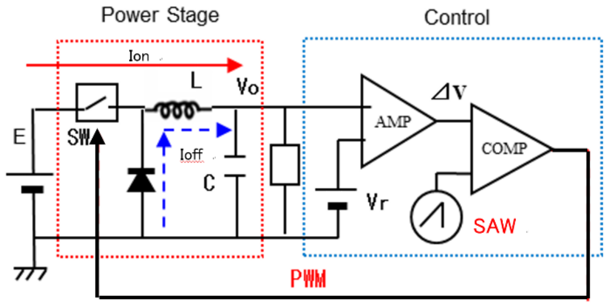
In this paper, we show the EMI reduction and the notch frequency in the noise spectrum of the switching converter, and show the experiment of the notch characteristics using the PWC method.

2. Switching Converters with Spread Spectrum

2.1 Basic DC-DC Switching Converters

Fig. 1 shows the basic block diagram of the buck type DC-DC converter with the PWM (Pulse Width Modulation) signal and Fig.2 shows its main signals. This converter consists of the power stage and the control block. The power stage contains a main power switch, a free-wheel diode, an inductor and an output capacitor. The main switch is controlled by the PWM signal from the control block, which consists of an operational amplifier, a comparator and a reference voltage source. The comparator generates the PWM signals compared a saw-tooth signal and the amplified error voltage.

When the switch is ON, the inductor current flows from the input voltage source E and charges the output capacitance shown as the solid line in Fig. 1. When the switch is OFF, the inductor current flows through the diode shown as the dashed line in Fig.1.



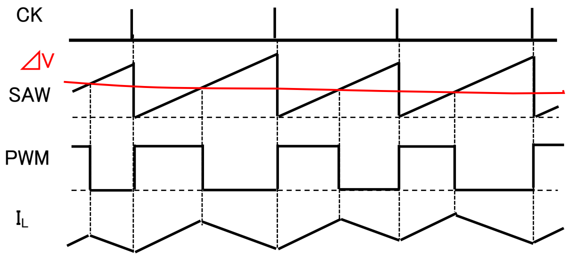
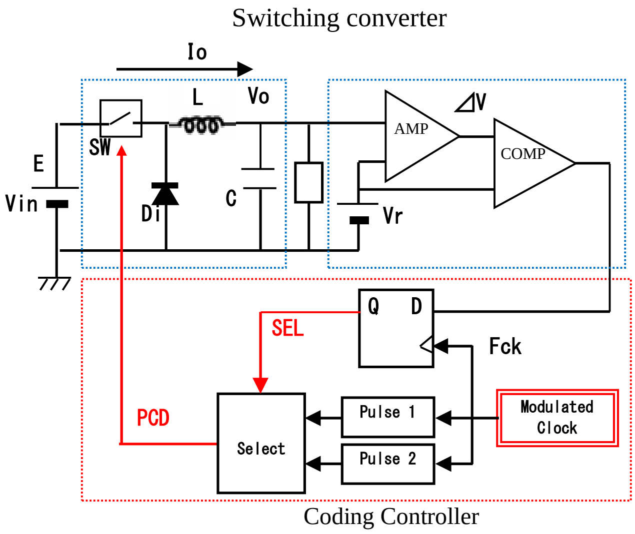


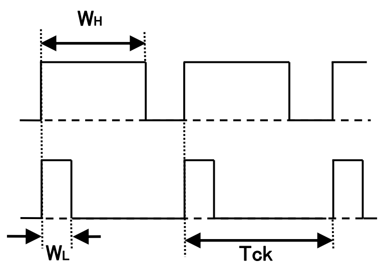
Fig.1 Switching buck converter with PWM signal Fig.2 Waveform of switching buck converter

2.2 EMI Reduction and Pulse Coding Method

In order to reduce the radiation from the power switching, random shaking is usually used by shaking the phase or frequency of the clock shown in Fig. 3, which also shows the pulse coding circuit. In Fig. 3, the input of the comparator is the reference voltage and its output is connected to the D-type flip-flop (D-FF) in the coding controller.

In the coding controller, there are two pulse generators, whose pulse widths are different each other to perform the pulse with coding control. These coding pulses are selected by the select signal SEL from the D-FF. On the other hand, these coding pulses are generated using the phase (or frequency) modulated clock pulse. Fig. 4 shows the two coded pulses and their conditions from the pulse generators.





●Conditions
Tck =5.0μs

★Pulse 1
W_H = 4.0μs
$D_H = W_H/T_{ck}$ =0.80

★Pulse 2
W_L = 0.75μs
$D_L = W_L/T_{ck}$= 0.15

Fig.3 Converter with EMI reduction & PWC control Fig.4 Coded pulses of PWC control

2.3 Simulation Results of EMI Reduction & Notch Frequency in the Noise Spectrum

The conditions of the converter shown in Fig. 3 are Vi=10V, Vo=5.0V, Io=0.2A, Fck=200kHz and the pulse coding parameters are shown in Fig. 4. Here three spectrographs are shown in Fig. 5 and Fig. 6, Fig. 5(a) and Fig. 5(b) are the spectrum of the standard buck converter, that of without EMI reduction converter and with EMI reduction converter. Comparing Fig. 5(b) with Fig. 5(a), the peak level of the clock frequency (200 kHz) is reduced from 3.5V to 2.0V that is 4.9 dB reduction. The peak levels of the harmonic frequencies are greatly reduced to be less than 100 mV. On the other hand, the bottom levels of the spectrum are higher than 8 mV. This is not so good for the communication devices which receive weak radio waves. In Fig. 6, there is the spectrum of the proposed converter with the pulse width coding method, there appears the notch characteristics at the frequency of 770 kHz whose bottom level is less than -20 dB. In this converter, the clock frequency is 500 kHz.

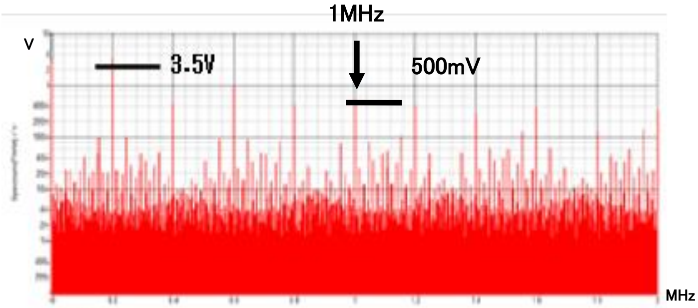


Fig. 5(a) Simulated spectrum without EMI reduction

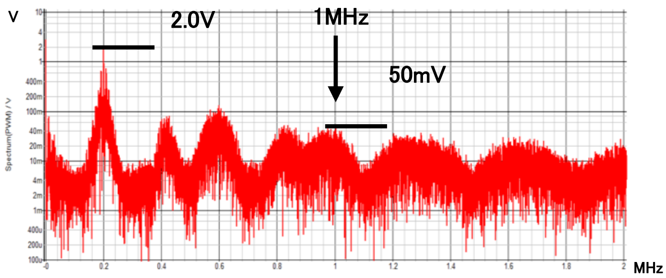


Fig. 5(b) Simulated spectrum with EMI reduction

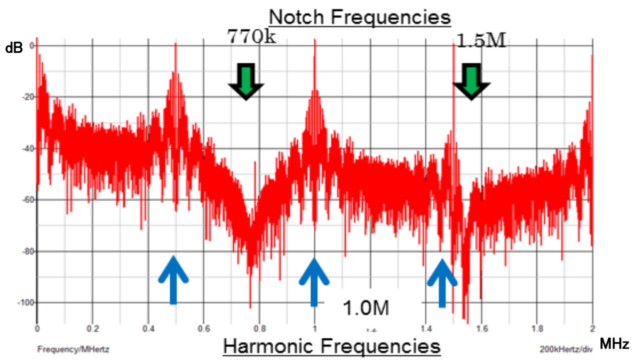


Fig. 6 Simulated spectrum with PWC control

2.4 Derivation of Theoretical Notch Frequency

The PWM pulse of the PWC converter is the random series of the two pulses shown in Fig. 4. The theoretical frequency of the PWC control is derived as bellow, performing fast Fourier transform to the pare of the coding pulses.

$$F(\omega) = \int_{-\infty}^{\infty} f(t) e^{-j\omega t} dt = \int_{0}^{t_1} e^{-j\omega t} dt + \int_{\frac{T}{2}}^{\frac{T}{2}+t_2} e^{-j\omega t} dt \quad (1)$$

$$= \frac{1}{\omega} (\sin(\omega t_1) - \sin(\omega t_2) + jcos(\omega t_1) - jcos(\omega t_2) \quad (2)$$

The absolute value of above complex Eq.(2) is shown in the next sinc function (3).

$$|F(\omega)| = \frac{1}{\omega}\sqrt{4sin^2\left(\frac{\omega t_2-\omega t_1}{2}\right)} = (t_2 - t_1)sinc\left(\frac{t_2-t_1}{2}\omega\right) \quad (3)$$

Where ω=2πf, so the notch frequencies are shown in the following equation. Here, N is the natural number. In the Eq.(4), it depends on the difference of the pulse width only, not depends on the period of the control pulse.

$$f_n = \frac{N}{(t_2-t_1)} \quad (4)$$

3. Experimental Result of the PWC Converter

3.1 Experimentation of the PWC Converter

Fig. 7 shows the experimental noise spectrum, the PWM signal and the SEL signal of the PWC converter. The parameters of this converter are as follow: the clock frequency is about 160kHz (the period Tck=6.25μs) and the pulse conditions are W_H=5.0μs and W_L=1.3μs respectively. In this case, the theoretical notch frequency is 270 kHz and the appeared notch frequency is 274kHz. This experimental notch appears between the clock frequency 160kHz and the twice frequency 320kHz. Another notch at twice frequency (540kHz) does not appear in this figure.

Fig. 8 shows the output voltage ripple and the step response when the output load current changes between 0.33A and 0.53A. There are many spike noises of the clock pulse, so the bandwidth is limited to 2.0 MHz in this figure. The static voltage ripple is 8mVpp at Io=0.33A and 15mVpp at Io=0.53A. The overshoot/undershoot of the step response is ±18mV when the output current step is ±0.2A.

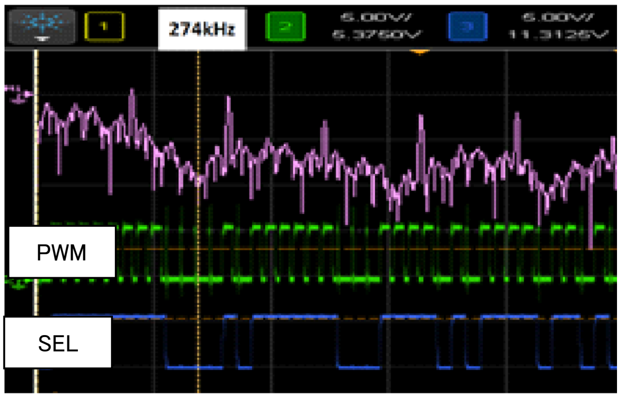


Fig.7 Experimental spectrum of PWC converter 1

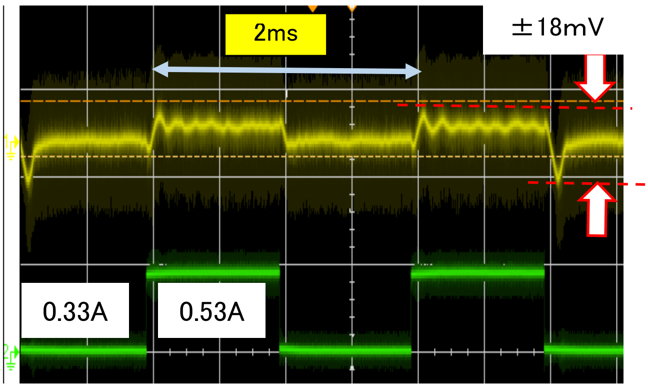


Fig.8 Experimental output voltage ripple

3.2 Experimental Notch Frequency in Noise Spectrum

Fig. 9 shows the experimental another spectrum, the notch frequency is 350kHz which appears between the first and second harmonic frequency (320k and 640kHz) of the clock. Here the conditions of the coded pulses are W_H=4.0μs and W_L=1.1μs respectively and the theoretical notch frequency is 345kHz. The clock frequency is Fck=160 kHz.

According to the Eq.(4), many notches will appear in the noise spectrum. In Fig. 9, there is the second notch at 700kHz.

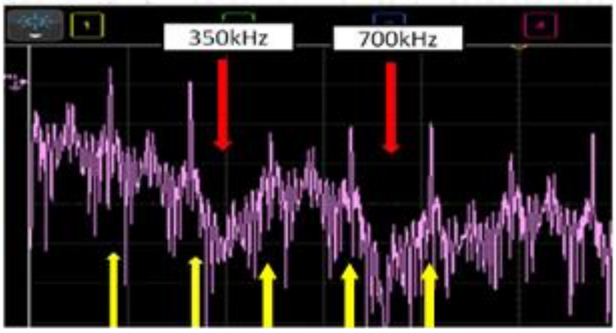


Fig.9. Experimental spectrum of PWC converter 2

4. Automatic Self-Adjusting the Notch Frequency

4.1 Relationship with the Clock and the Notch

Generally speaking, it is good for the notch frequency Fn to appear at the middle between the clock frequency Fck and its twice frequency 2Fck as shown in Fig. 7. In this case, Fn will be equal to the frequency of the receiving signal Fin. The relationship between Fin and Fck is shown as the next equation, which is easy to be set using the PLL (Phase Locked Loop) circuit.

$$F_{in} = 1.5F_{ck} \quad \text{or} \quad \frac{F_{in}}{3} = \frac{F_{ck}}{2} \tag{5}$$

On the other hand, the duty Do of the PWM signal in the switching converter is usually represented like Do=Vo/Vin, here Vo is the output DC voltage and Vin is the input DC voltage respectively. Hence the pulse width To of the PWM signal is represented shown in the Eq.(6).

According to the Eq.(4), the period of the notch frequency Tn is derived from the difference between the pulse width of W_H and W_L, here W_H or W_L means t_2 or t_1 in the Eq.(4) respectively. In this case, W_H, W_L and To have the relations shown in the Eq.(6) ~ (8) in order to control the output voltage Vo stable. Here, Tp equals W_H - To or To - W_L .

$$T_o = D_0 \times T_{ck} = \frac{V_o}{V_{in}} \times T_{ck} \tag{6}$$

$$W_H = T_o + T_p \quad W_L = T_o - T_p \tag{7}$$

$$\therefore \quad T_n = W_H - W_L = 2 \times T_p \tag{8}$$

4.2 Simulation Circuit and the Major Waveform

Fig. 10 shows the block diagram of the control part of the proposed converter. The received signal Fin and the generated clock signal are synchronized by the PLL circuit concerned with the equation (5). PLL signals are synchronized as shown in Fig.11 (VCO: Voltage Control Oscillator, LPF: Low-Pass Filter). In Fig. 10, P_H means the pulse 1 with the wide pulse width and P_L with the narrow pulse width. In order to generate the coding pulses P_H and P_L, the periods of the signals (Fin and Fck) are measured with the counters and their data are kept in the data registers. From half of these measured values, half values of them are calculated to generate the coding pulses P_H and P_L.

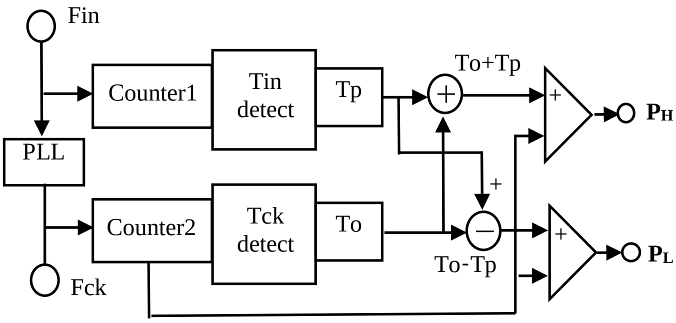


Fig.10. Block diagram of the proposed circuit

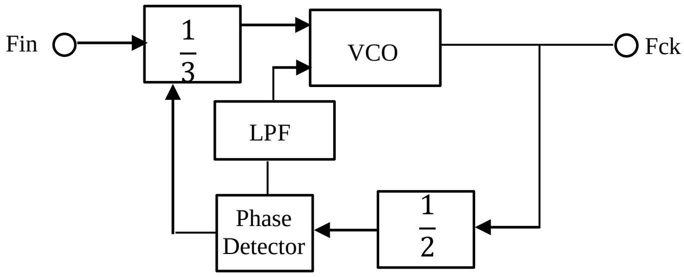


Fig.11. The generation of PLL synchronized signals

The simulation use SIMetrix-SIMPLIS and Fig. 12 shows the synchronized signals of Fin and Fck and Fig. 13 shows the major signals of Fig. 10. The frequency of Fin is 750kHz and that of Fck is 500kHz.

In our converter, Vin=10V and Vo=5.0V, so Do=0.5 from the Eq.(6). When the frequency of the input signal is set at Fin=750kHz, the frequency of the clock is guided Fck=500kHz by the Eq.(5). Then the simulated clock frequency Fcks is 500kHz as shown in Fig. 9. Then the calculated frequency Tpc is decided as Tpc=Tn/2=Tin/2=0.67μs from the Eq.(8). By the Eq.(7), the pulse widths of the simulated coding pulses are guided as W_{HS} =1.67μs and W_{LS} =0.33μs.

Fig. 13 shows the coding pulses in the PWM signal, here W_{HS} =1.64μs and W_{LS} =0.36μs. In this case, the theoretical simulation notch frequency is appeared at Fnso=780kHz. Fig.14 shows the experimental spectrum using the derivation method from Eq.(6) ~ (8). Here, the experimental notch frequency appears at Fns=790kHz, which is almost equal to the theoretical notch frequency Fnt=750kH.

Fig. 15 shows the output voltage ripple for the dynamic load regulation when the load current changes is 0.5A. The static output voltage ripple is less than 2mVpp and the overshoot or the undershoot is about ±28mV.

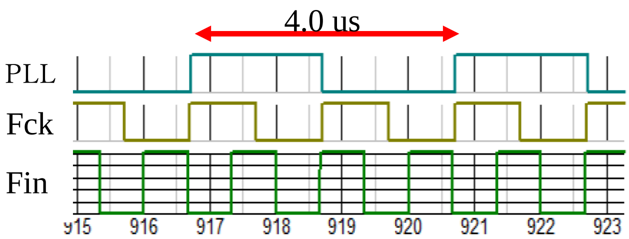


Fig.12 Waveform of PLL circuit (Tin:Tck=2:3)

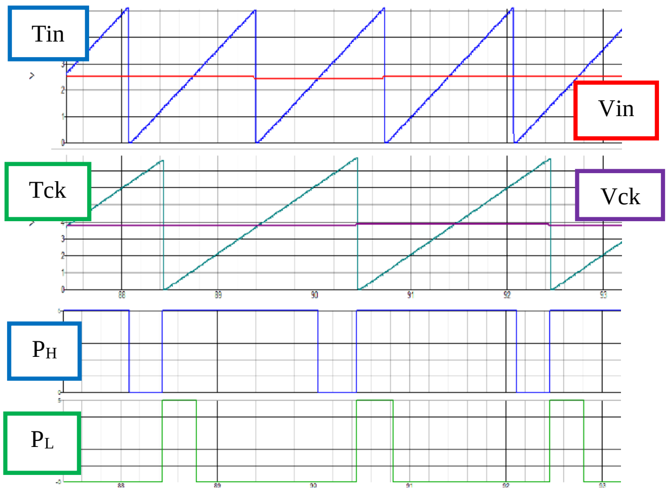


Fig.13 Major waveform of Fig.10 (Fin=750 kHz)

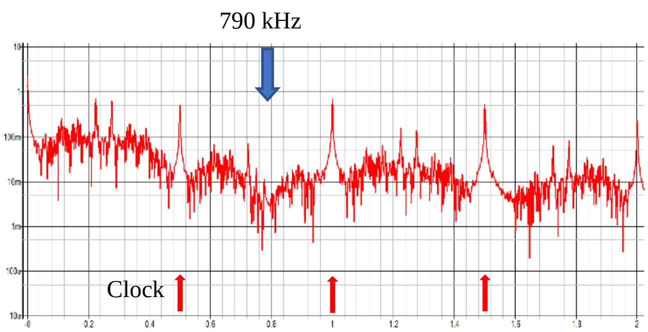


Fig. 14 Noise spectrum with pulse coding

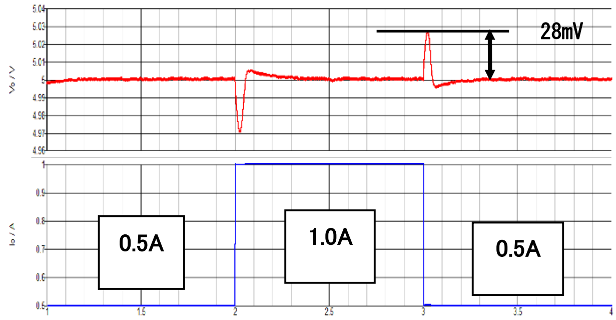


Fig.15 Output voltage ripple with ⊿Io=±0.5A

4.3 Simulated Noise Spectrum of PWM Signal

Fig. 16 shows the noise spectrum of the pulse coding converter. Here, the automatic notch frequency appears at about 750kHz which is the input frequency. In this case, the 1st notch appears between the clock frequency and the 2nd harmonic frequencies. There are the 3rd and 4th harmonic notches at the frequency 2.25MHz and 3.0MHz.

Fig. 17 shows the another noise spectrum, where the notch appears between the 2nd and the 3rd harmonic frequencies. The bottom level is about 1mV.

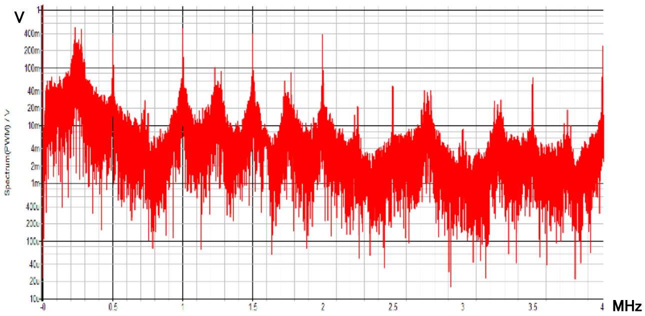


Fig.16 Simulated noise spectrum of proposed system

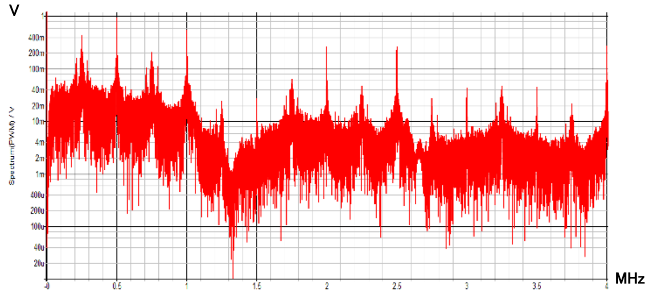


Fig. 17 Another simulated noise spectrum

4.4 Simulated Noise spectrum of PWM signal

In the communication devices, there are many changes of the receiving signal and the input frequency. It is important for these devices to response quickly for the frequency changes. Fig.18 shows the responses of our proposed converter when N=1, here Fck=750kHz when Fin=1.0MHz. There are the output voltage ripple and the response of the PLL circuit when Fin changes 0.5M/1.0MHz. Here the waveform of Tck shows the response of the PLL circuit. The static voltage ripple is 15mVpp at Fin=0.5MHz and 8mVpp at Fin=1.0MHz. The undershoot is about 15mV and the settling time is about 150μs.

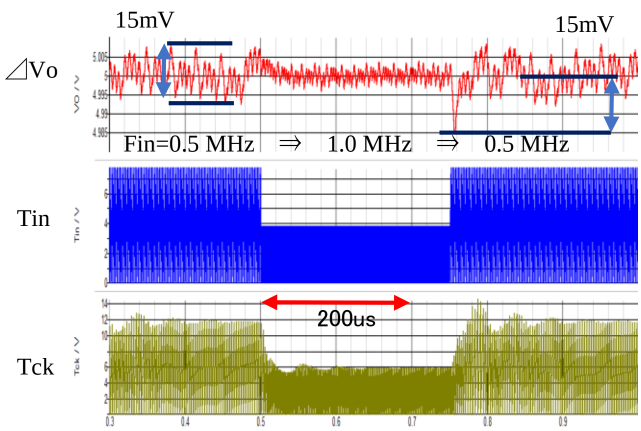


Fig. 18 Transient response with Fin change

5. Conclusion

This paper proposes a new technique to automatically generate the notch characteristics at the desired frequency in the noise spread spectrum of the switching converter. In order to generate the notch frequency, the clock frequency and the coding pulses are automatically generated using the PLL circuit. The notch frequency appears between the clock frequency and the 2nd harmonic frequency, or between the 2nd and 3rd harmonic of the clock frequencies.

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