Redundant SAR ADC Algorithm for Minute Current Measurement


Division of Electronics and Informatics
Gunma University

Kobayashi Laboratory
OUTLINE

• Introduction

• Problems & Solutions Minute Current Measurement

• SAR ADC & Redundancy Design

• Redundancy Design using Fibonacci Sequence

• New Discovery of Fibonacci Sequence Weighted SAR ADC

• Conclusion
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Minute current measurement using **SAR ADC**

**Research Objective**

- **Sample & Hold**
  - **Settling Time**
  - **Large**

**Very small current input** $I_{in}$

**SAR ADC**

**Binary type** or **Redundant type**

**SAR**: Successive Approximation Register
Our Approach

Each step time can be shorter

Binary type $\rightarrow$ Redundant type

Possibility of Measurement time reduction
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Problem of Minute Current Measurement

Using SAR ADC

- Sample Hold
- Comparator
- SAR Logic
- DAC
- Clock
- Digital Output

Input

\( V \)

Settling time

SH circuit voltage

\( t \)
Solution

Reduction each step measurement time

Increase measurement speed
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  ➢ SAR ADC
  ➢ SAR ADC Redundancy Design

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SAR ADC Configuration

Based on the principle of balance

Generally use binary weight

(1, 2, 4, 8, 16, 32, 64 ...)

Balance scale

Object

Sample Hold

Comparator

DAC

SAR Logic

Digital Output

Analog Input

Clock

Weight

1 2 4
Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input: 7.3 [V]
- Binary weight: 16, 8, 4, 2, 1

<table>
<thead>
<tr>
<th>Step</th>
<th>Weight p(k)</th>
<th>1st</th>
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Binary weight: 16, 8, 4, 2, 1

Analog Input: 7.3 [V]

Left? Right?
5bit-5step SAR ADC

- Analog Input: 7.3 [V]
- Binary weight: 8, 4, 2, 1

Binary Search SAR ADC Operation

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</table>
## Binary Search SAR ADC Operation

### 5bit-5step SAR ADC

- **Analog Input:** 7.3 [V]
- **Binary weight:** 2, 1

#### Analog Input: 7.3 [V]

![Analog Input diagram](image)

- **Level:**
  - Upper step: 16
  - Lower step: 7.3

- **Weight p(k):**
  - 31
  - 30
  - 29
  - 28
  - 27
  - 26
  - 25
  - 24
  - 23
  - 22
  - 21
  - 20
  - 19
  - 18
  - 17
  - 16
  - 15
  - 14
  - 13
  - 12
  - 11
  - 10
  - 9
  - 8
  - 7
  - 6
  - 5
  - 4
  - 3
  - 2
  - 1
  - 0

- **Step:**
  - 1st
  - 2nd
  - 3rd
  - 4th
  - 5th

- **output:**
  - 31
  - 30
  - 29
  - 28
  - 27
  - 26
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  - 6
  - 5
  - 4
  - 3
  - 2
  - 1
  - 0

- **Left:**
  - 2, 1

- **UP!**
Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input: 7.3 [V]
- Binary weight:

\[ 7.3 \Rightarrow 00111 \Rightarrow 7 \]

\[ 16 - 8 - 4 + 2 + 1 + 0.5 - 0.5 = 7 \]
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Redundancy

- Surplus, Extra

Using time redundancy

- Extra comparison steps
- Change reference to non-binary voltages

Enable digital error correction!

$q(k)$: $k$-th step correctable difference
Redundancy Design Operation (No Error)

4bit-5step SAR ADC

- Analog input: 6.3
- Redundant weight: 16, 10, 6, 3, 2, 1

**Correctable expression**

6.3 → 010001 → 6

16 − 10 + 6 − 3 − 2 − 1 + 0.5 − 0.5 = 6
Redundancy Design Operation (One Error)

4bit-5step SAR ADC
- Analog input: 6.3
- Redundant weight: 16, 10, 6, 3, 2, 1

Correctable expression
6.3 → 010001 → 6

Another expression
6.3 → 01111 → 6
16 - 10 - 6 + 3 + 2 + 1 + 0.5 - 0.5 = 6

Error correction → High-Reliability
**Redundant Search SAR ADC Speed**

**Binary search**

<table>
<thead>
<tr>
<th>Step1</th>
<th>Step2</th>
<th>Step3</th>
<th>Step4</th>
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**5bit SAR ADC**

<table>
<thead>
<tr>
<th>Step1</th>
<th>Step2</th>
<th>Step3</th>
<th>Step4</th>
<th>Step5</th>
<th>Step6</th>
<th>Step7</th>
</tr>
</thead>
</table>

**Error correction**

- **Early steps:** relaxing comparative condition → increase ADC speed
- **Later steps:** correct misjudgment

Each step time is shortened → ADC speed increases
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Fibonacci Sequence

**Definition** \((n=0,1,2,3...)\)

\[
F_0 = 0 \\
F_1 = 1 \\
F_{n+2} = F_n + F_{n+1}
\]

**Fibonacci number**

\[0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, \ldots\]

**Property**

The closest terms ratio converges to **"Golden Ratio"**!

\[
\lim_{n \to \infty} \frac{F_n}{F_{n-1}} = 1.6180339887 \ldots = \phi
\]
Fibonacci Sequence Weighted SAR ADC

Weight is Fibonacci sequence
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We consider settling time of Sample & Hold circuit

Measurement time

Binary type SAR ADC

\[ V \]

Fibonacci type SAR ADC
Simulation Conditions (1/2)

- Input signal: Current source ⇒ Voltage source
- Consider settling time of Sample & Hold circuit
Simulation with scilab
Resolution: 1 ~ 14bit
Accuracy: $\frac{1}{2}$ LSB
Initial voltage of capacitor: Half of full scale
Simulation Method (1/3)

Clock generation from worst case (Ex. 5 bit)

- Fibonacci type clock
- Binary type clock

Graph:
- S&H circuit voltage
- Input voltage

- $V_t$
- $O$
- $t$
- $1/2$ LSB
- $32$
- $16$
Simulation Method (2/3)

Judgment / Change (Binary & Fibonacci)

\( V_{in} = 0 \sim 32 \)

- **LSB or less**
  - \( \Rightarrow \) Judgement end
- **Others**
  - \( \Rightarrow \) Clock increase
  - \( \Rightarrow \) Judge again

- **S&H circuit output**
- **Input voltage**
- **Judgment result**

Binary or Fibonacci clock
Determination Example (1/3)

When $V_{in} = 32$

**Binary type**

**Fibonacci type**

![Graph showing S&H circuit voltage and comparison voltage for binary and Fibonacci types. The Fibonacci type shows a misjudgment at certain points.](image-url)
When \( V_{in} = 25 \)

**Binary type**

**Fibonacci type**

Misjudgment
When $V_{in} = 16$

**Binary type**

**Fibonacci type**
Simulation Results

Relationship number of bits & measurement time

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- **Binary type**
  
  \[ y = 0.3604x^2 - 0.9909x + 1.5912 \]

- **Fibonacci type**
  
  \[ y = 1.0321x - 0.8573 \]
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Conclusion

Minute current measurement using SAR ADC

Consider settling time of sample & hold circuit

• Binary type (Redundancy: 😞) : Complete settling
• Fibonacci type (Redundancy: ☹️) : Incomplete settling

Reduction of each step measurement time

Measurement time

Binary SAR ADC > Fibonacci SAR ADC
Thank you for listening

Golden Ratio

1.62

1