Redundant SAR ADC Algorithm for Minute Current Measurement

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OUTLINE

- Introduction
- Problems & Solutions Minute Current Measurement
- SAR ADC & Redundancy Design
- Redundancy Design using Fibonacci Sequence
- New Discovery of Fibonacci Sequence Weighted SAR ADC
- Conclusion

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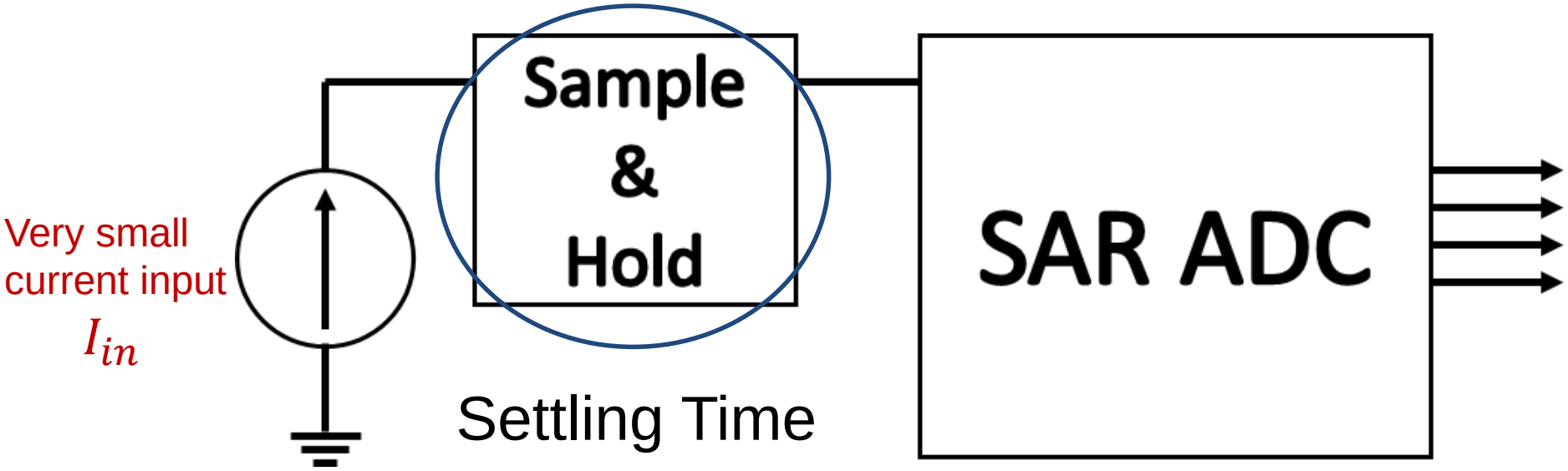
Research Objective

Minute current measurement using SAR ADC



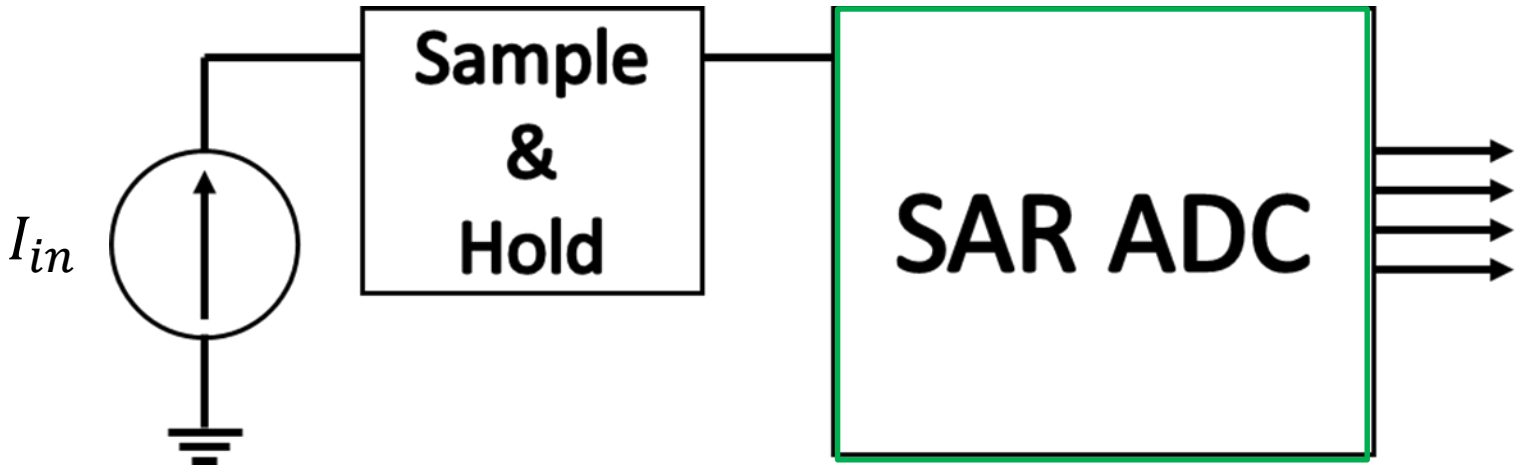
Settling Time

Large

Binary type
or
Redundant type

SAR: Successive Approximation Register

Our Approach



SAR Algorithm

Binary type → Redundant type

Each step time can be shorter

↓

Possibility of Measurement time reduction

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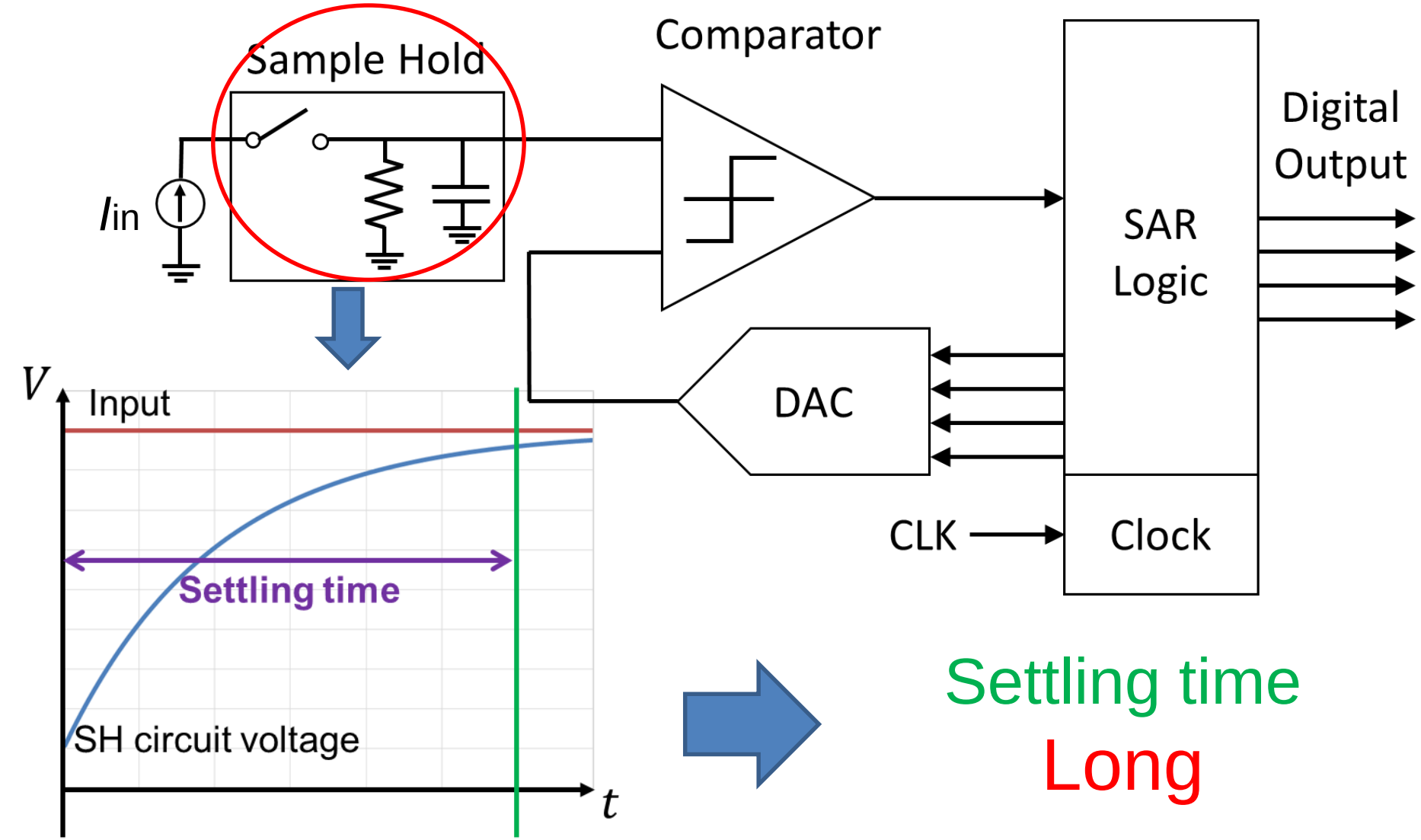
Problem of Minute Current Measurement

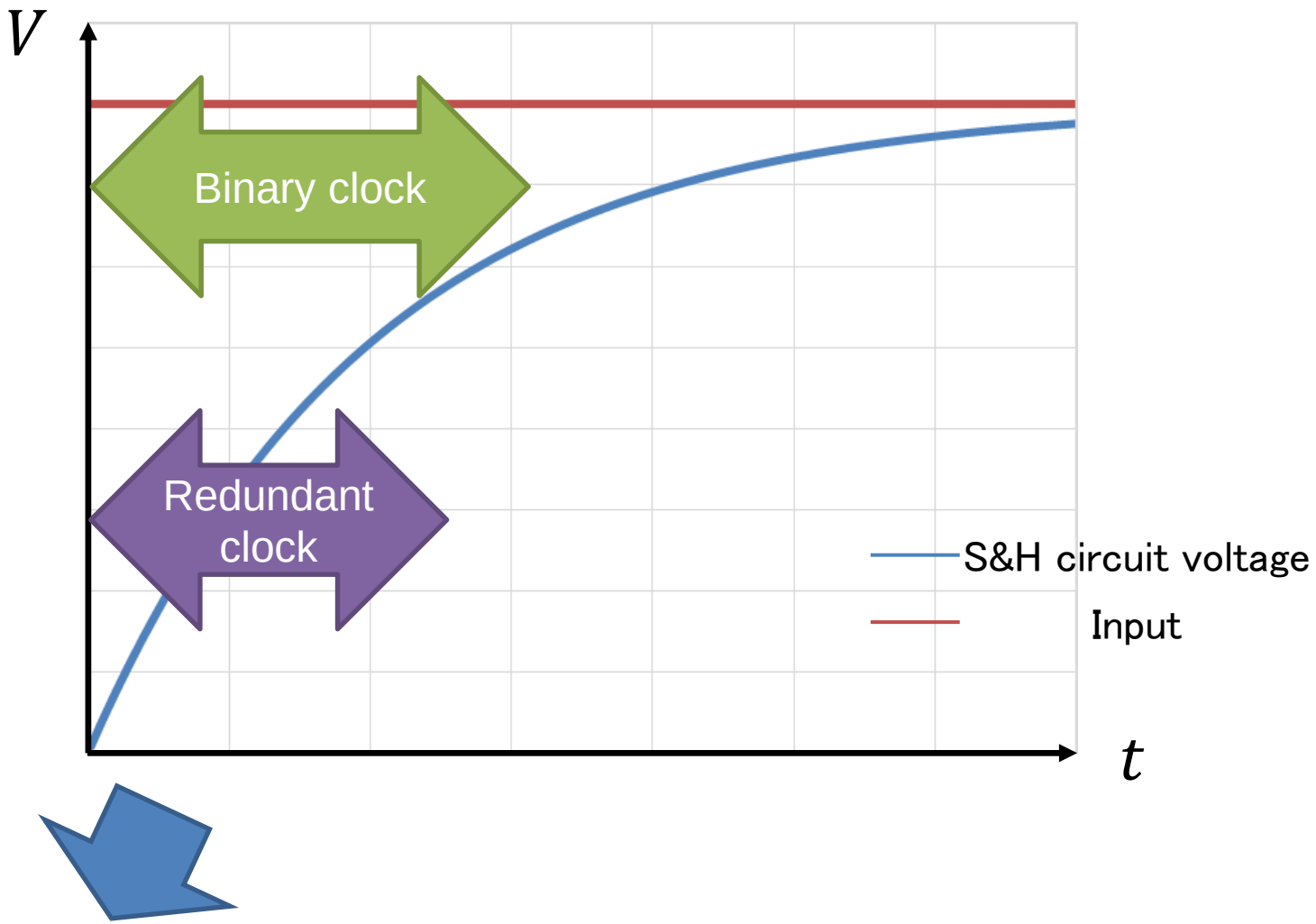
Using SAR ADC



Settling time

Long

Solution



Reduction each step measurement time ⇒ Increase measurement speed

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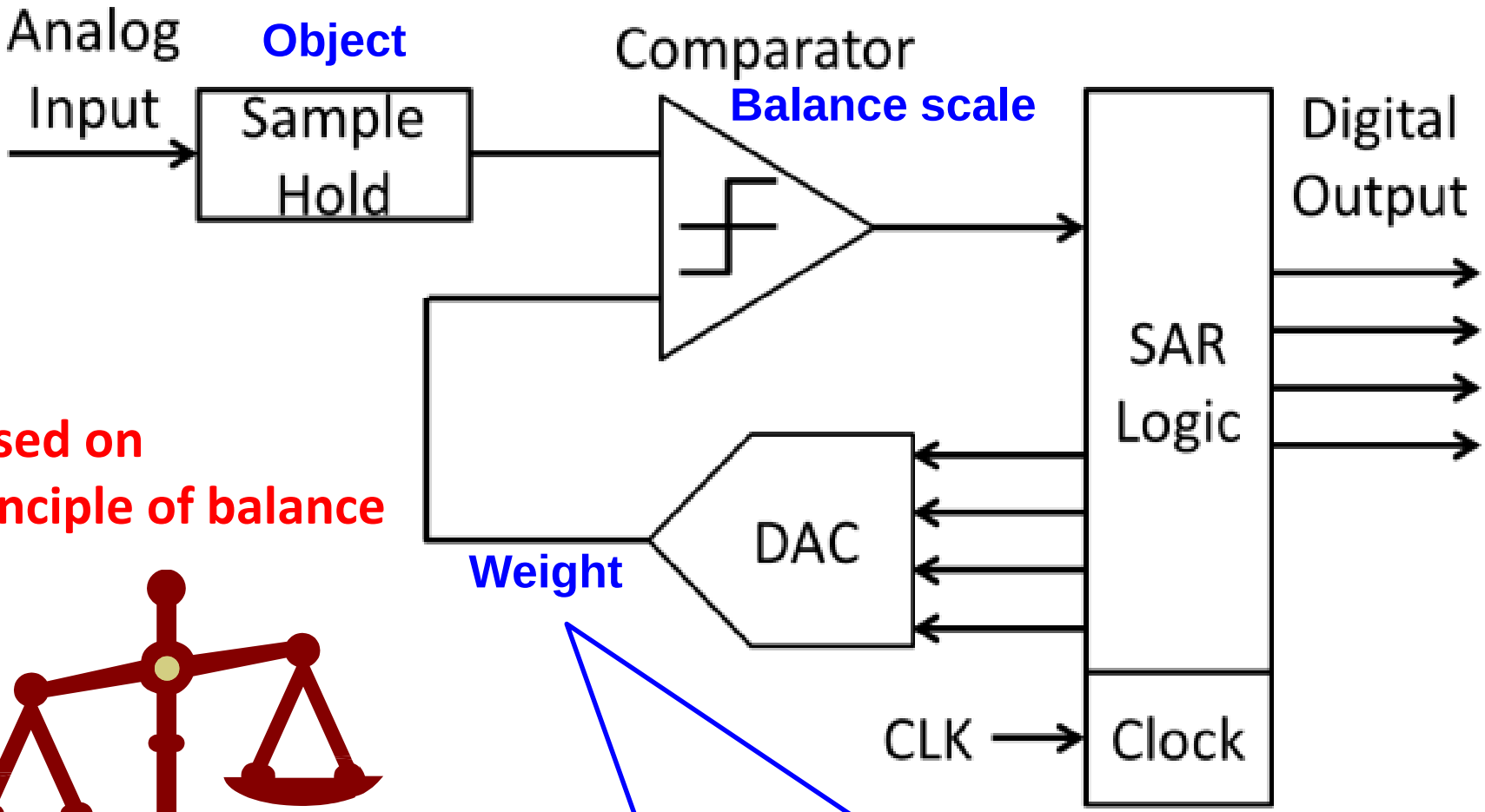
SAR ADC Configuration



Based on principle of balance

Generally use binary weight

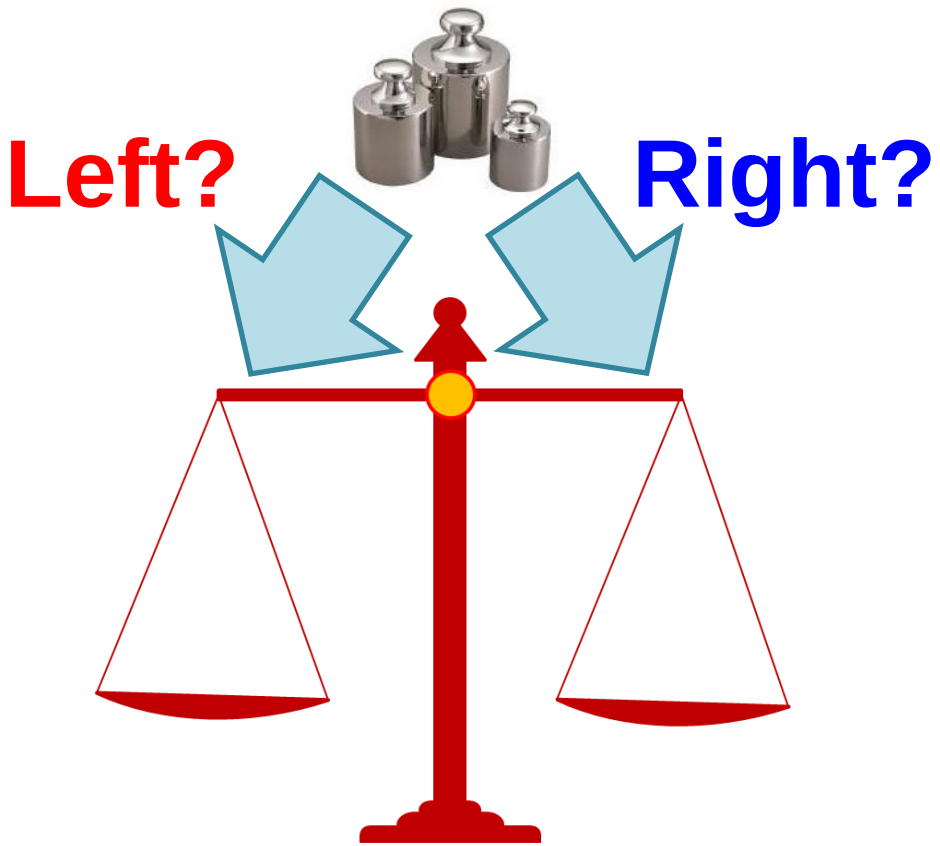
(1 , 2 , 4 , 8 , 16 , 32, 64 …)

Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input：7.3 [V]
- Binary weight :

16, 8, 4, 2, 1



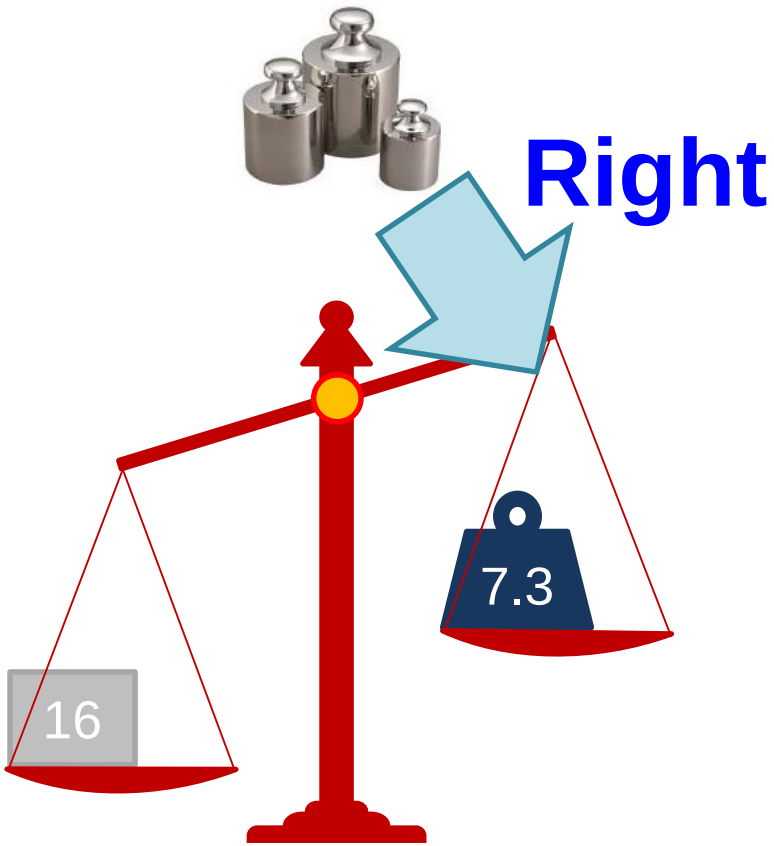
Step		1st	2nd	3rd	4th	5th	output
Weight p(k)		16	8	4	2	1	
Level	31						31
	30						30
	29						29
	28						28
	27						27
	26						26
	25						25
	24						24
	23						23
	22						22
	21						21
	20						20
	19						19
	18						18
	17						17
	16						16
	15						15
	14						14
	13						13
	12						12
	11						11
	10						10
	9						9
	8						8
	7						7
	6						6
	5						5
	4						4
	3						3
	2						2
	1						1
	0						0

Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input：7.3 [V]
- Binary weight :

8, 4, 2, 1



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	21						21
	20						20
	19						19
	18						18
	17						17
	16						16
	15						15
	14						14
	13						13
	12						12
	11						11
	10						10
	9						9
	8						8
	7						7
	6						6
	5						5
	4						4
	3						3
	2						2
	1						1
	0						0

Down!

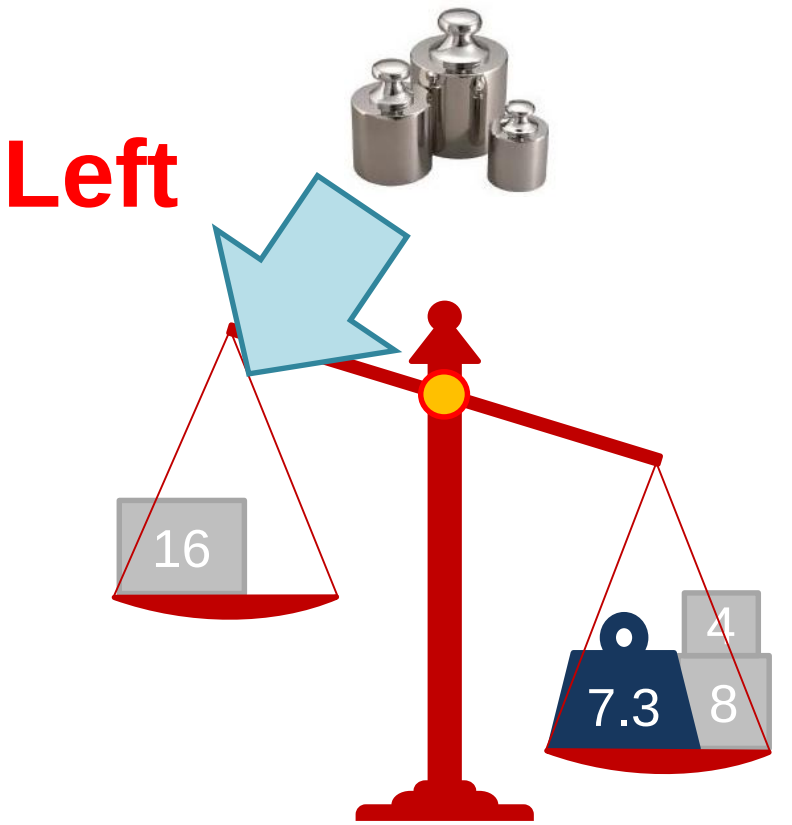
0

Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input：7.3 [V]
- Binary weight :

2, 1



Step		1st	2nd	3rd	4th	5th	output
Weight p(k)		16	8	4	2	1	
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	20						20
	19						19
	18						18
	17						17
	16						16
	15						15
	14						14
	13						13
	12						12
	11						11
	10						10
	9						9
	8						8
	7						7
	6						6
	5						5
	4						4
	3						3
	2						2
	1						1
	0						0

UP!

0 0 1

Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input：7.3 [V]
- Binary weight :

7.3⇒00111⇒7

$16 - 8 - 4 + 2 + 1 + 0.5 - 0.5 = 7$

Step	1st	2nd	3rd	4th	5th	output
Weight p(k)	16	8	4	2	1	
Level 31						31
30						30
29						29
28						28
27						27
26						26
25						25
24						24
23						23
22						22
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19						19
18						18
17						17
16						16
15						15
14						14
13						13
12						12
11						11
10						10
9						9
8						8
7						7
6						6
5						5
4						4
3	0	0	1	1	1	3
2						2
1						1
0						0

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SAR ADC Redundancy Design

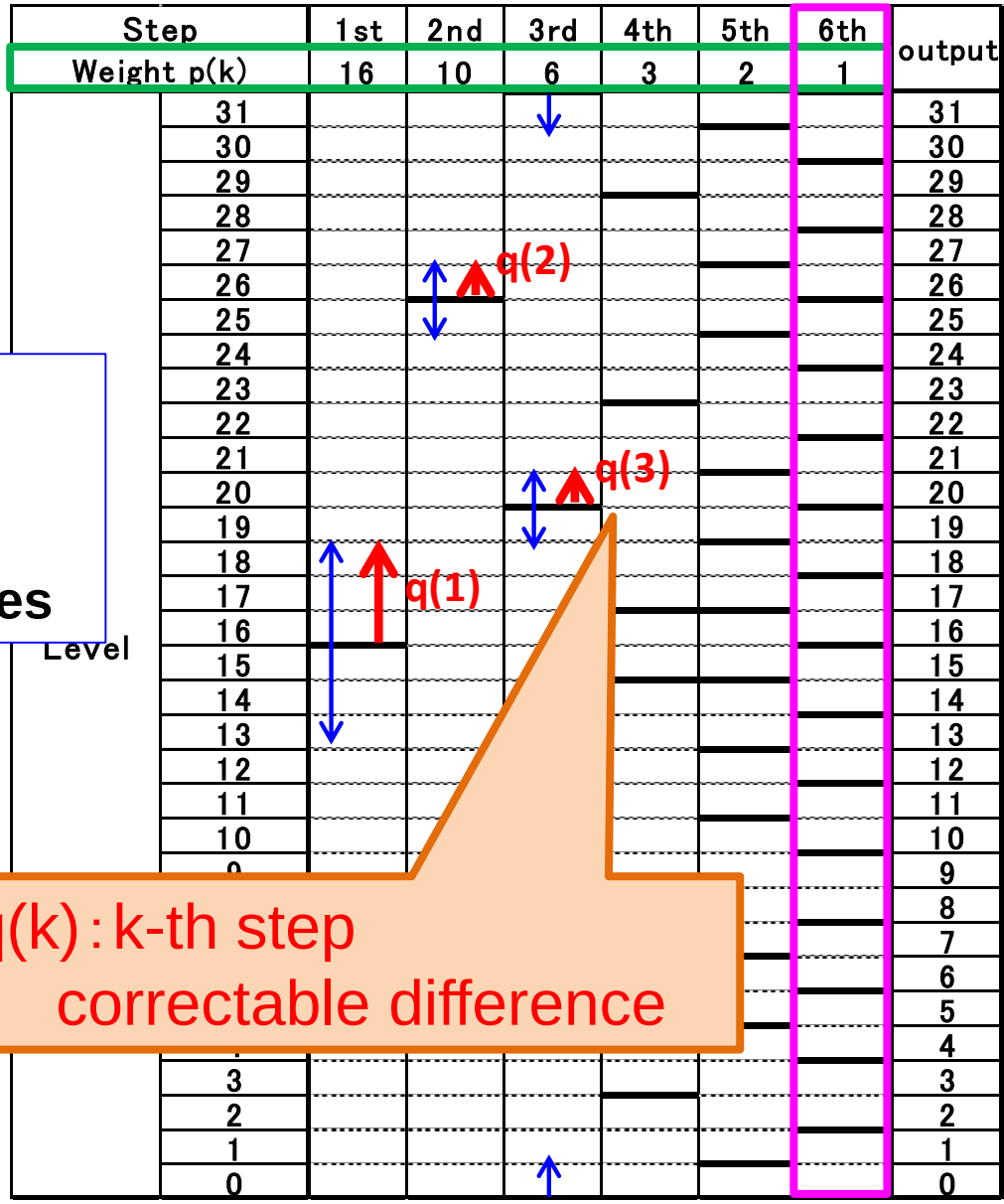
Redundancy

➡ Surplus, Extra

Using time redundancy

- **Extra comparison steps**
- **Change reference to Non-binary voltages**

Enable digital error correction!



Redundancy Design Operation(No Error)

4bit-5step SAR ADC

- Analog input : 6.3
- Redundant weight :

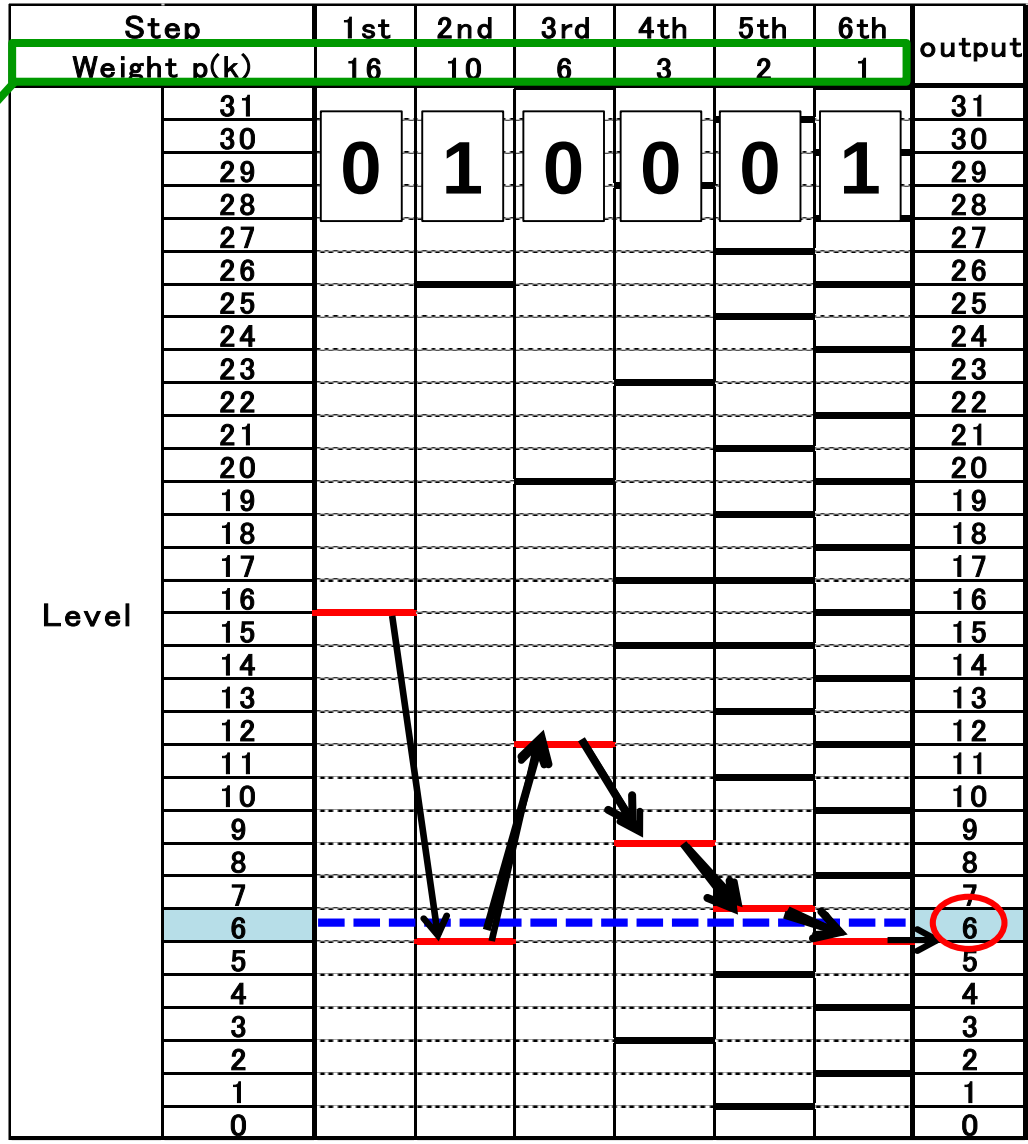
  16, 10, 6, 3, 2, 1

Correctable expression

6.3⇒010001⇒6

$$16 - 10 + 6 - 3 - 2 - 1 + 0.5 - 0.5$$

=6



Redundancy Design Operation(One Error)

4bit-5step SAR ADC

- Analog input：6.3
- Redundant weight :

  16, 10, 6, 3, 2, 1

Correctable expression

6.3⇒010001⇒6

Another expression

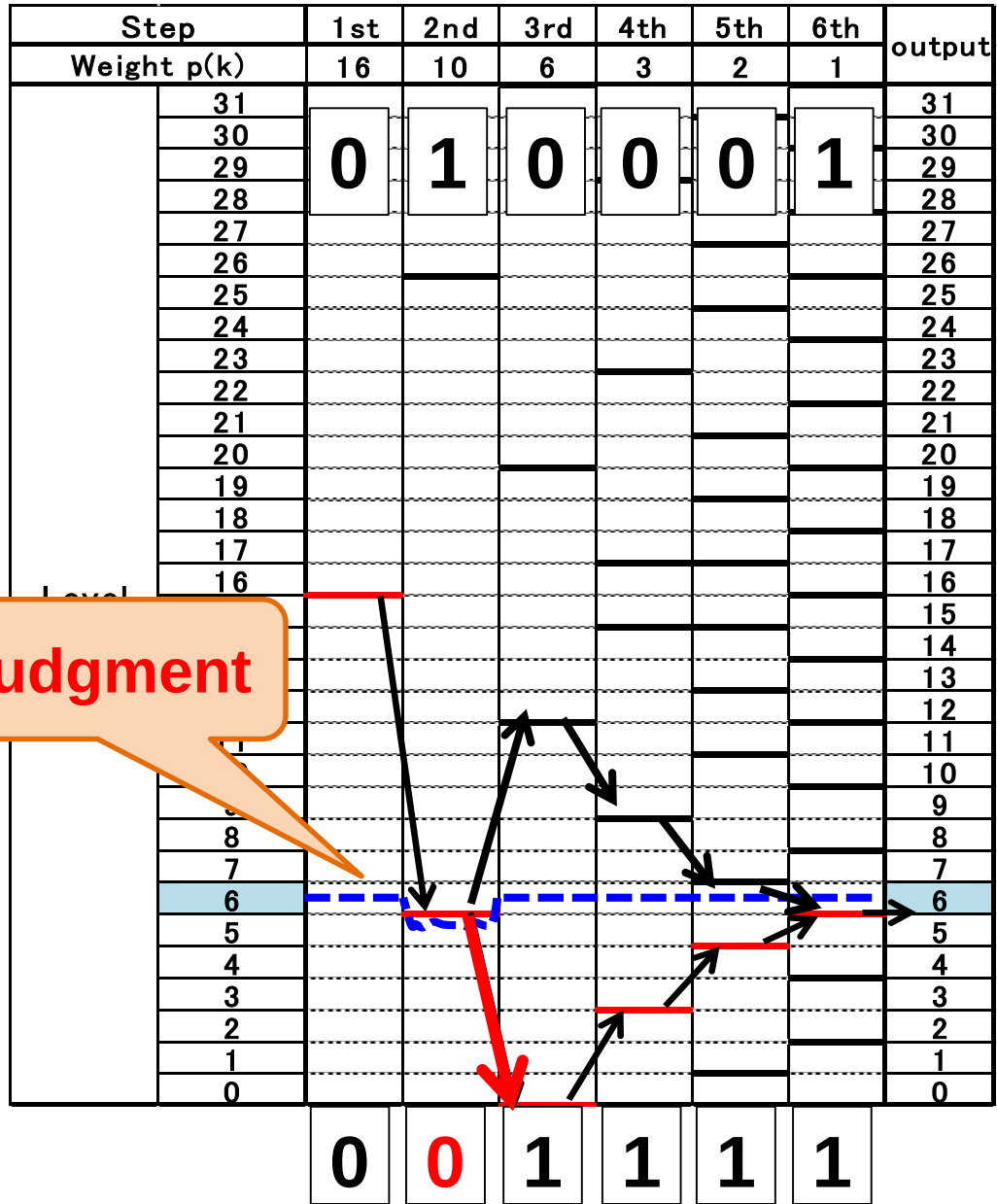
6.3⇒001111⇒6

$16 - 10 - 6 + 3 + 2 + 1 + 0.5 - 0.5$

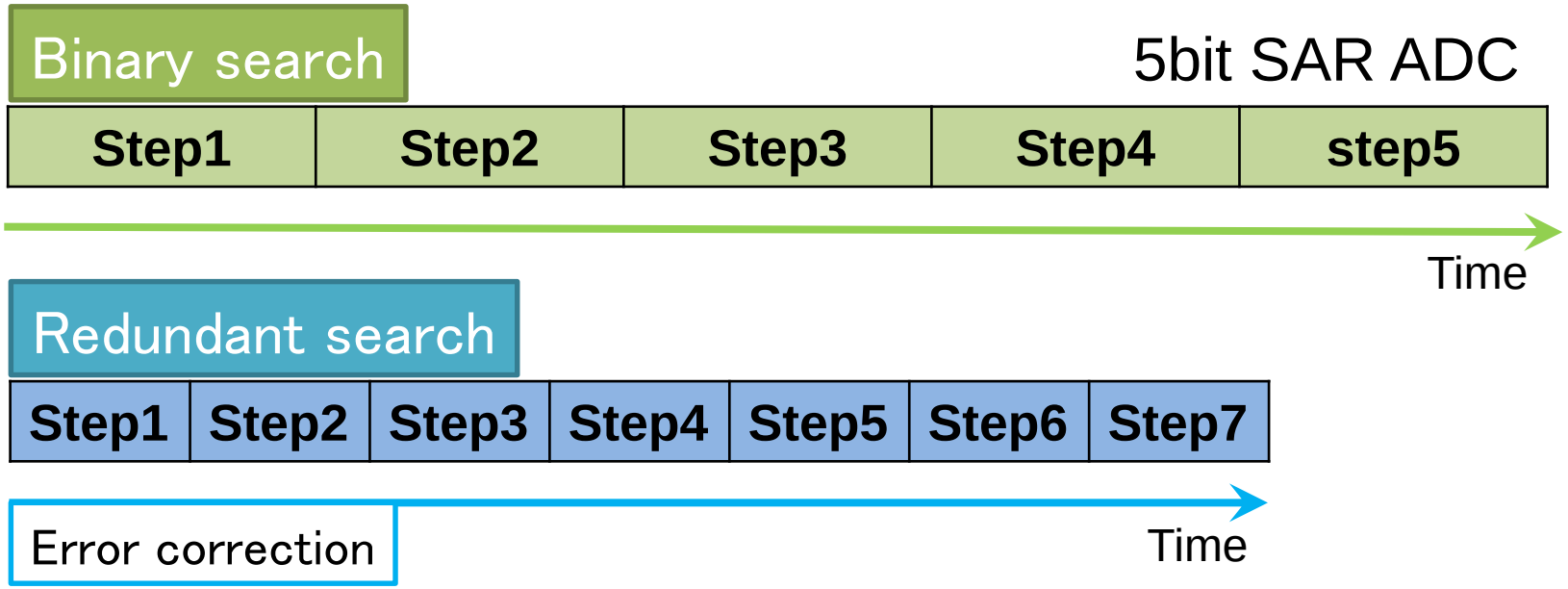
$= 6$

Error correction

High-Reliability



Redundant Search SAR ADC Speed



Early steps: relaxing comparative condition
→ increase ADC speed
Later steps: correct misjudgment

Each step time is shortened → ADC speed increases

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Fibonacci Sequence

Definition (n=0,1,2,3...)

$$F_0 = 0$$
$$F_1 = 1$$
$$F_{n+2} = F_n + F_{n+1}$$

Fibonacci number

$$0, 1, 1, \mathbf{2}, 3, 5, \mathbf{8}, 13, 21, 34, \mathbf{55} \ldots$$

Property

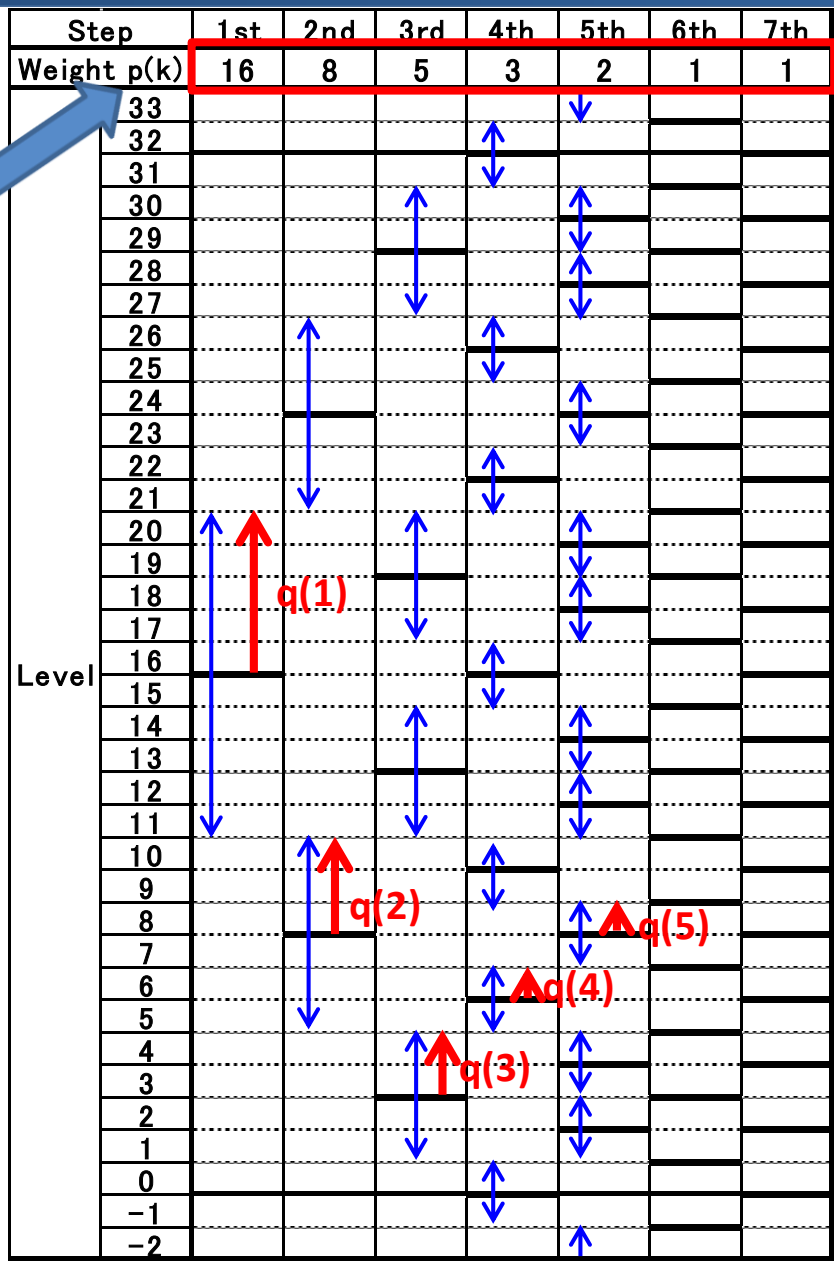
The closest terms ratio converges to *"Golden Ratio"* !

$$\lim_{n\to\infty} \frac{F_n}{F_{n-1}} = 1.6180339887 \ldots = \phi$$

Fibonacci Sequence Weighted SAR ADC

Fibonacci sequence SAR ADC

Weight is Fibonacci sequence



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Proof Content

We consider settling time of Sample & Hold circuit

Measurement time

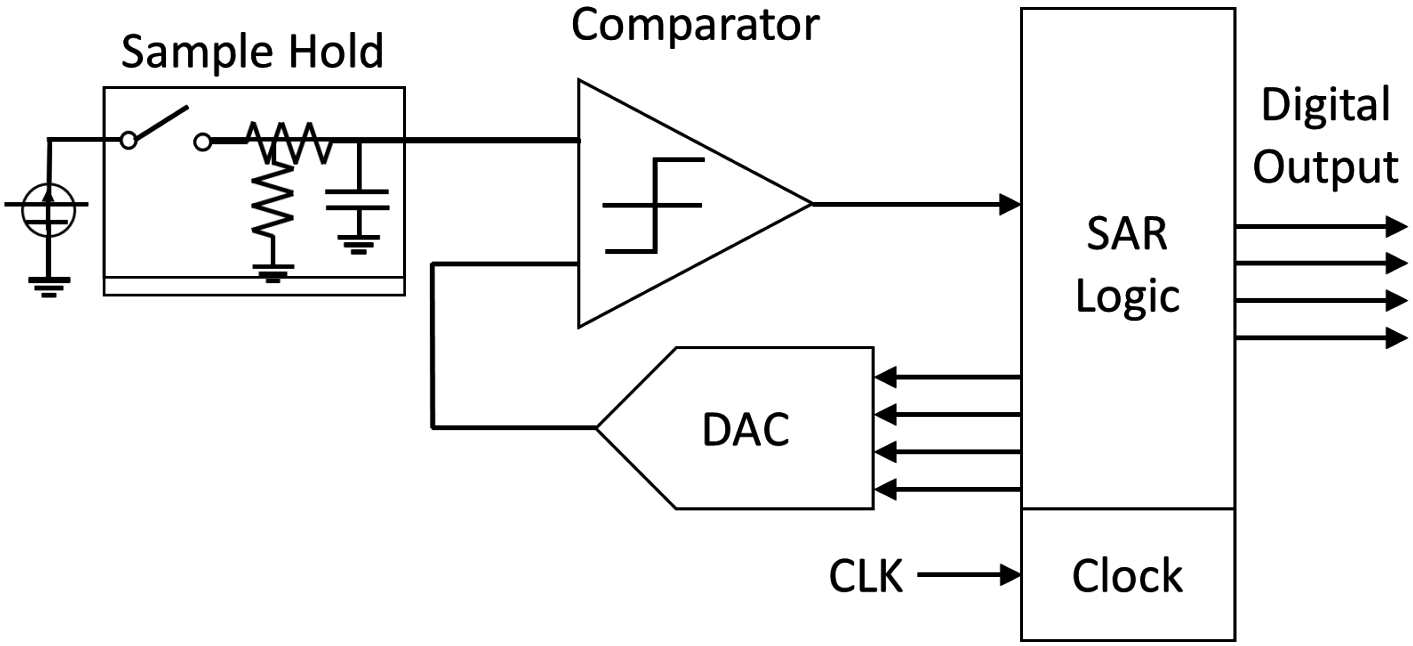
Binary type SAR ADC

V

Fibonacci type SAR ADC

Simulation Conditions(1/2)

- Input signal : Current source⇒Voltage source
- Consider settling time of Sample & Hold circuit



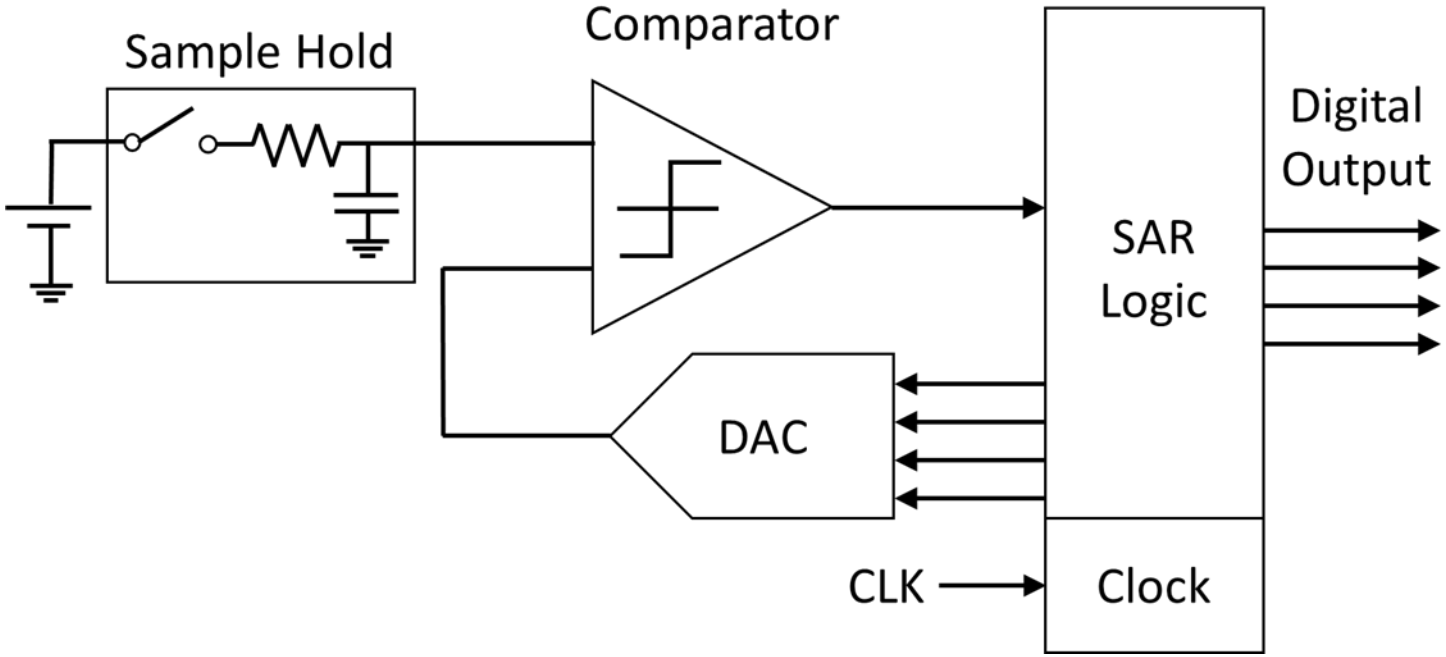
Simulation Conditions(2/2)

Simulation with scilab

Resolution：1～14bit

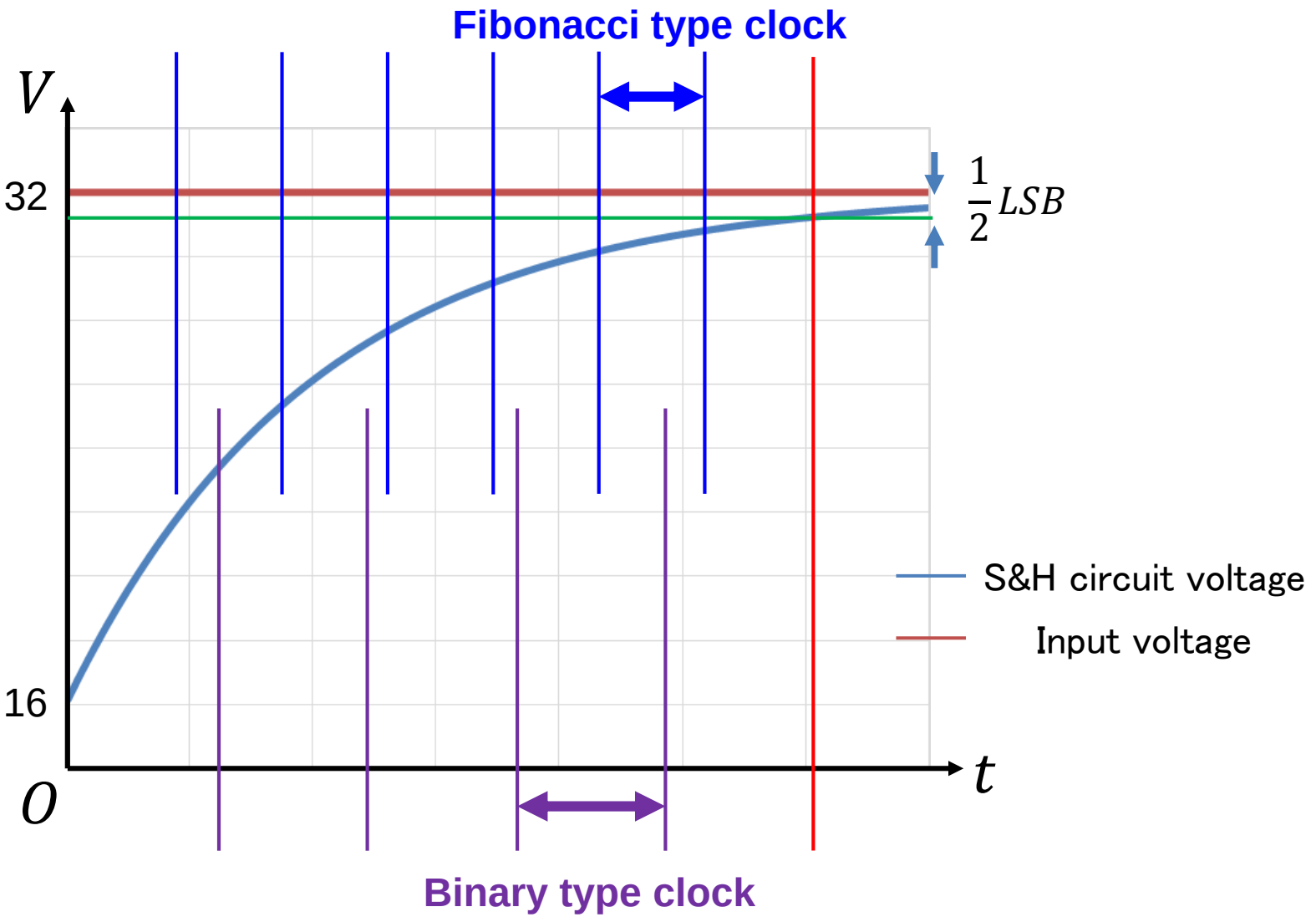
Accuracy　：$\frac{1}{2}$LSB

Initial voltage of capacitor：Half of full scale



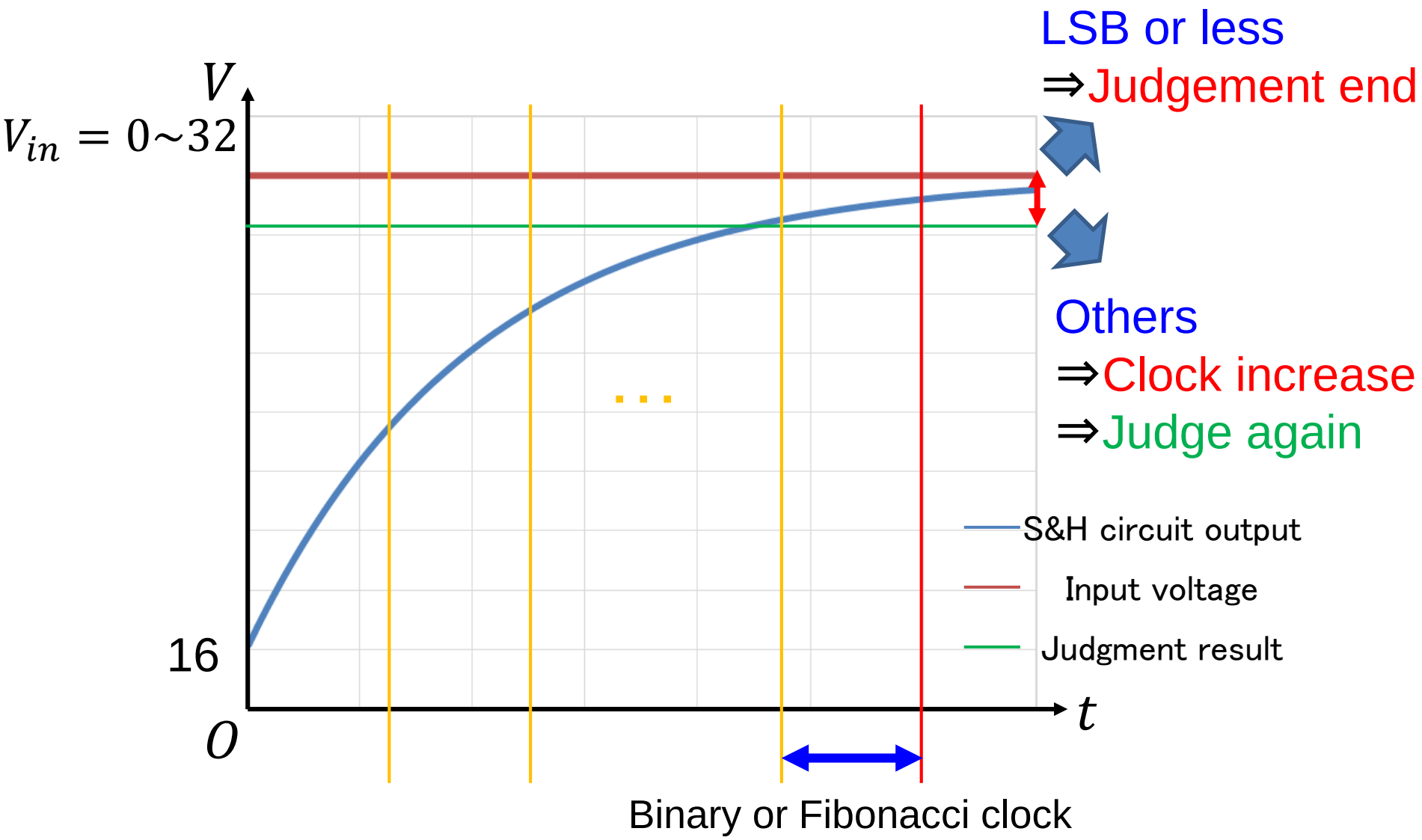
Simulation Method(1/3)

Clock generation from worst case(Ex.5 bit)



Simulation Method(2/3)

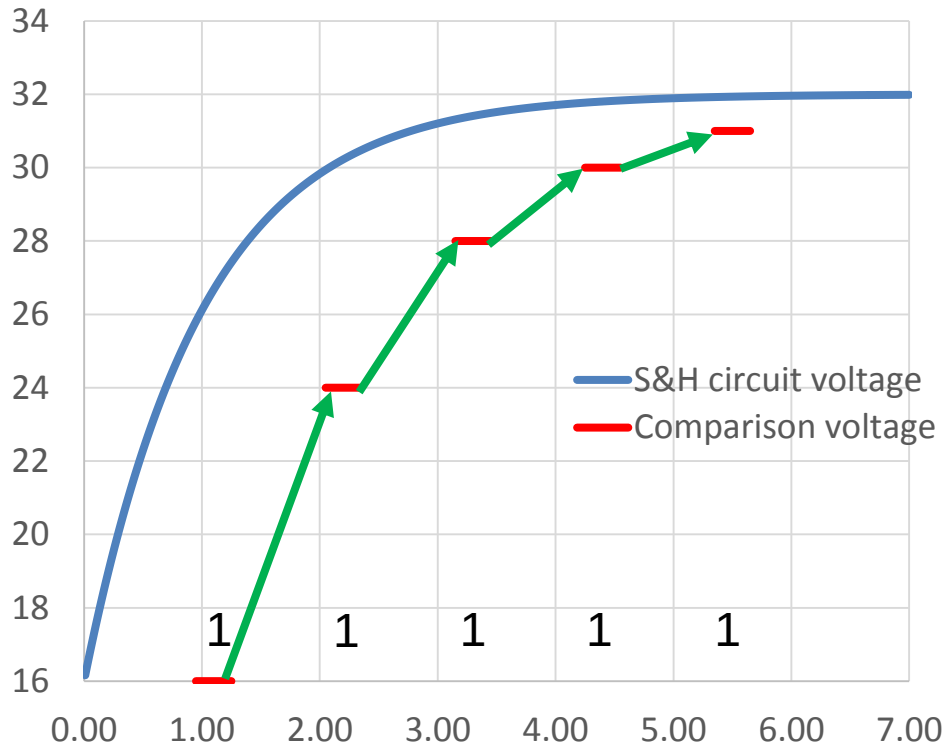
Judgment / Change(Binary & Fibonacci)



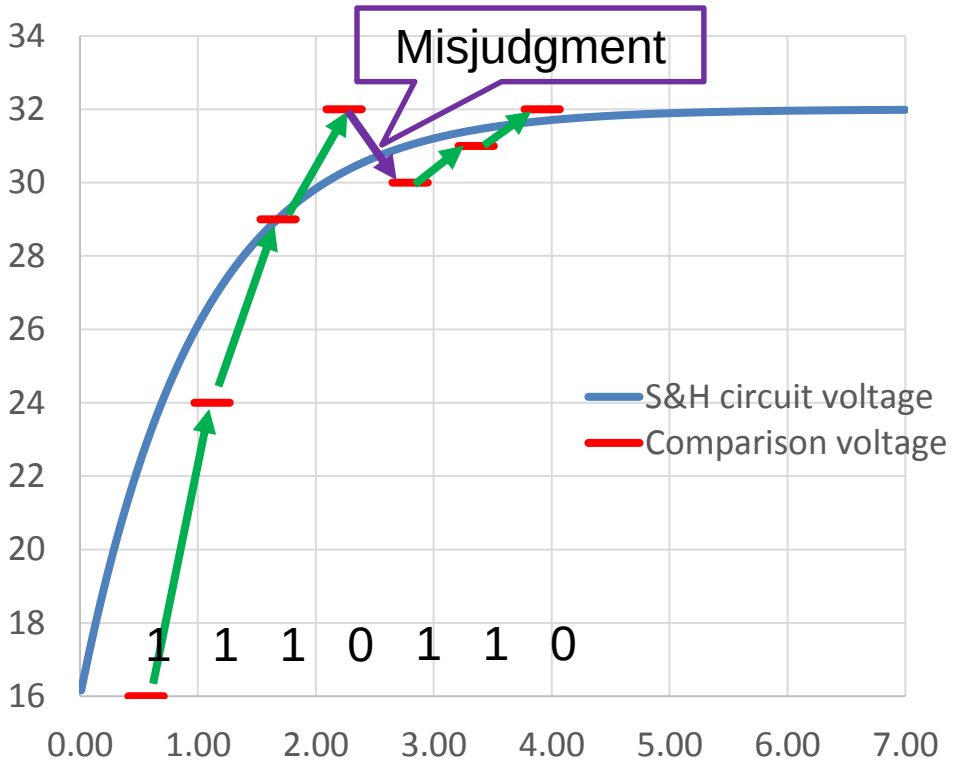
Determination Example(1/3)

When $V_{in} = 32$

Binary type



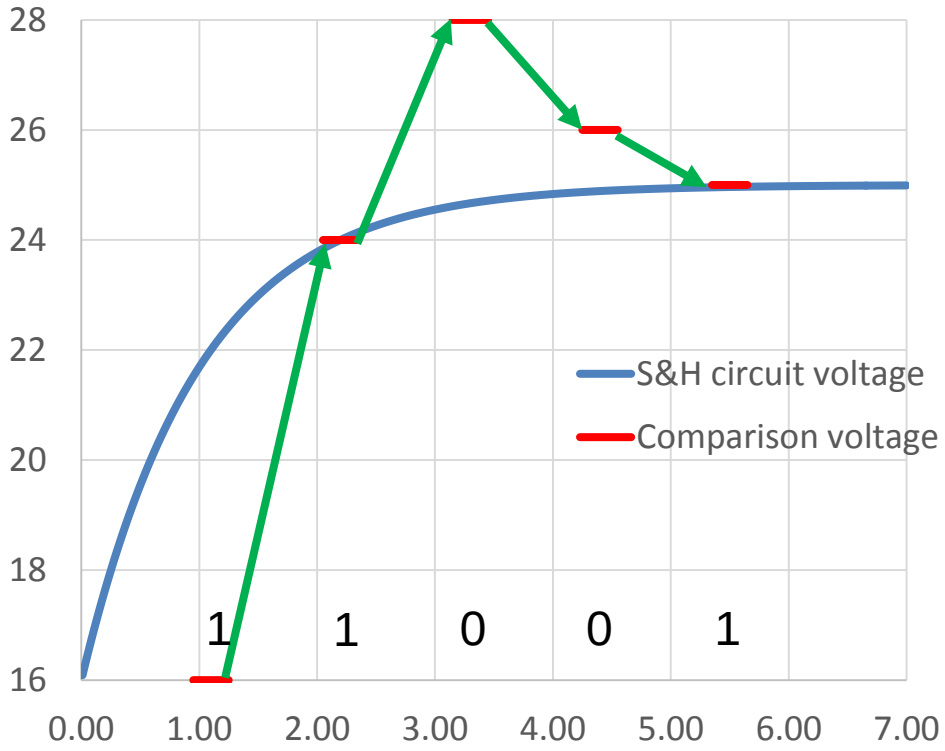
Fibonacci type



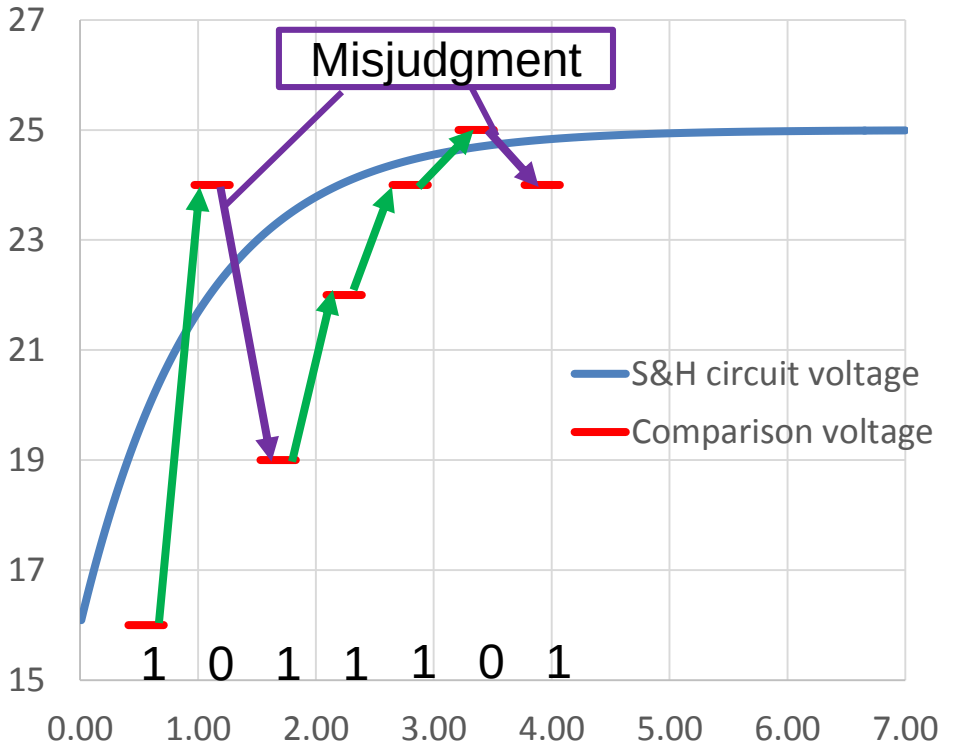
Determination Example(2/3)

When $V_{in} = 25$

Binary type



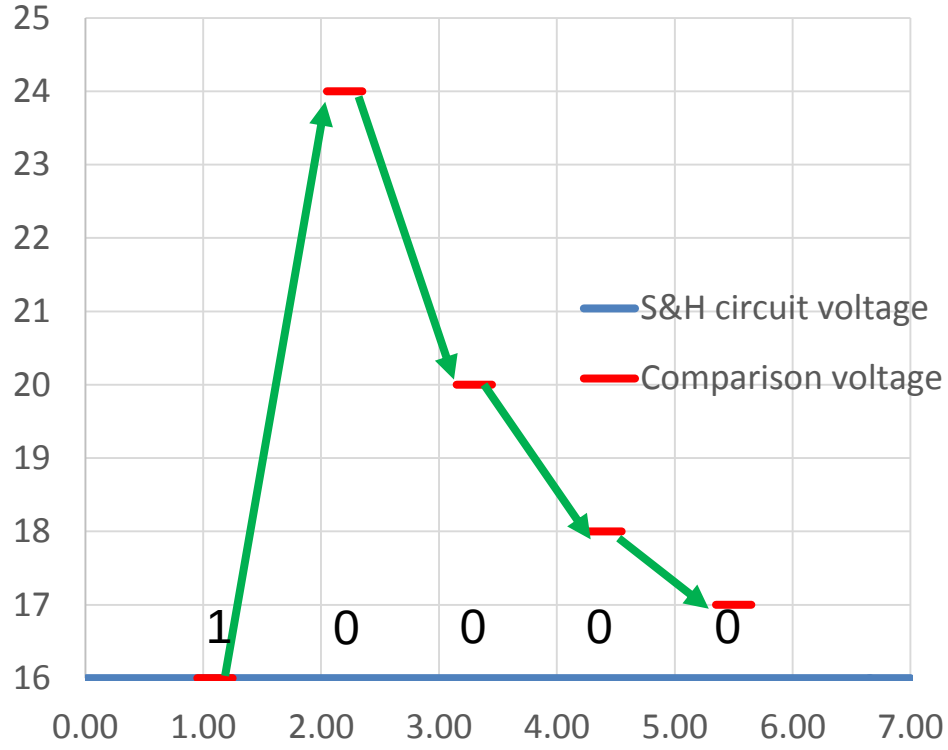
Fibonacci type



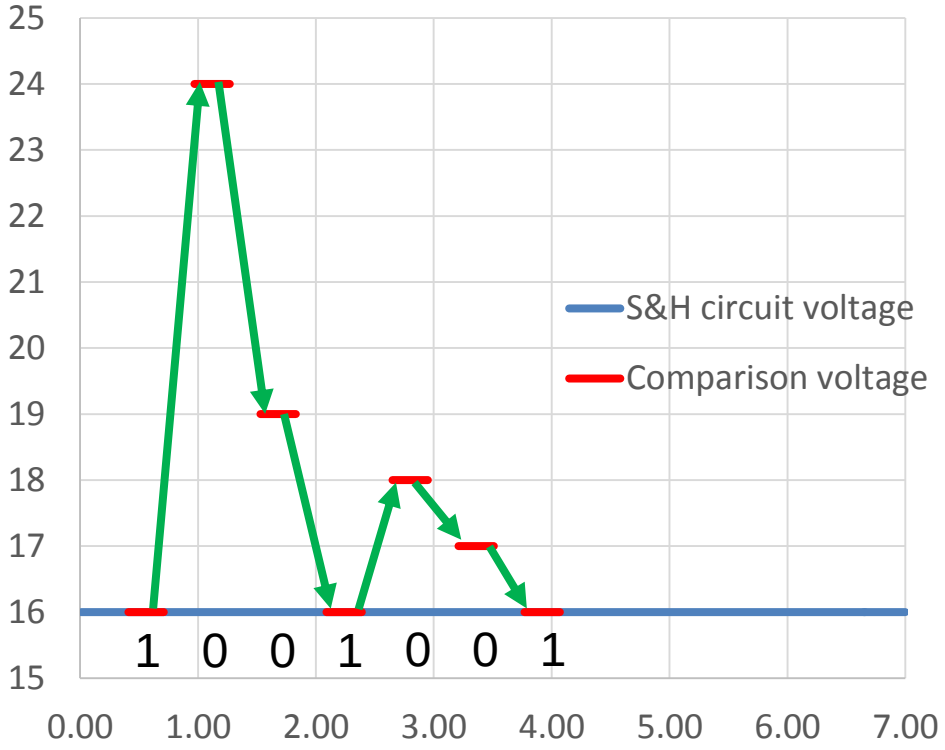
Determination Example(3/3)

When $V_{in} = 16$

Binary type

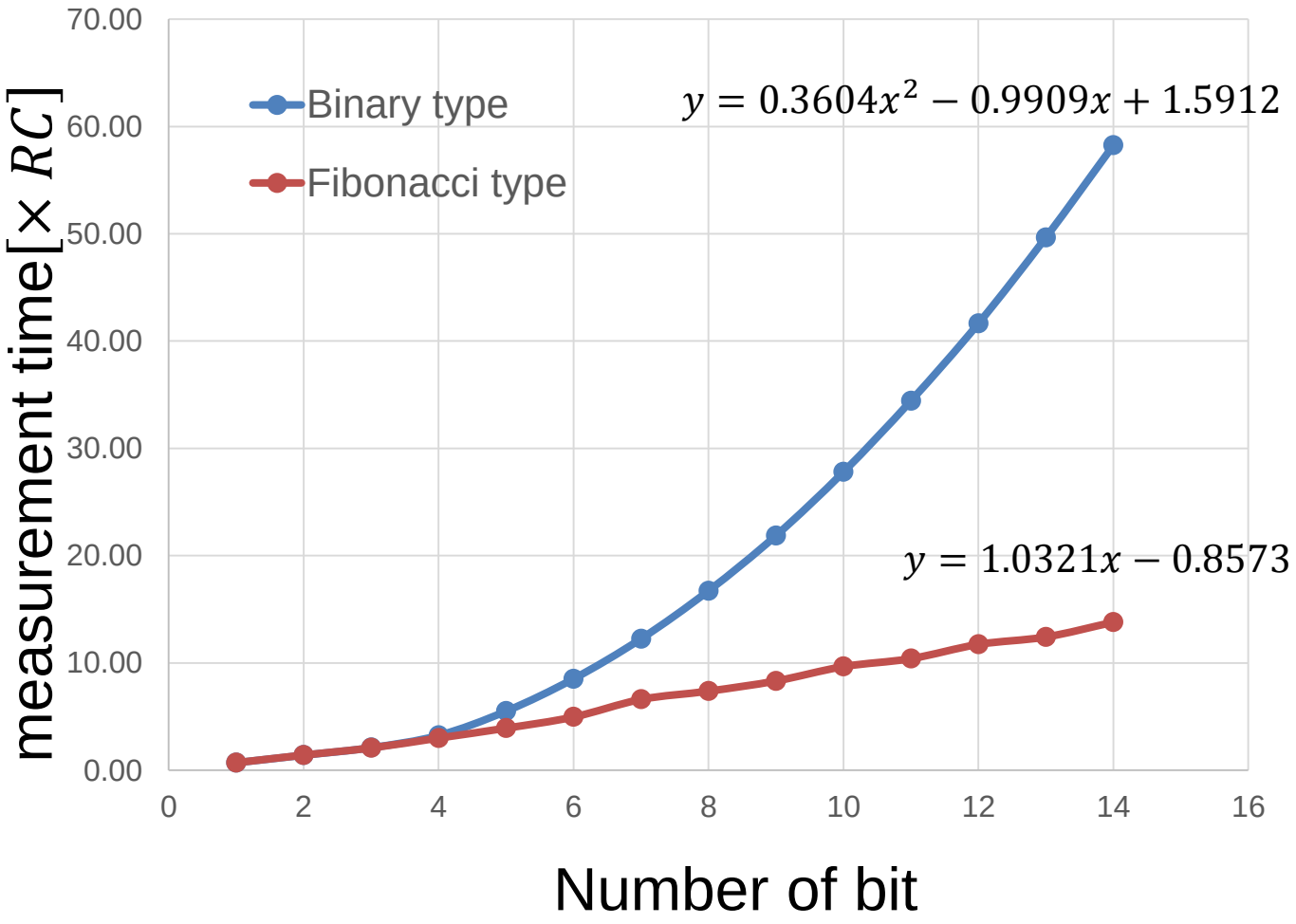


Fibonacci type



Simulation Results

Relationship number of bits & measurement time



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Conclusion

Minute current measurement using SAR ADC

→ Consider settling time of sample & hold circuit

- Binary type(Redundancy: ) :Complete settling
- Fibonacci type(Redundancy: ) : Incomplete settling

→ Reduction of each step measurement time

↓

Measurement time

Binary SAR ADC > Fibonacci SAR ADC

Thank you for listening

Golden Ratio