Linearity Improvement Algorithms of Multi-bit ΔΣ DA Converter –DWA, Self-Calibration and Their Combination

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Research Objective

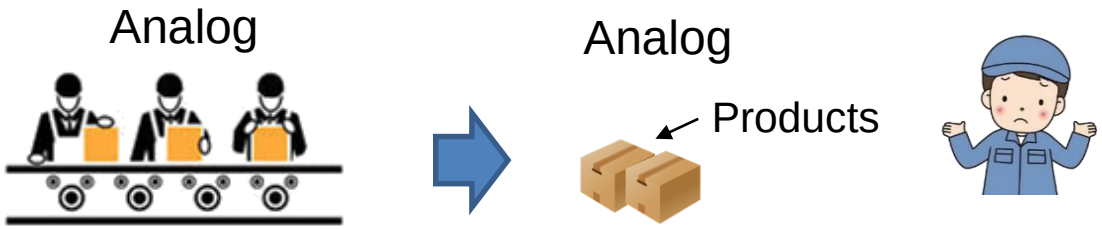
Objective

- **Linearity improvement of Multi-bit ΔΣ DAC for analog signal generation**

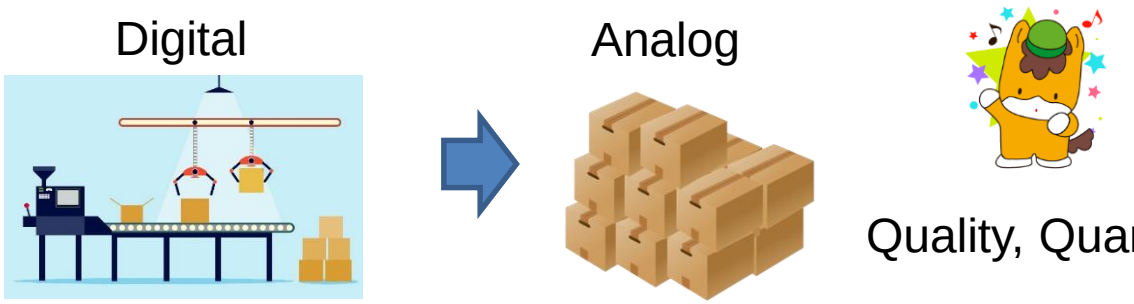
Approach

- **Digital signal techniques using DWA & self-calibration**

Conventional …



Proposed !!



Quality, Quantity is great

Outline

- Research Background
- DWA* Algorithm (* Data-Weighted Averaging)
- Self-Calibration Algorithm
- Simulation Configuration & Results
- New finding for HP ΔΣ DAC
- Conclusion

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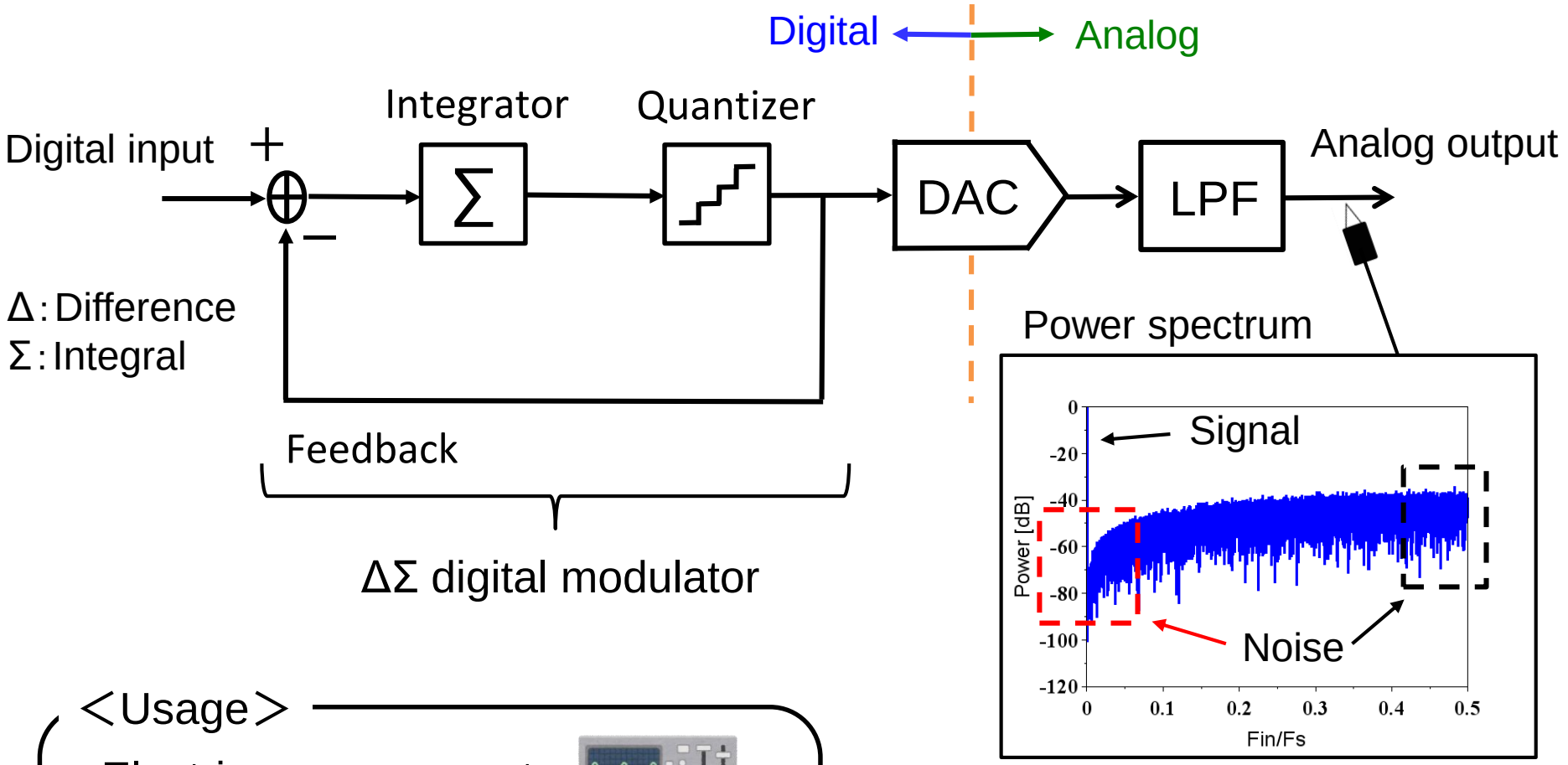
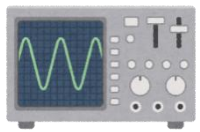
ΔΣ DA Converter (LP model)



＜Usage＞

- Electric measurement

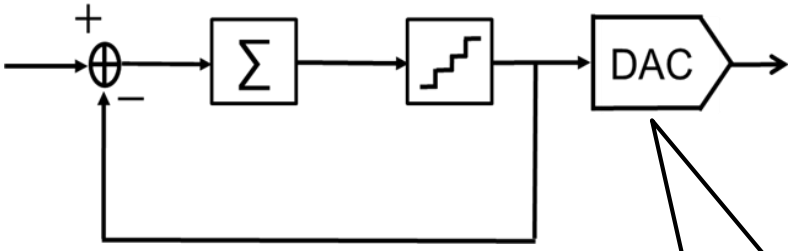


- Audio system

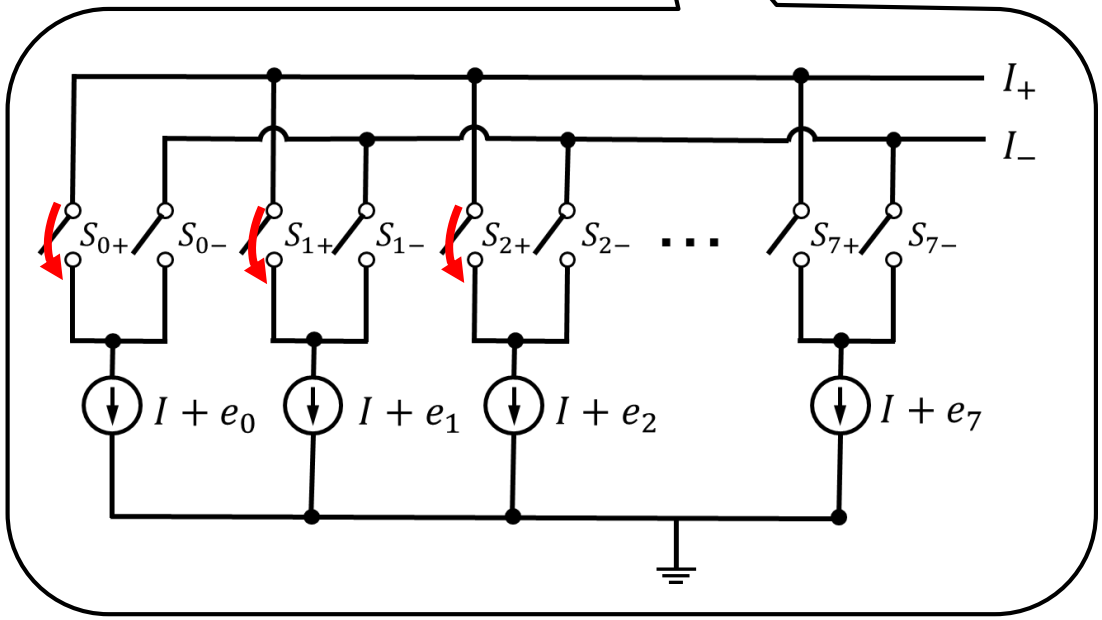
Noise is decreased at low frequency
increased at high frequency

Multi-bit DAC Operation (1/3)

DAC input digital = +3



$$I_{out} = I_+ - I_-$$
$$= +3 \times I + (e_0 + e_1 + e_2)$$ Positive current



Digital	I_{out}
+3	$+3 \times I + (e_0 + e_1 + e_2)$
0	
-2	

Current $I_k = I + e_i$

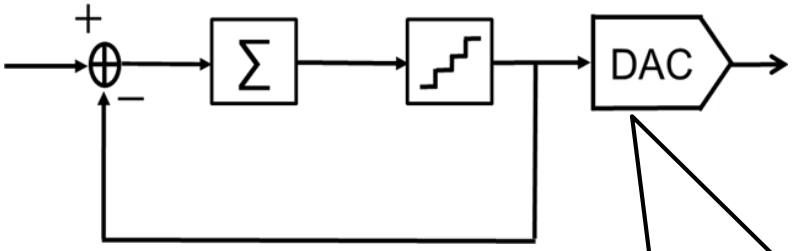
e_i : Current source mismatches

✓ We consider “Ternary” case ⇒ positive, zero, negative

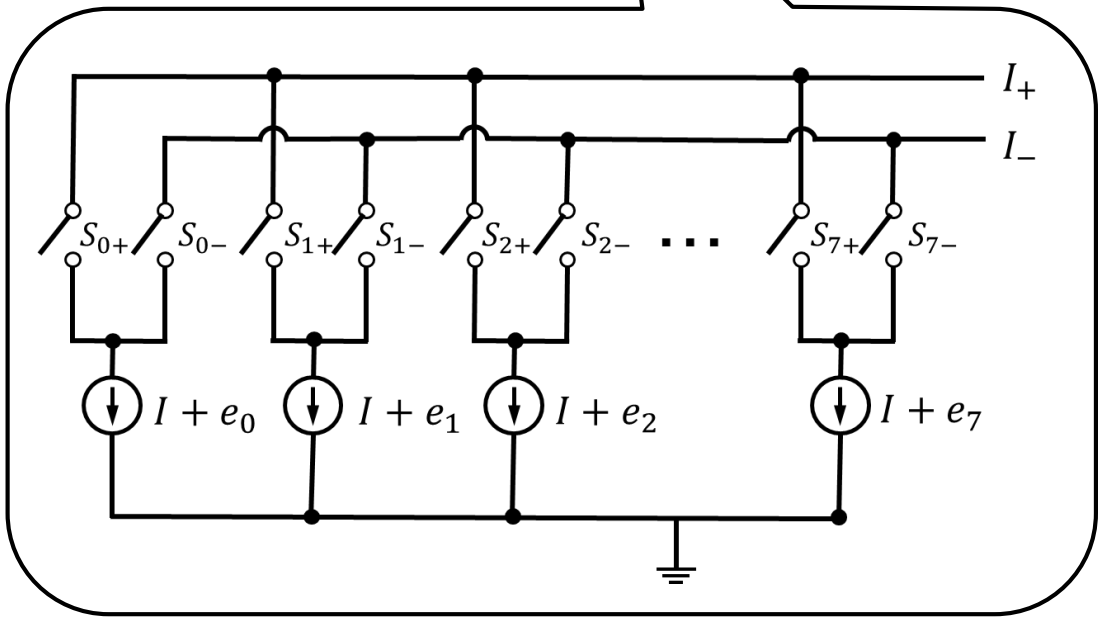
(※ Binary case ⇒ positive, zero)

Multi-bit DAC Operation (2/3)

DAC input digital = 0



$$I_{out} = I_+ - I_- = 0$$ Zero current



Digital	I_{out}
+3	$+3 \times I + (e_0 + e_1 + e_2)$
0	0
-2	

Current $I_k = I + e_i$

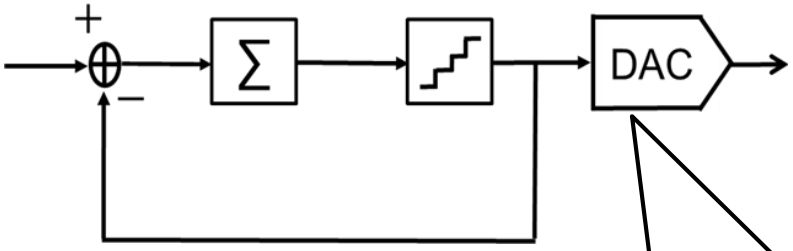
e_i : Current source mismatches

✓ We consider "Ternary" case ⇒ positive, zero, negative

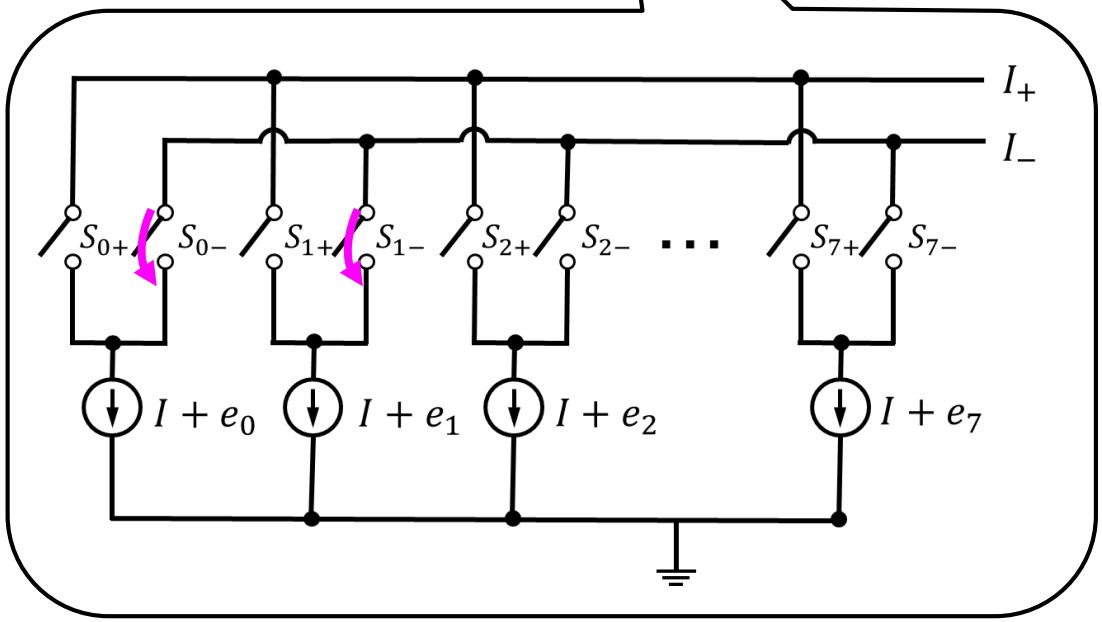
(※ Binary case ⇒ positive, zero)

Multi-bit DAC Operation (3/3)

DAC input digital = −2



$$I_{out} = I_+ - I_-$$
$$= -[2 \times I + (e_0 + e_1)]$$ Negative current



Digital	I_{out}
+3	$+3 \times I + (e_0 + e_1 + e_2)$
0	0
-2	$-[2 \times I + (e_0 + e_1)]$

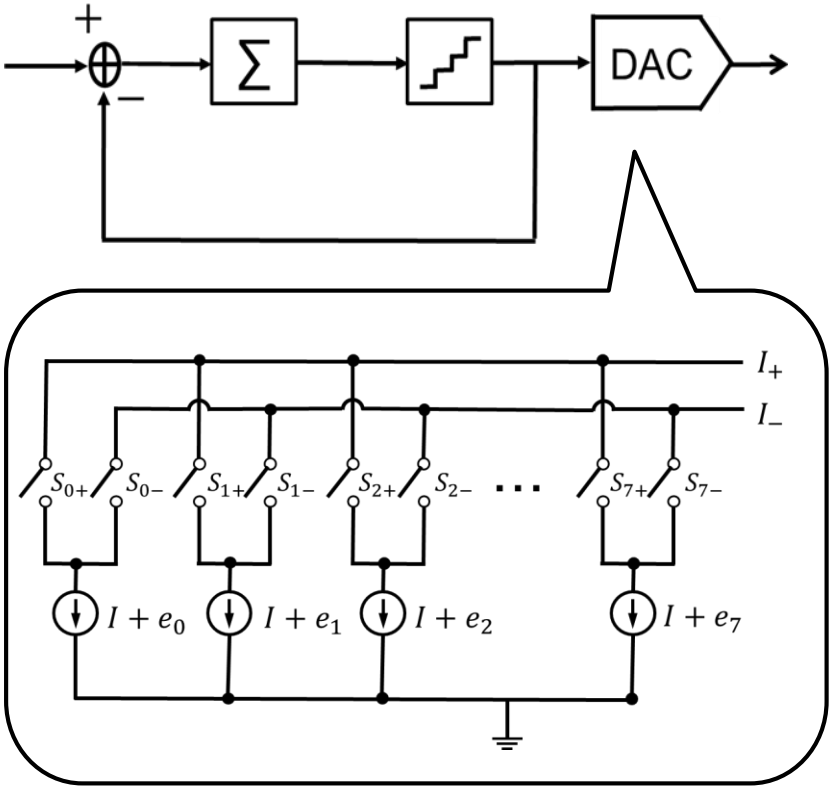
Current $I_k = I + e_i$

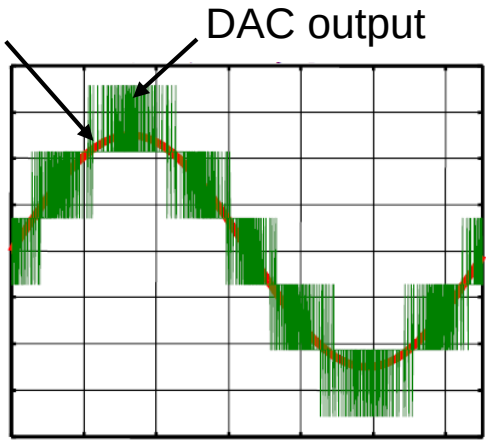
e_i : Current source mismatches

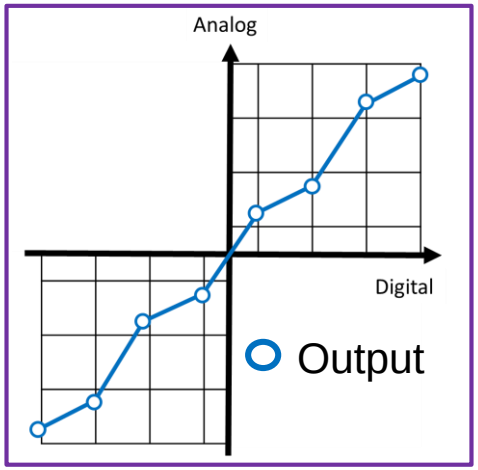
✓ We consider "Ternary" case ⇒ positive, zero, negative

(※ Binary case ⇒ positive, zero)

Nonlinearity Problem of Multi-bit ΔΣ DAC







Merit

- Quantization error suppression
- Relax following filter requirement

Nonlinearity Problem

Currents are Difference for process variation inside IC chip

Current $I_k = I + e_i$

e_i : Current source mismatches

Objective is linearity improvement

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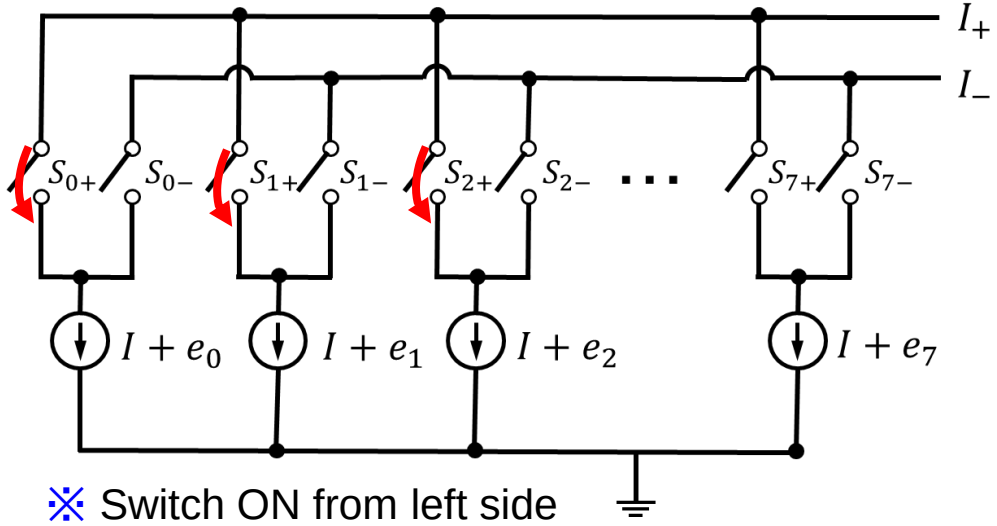
Multi-bit DAC (1/2)

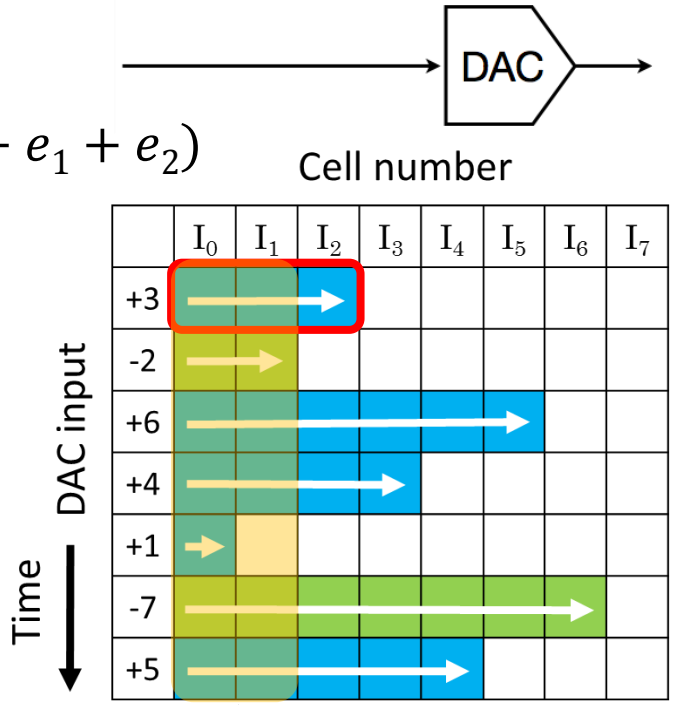
◆ Conventional segmented DAC

DAC input = +3

$$I_{out} = I_+ - I_- = +3 \times I + (e_0 + e_1 + e_2)$$



※ Switch ON from left side



✓ Currents are different
due to process variation inside IC chip

Current $I_k = I + e_i$

e_i : Current source mismatches

Accumulate mismatch of particular cells

e_i

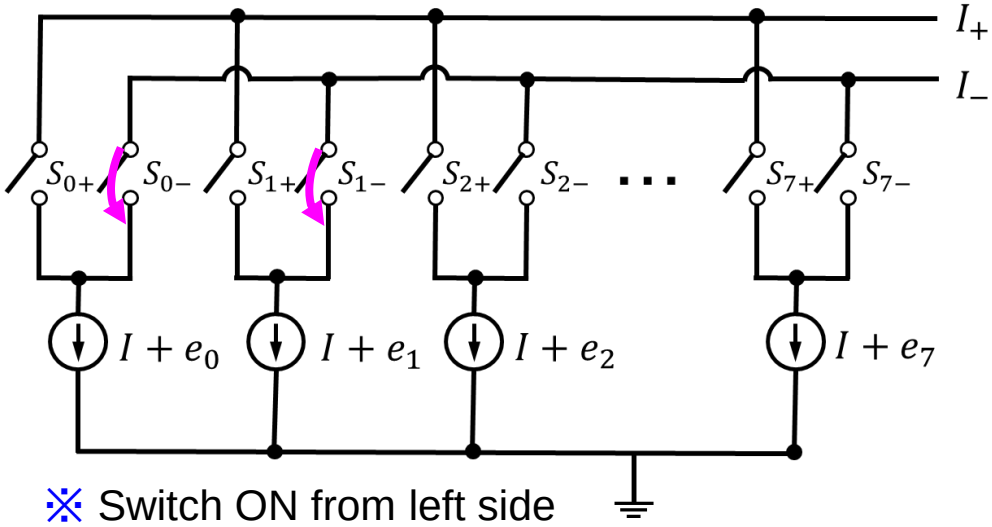
⇒ DAC Nonlinearity ☹

Multi-bit DAC (2/2)

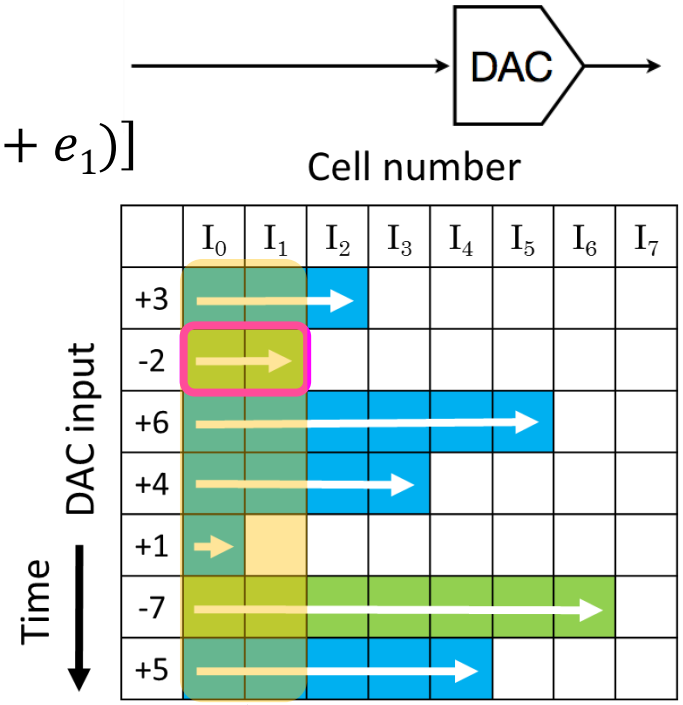
◆ Conventional segmented DAC

DAC input = -2

$$I_{out} = I_+ - I_- = -[2 \times I + (e_0 + e_1)]$$



※ Switch ON from left side



✓ Currents are different
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Current $I_k = I + e_i$

e_i : Current source mismatches

Accumulate mismatch of particular cells

e_i

⇒ DAC Nonlinearity ☹

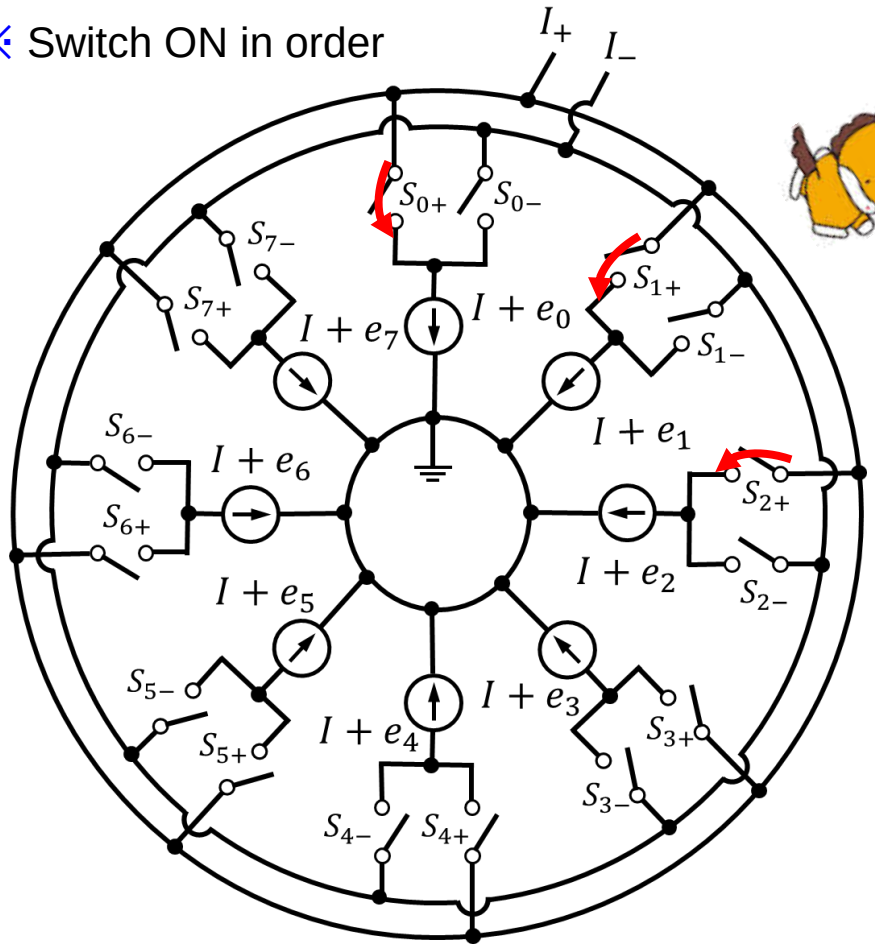
Multi-bit DAC + DWA (1/2)

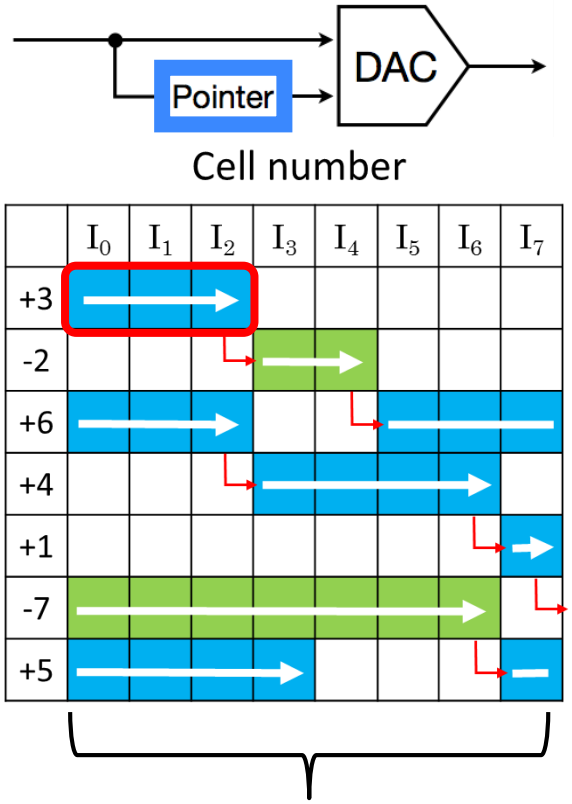
◆ DWA* DAC (*Data-Weighted Average)

DAC input = +3

$$I_{out} = I_+ - I_- = +3 \times I + (e_0 + e_1 + e_2)$$

※ Switch ON in order





Disperse mismatch of particular cells

⇒Time-averaged

⇒ Linearity improvement ☺

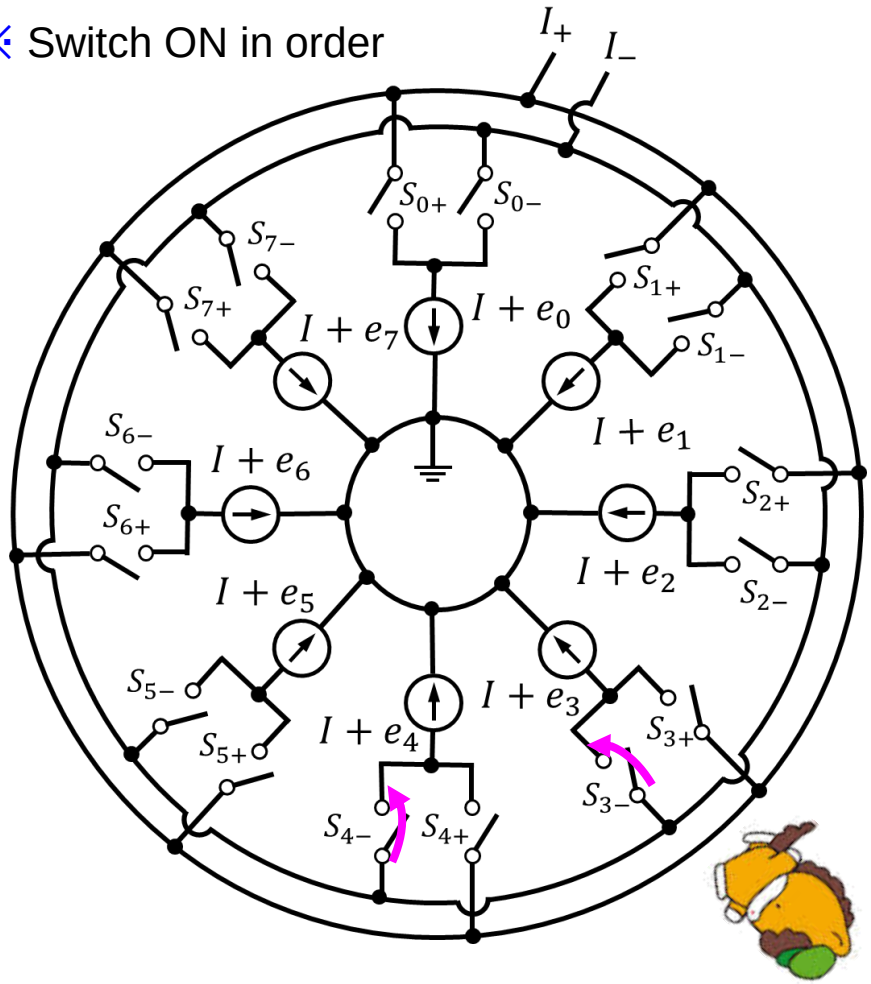
Multi-bit DAC + DWA (2/2)

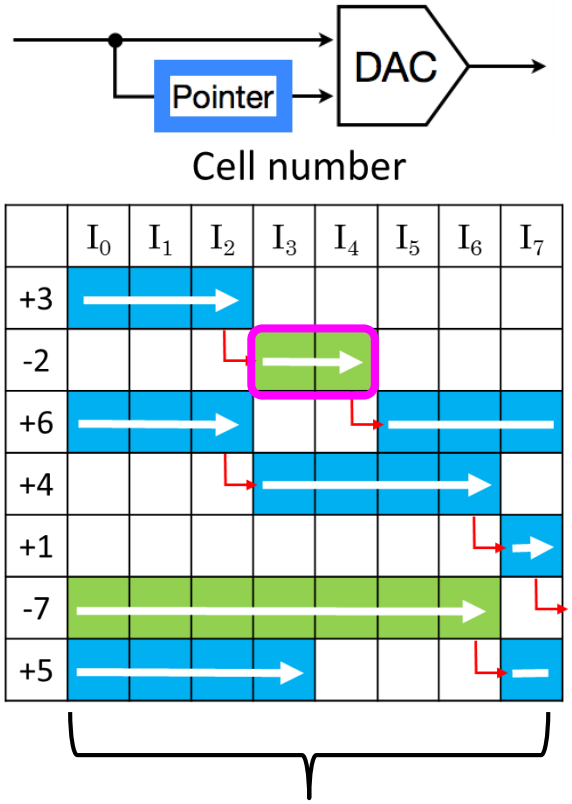
◆ DWA* DAC (*Data-Weighted Average)

DAC input = -2

$$I_{out} = I_+ - I_- = -[2 \times I + (e_3 + e_4)]$$

※ Switch ON in order





Disperse mismatch of particular cells

⇒Time-averaged

⇒ Linearity improvement ☺

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- **Self-Calibration Algorithm**
- Simulation Configuration & Results
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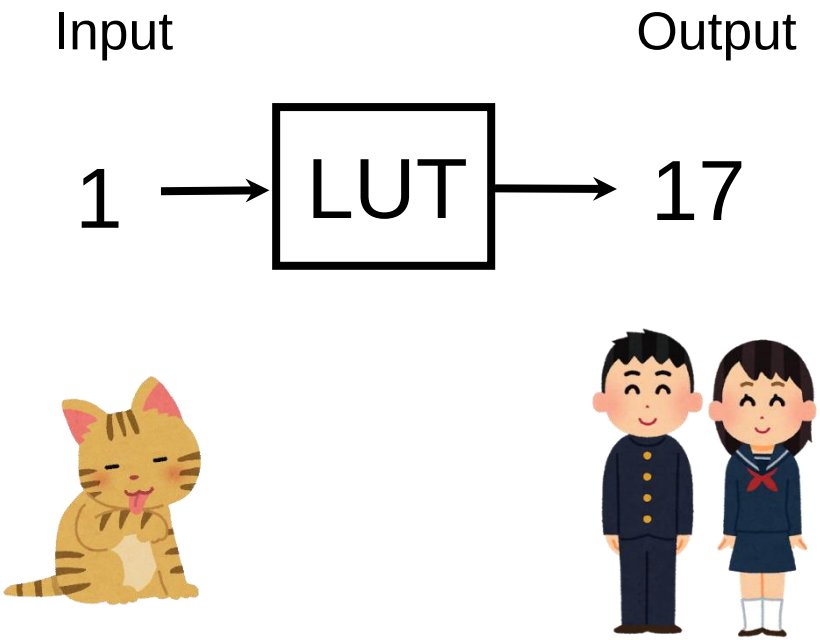
Look Up Table：LUT

- Data is stored in LUTs

  ➡ Output data is selected corresponding to input

For example

Cat age	Human age
1	17
2	23
3	28
4	32
5	36
6	40
7	44
8	48

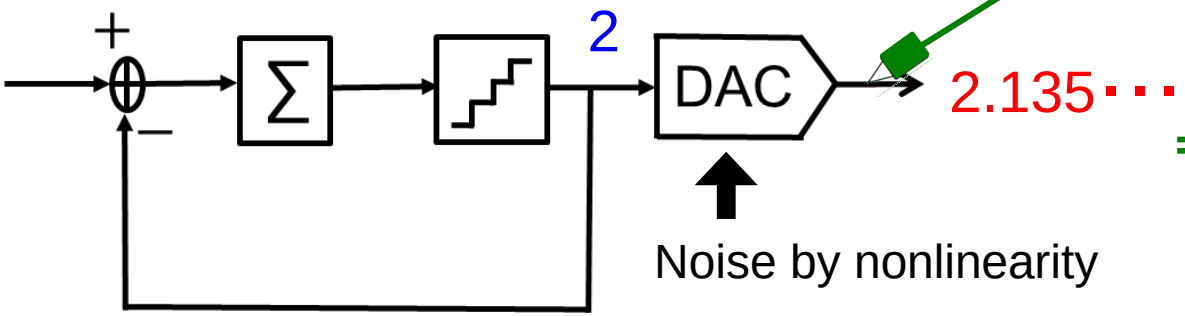


Self-Calibration Algorithm

Advance preparation

⇒ LUT data are created

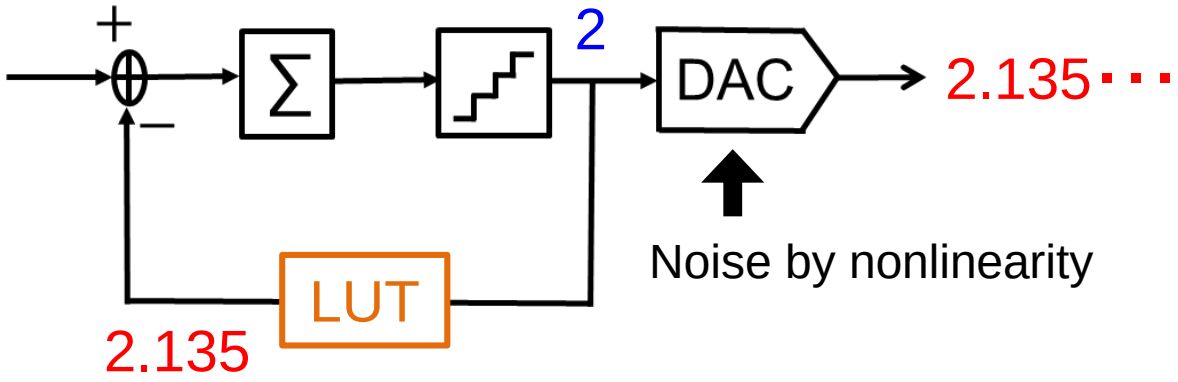
to measure feedback values with ΔΣADC



LUT

Input	Output
0	
1	
2	2.135
3	
⋮	

◆ Realization of Self-calibration



LUT

Input	Output
0	0.000
1	1.241
2	2.135
3	2.926
⋮	

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- **Simulation Configuration & Results**
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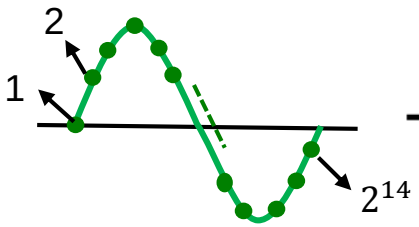
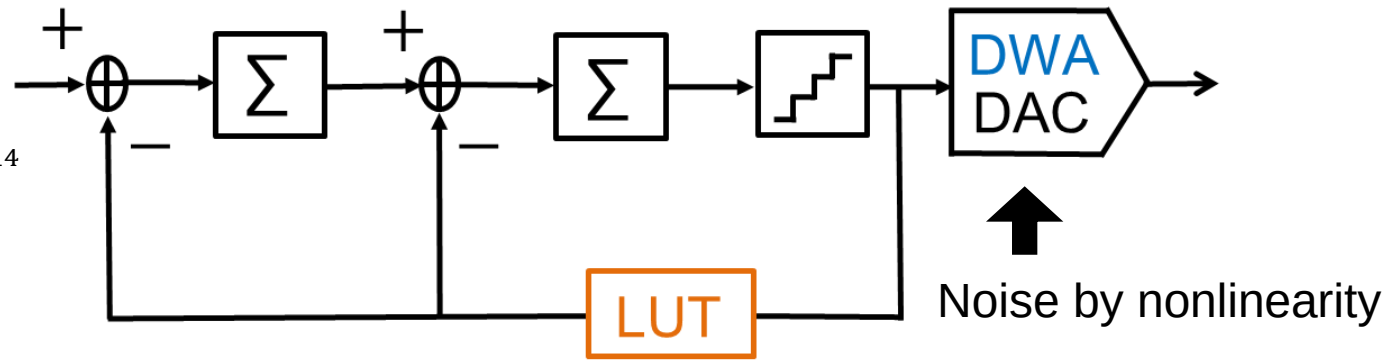
Simulation Configuration (LP model)

◆ 2nd-order LP ΔΣ DAC



Sine wave

(In 14-bit case)



Noise by nonlinearity

- Combination comparison

① 2nd LP ΔΣ Modu. + Nonlinear DAC

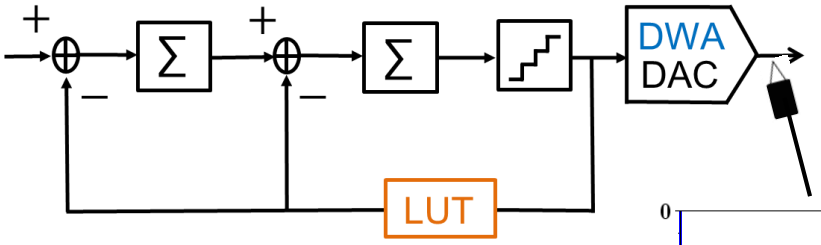
② 2nd LP ΔΣ Modu. + Nonlinear DAC + DWA (type Ⅰ)

③ 2nd LP ΔΣ Modu. + Nonlinear DAC + self-calibration

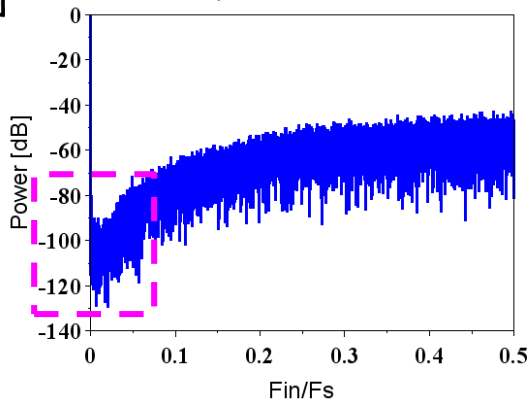
④ 2nd LP ΔΣ Modu. + Nonlinear DAC + DWA (type Ⅰ) + self-calibration (⇐ Prop.)

We verify linearity improvement

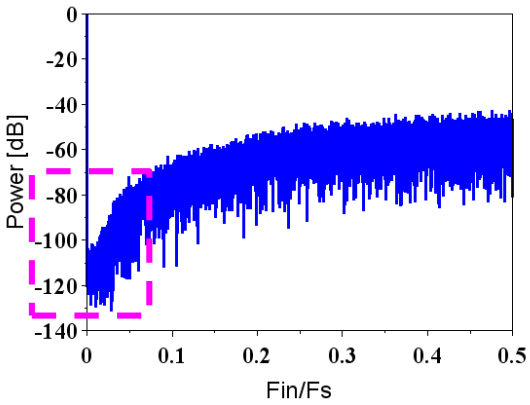
Simulation Results (LP model)



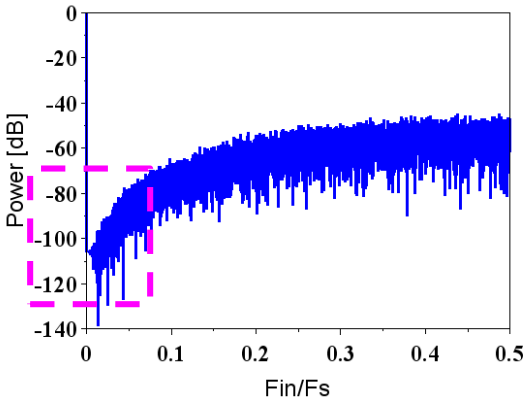
- ΔΣ DA output power spectrum
  (Mismatch standard deviation : σ = 1.0 %)



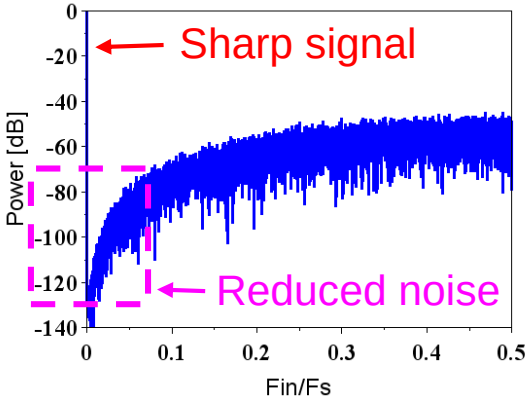
① × DWA, × Self-calibration



② ○ DWA, × Self-calibration

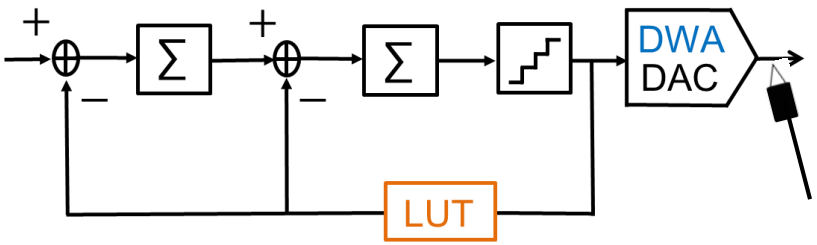


③ × DWA, ○ Self-calibration



④ ○ DWA, ○ Self-calibration

SNDR Comparison (LP model)

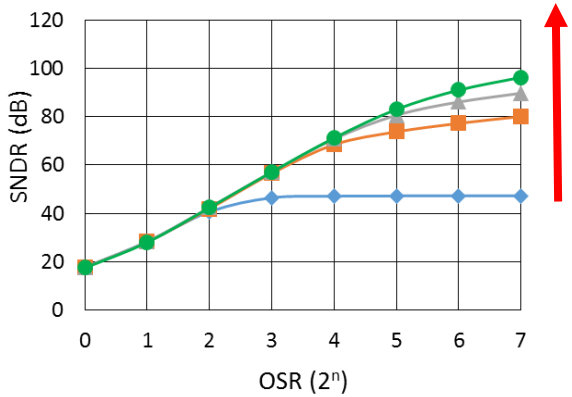


	①	②	③	④
DWA	×	○	×	○
Self-calibration	×	×	○	○

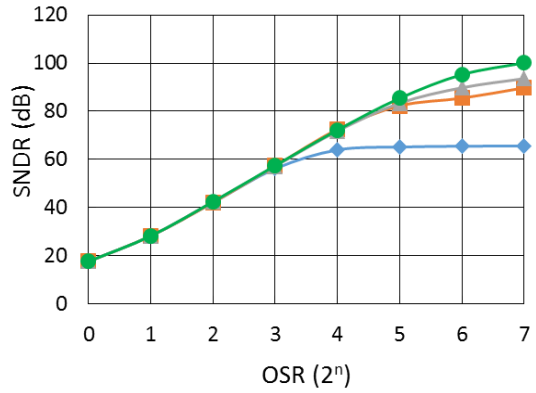
Great performance ☺

Proposed circuit
with DWA & self-calibration
(④)

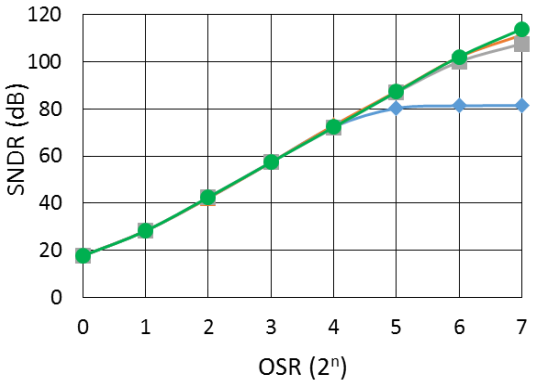
SNDR improvement



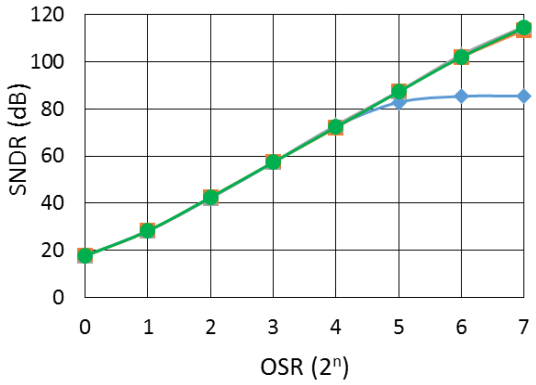
(a) σ = 5.0 %



(b) σ = 1.0 %



(c) σ = 0.1 %



(d) σ = 0.05 %

- Performance evaluation

$$\underline{\text{SNDR}} = \frac{\text{Signal}}{\text{Noise + Distortion}}$$

(Signal to Noise and Distortion Ratio)

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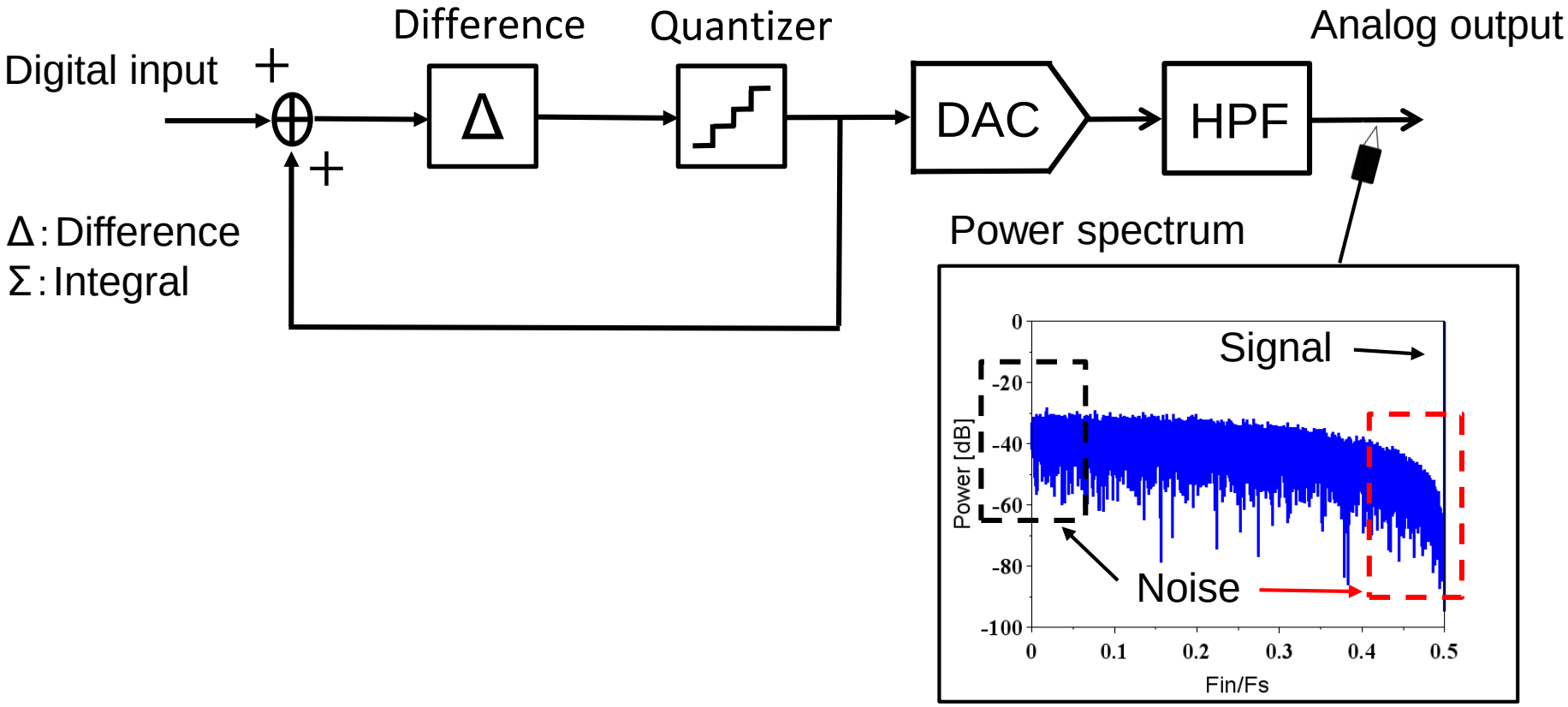
ΔΣ DA Converter (HP model)

✓ Similarly, we have simulated for HP ΔΣ DAC



Noise is decreased at high frequency
increased at low frequency

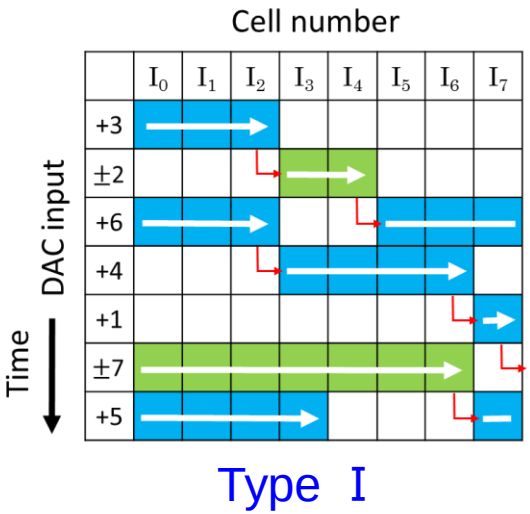
Effective DWA Type for HP

✓ We found that DWA type Ⅰ is effective for HP in the case of the ternary

Effective DWA type

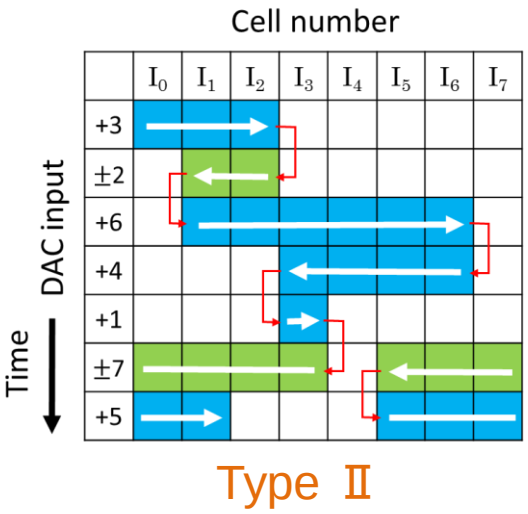
	LP	HP
Binary (+, 0)	Type Ⅰ	Type Ⅱ
Ternary (+, 0, −)	Type Ⅰ	**Type Ⅰ**

⇐ New finding



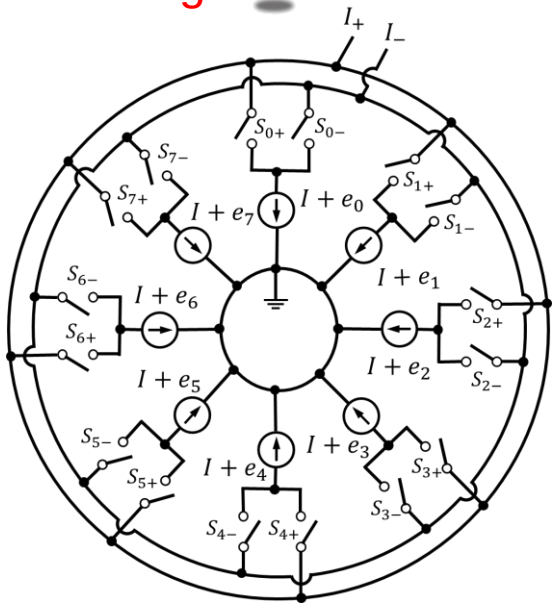
Type Ⅰ

(Go → Go → Go → ・・・)



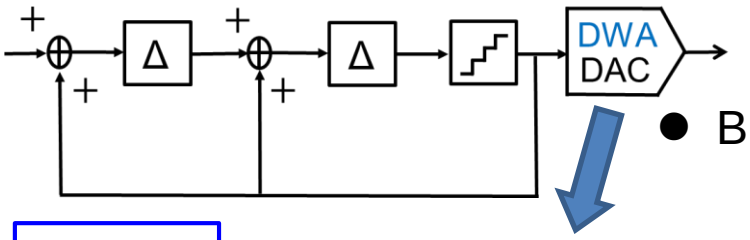
Type Ⅱ

(Go → Back → Go → ・・・)



DWA DAC

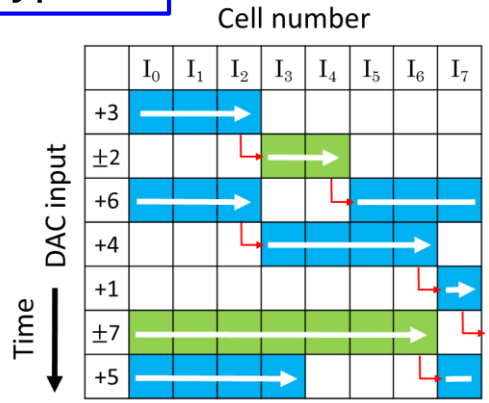
Simulation Results for DWA Type Ⅰ & Ⅱ

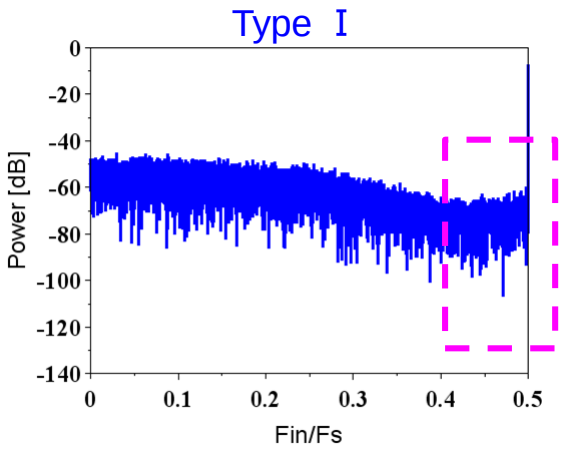


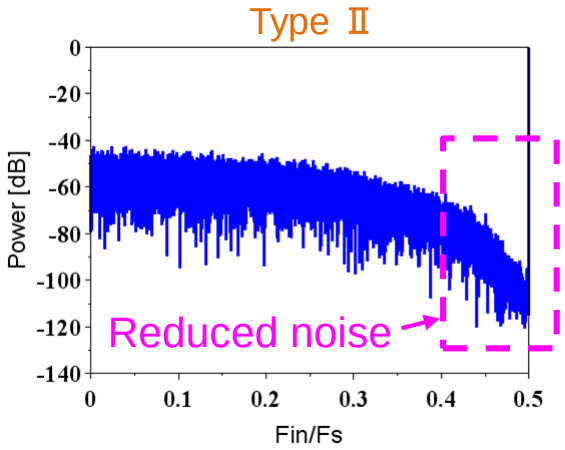
(Mismatch standard deviation : σ = 5.0 %)

- Binary (+, 0)

Type Ⅰ



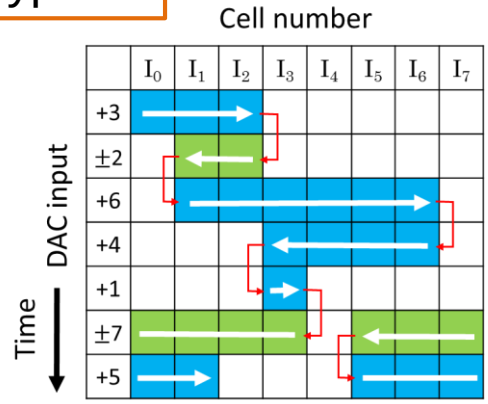


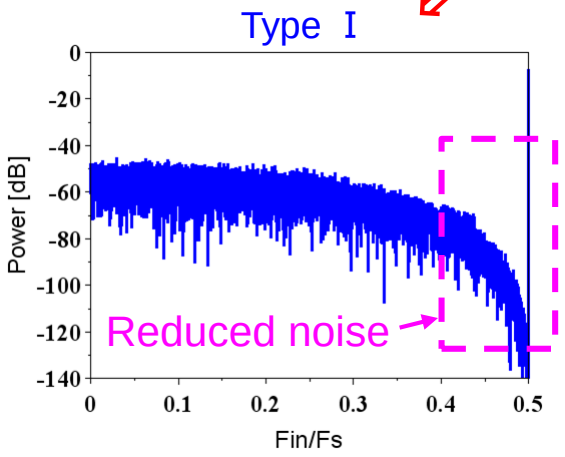


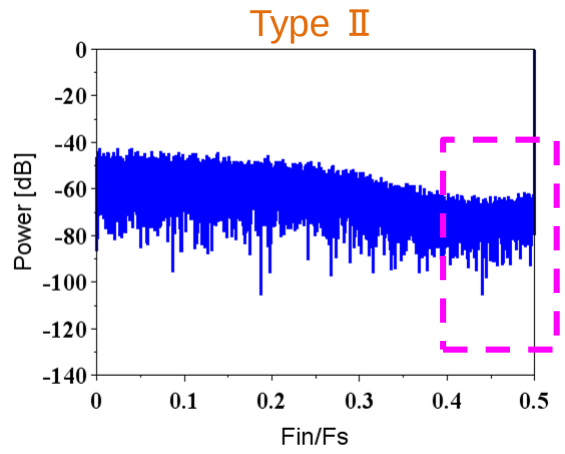
- Ternary (+, 0, −)

New finding

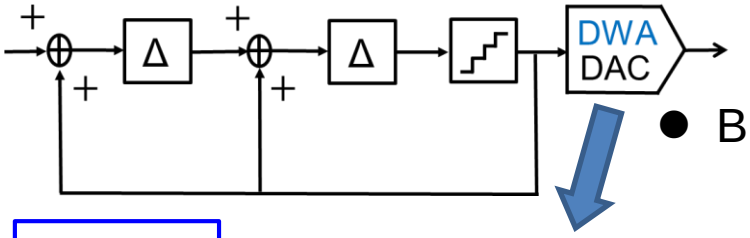
Type Ⅱ







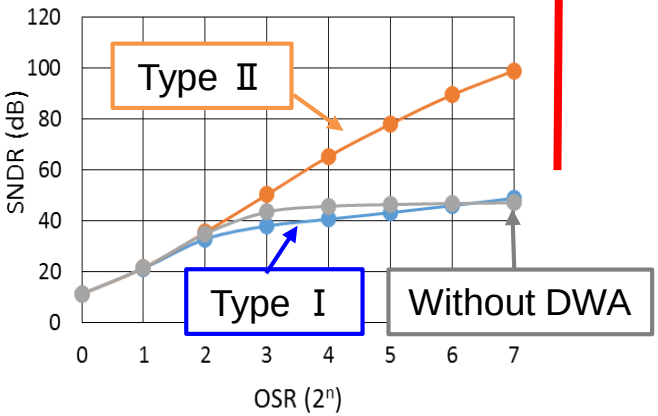
SNDR Comparison (HP model)



(Mismatch standard deviation : σ = 5.0 %)

- Binary (+, 0)

Great performance ☺

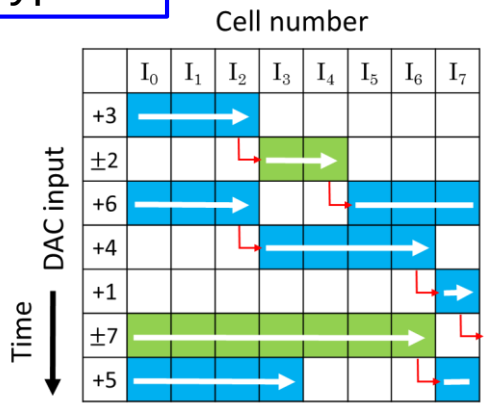


DWA Type Ⅱ

↓

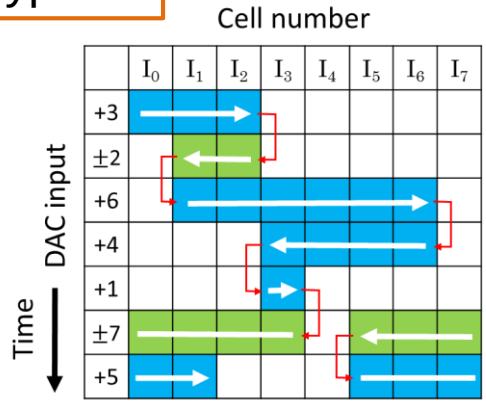
Effective method

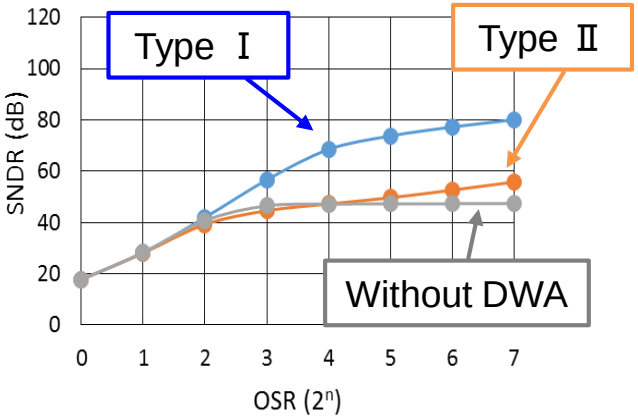
Type Ⅰ



- Ternary (+, 0, −)

Type Ⅱ





DWA Type Ⅰ

↓

Effective method

Outline

- Research Background
- DWA* Algorithm (* Data-Weighted Averaging)
- Self-Calibration Algorithm
- Simulation Configuration & Results
- New finding for HP ΔΣ DAC
- **Conclusion**

Conclusion

- Multi-bit ΔΣ DAC

  Conventional:

  Nonlinearity problem for process variation inside IC chip

  Proposed:

  Using DWA & self-calibration ⇒ Linearity improvement

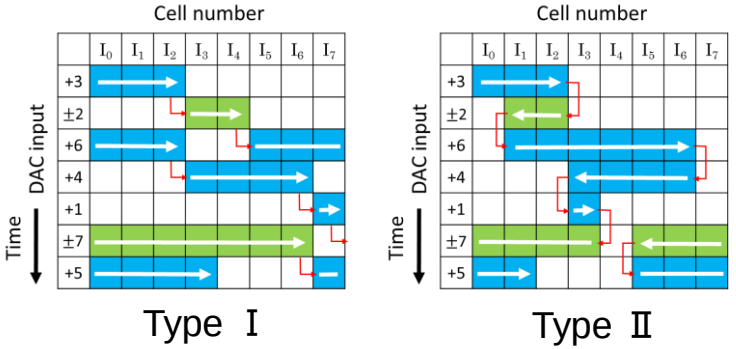
- New finding

  DWA type Ⅰ

  ⇒ Effective for HP in the case of the ternary

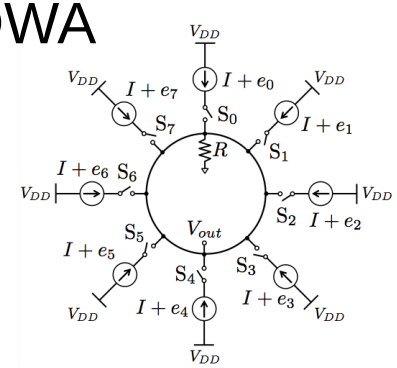
	LP	HP
Binary (+, 0)	Type Ⅰ	Type Ⅱ
Ternary (+, 0, −)	Type Ⅰ	**Type Ⅰ**

⇐New finding



Combining Great Things is Wonderful

DWA



Self-calibration

LUT

Cat age	Human age
1	17
2	23
3	28
4	32
5	36

Linearity improvement

Effective method × Effective method ⇒ Wonderful effective method

Great food × Great food ⇒ Delicious food !!

Curry and rice

Tonkatsu
(Japanese pork cutlet)

Katsu curry
(Curry rice with pork cutlet)