Time-to-Digital Converter Architecture Using Asynchronous Two Sine Waves with Different Frequencies

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Outline

- Research Objective
- Proposed TDC Principle
- Individual Circuit
  - Trigger Circuit
  - Logic Circuit
- Resolution of Proposed TDC
- SPICE Simulation verification
- Conclusion

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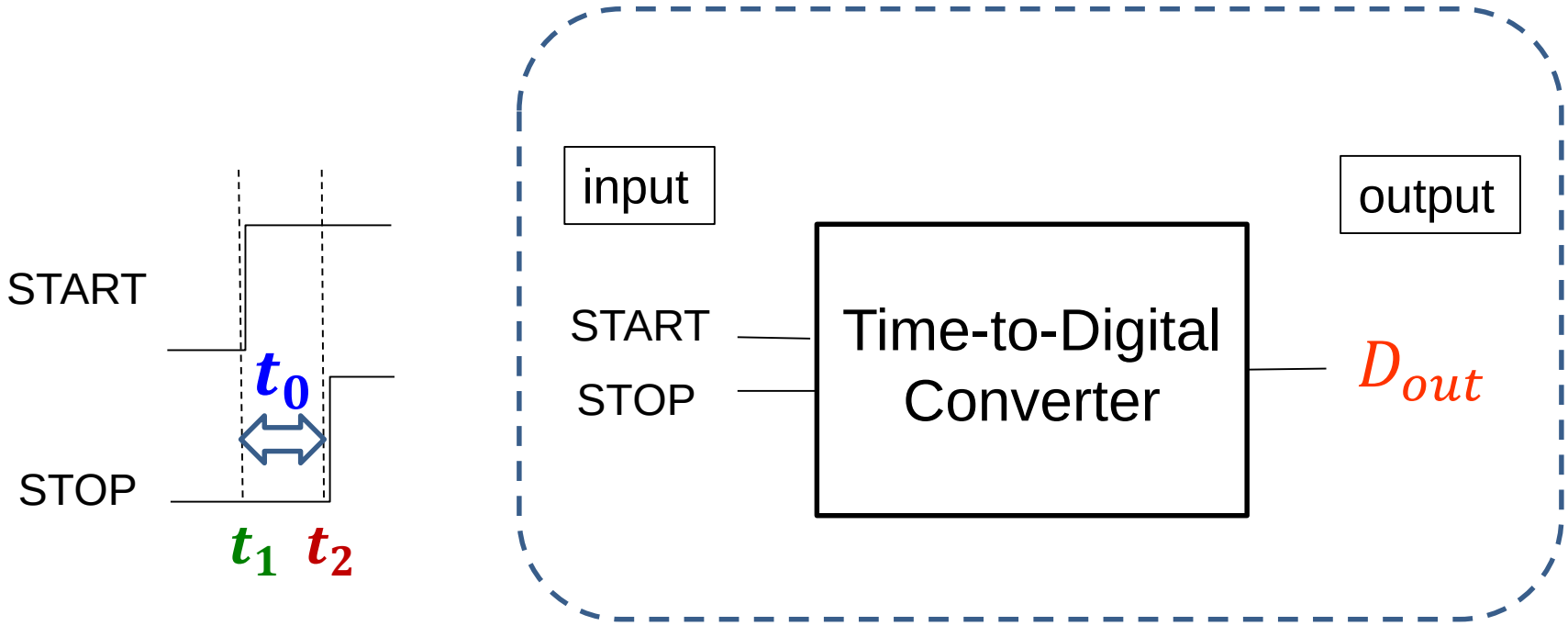
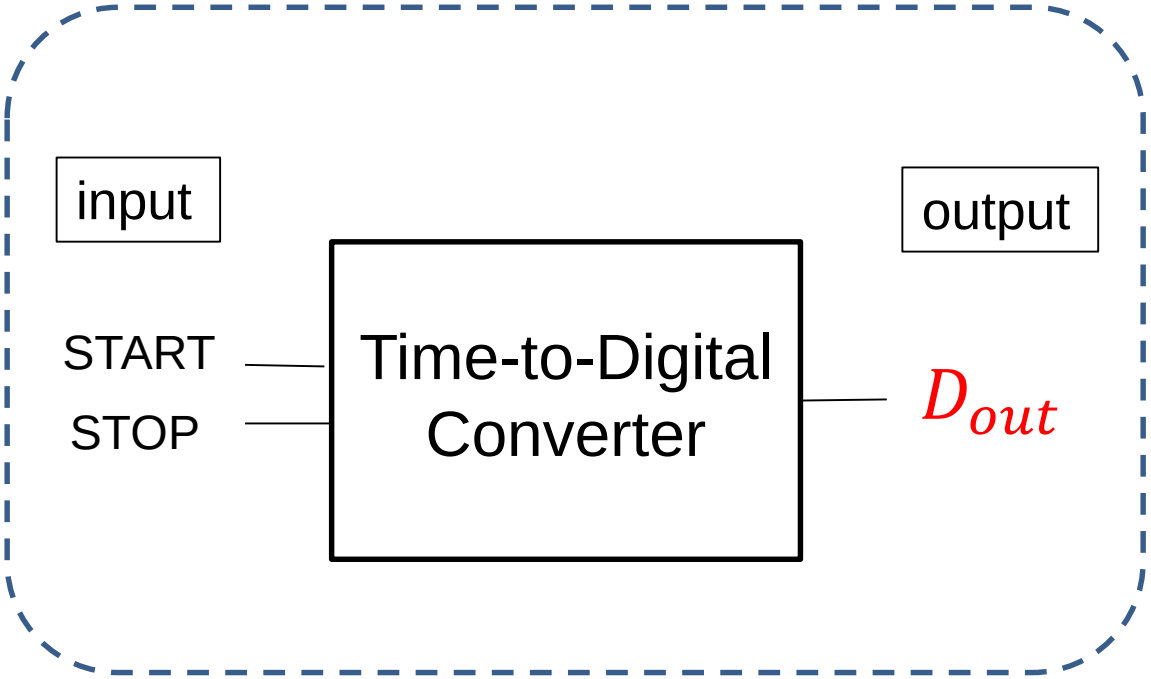
Time-to-Digital Converter



- Time-to-digital converter (TDC) measures **timing difference** t_0 between t_1 , t_2 and outputs as a **digital value** D_{out}

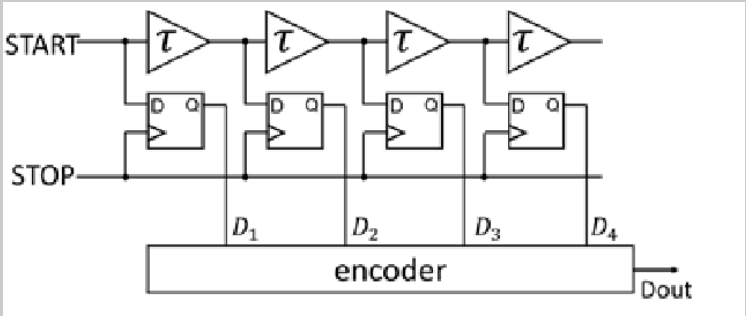
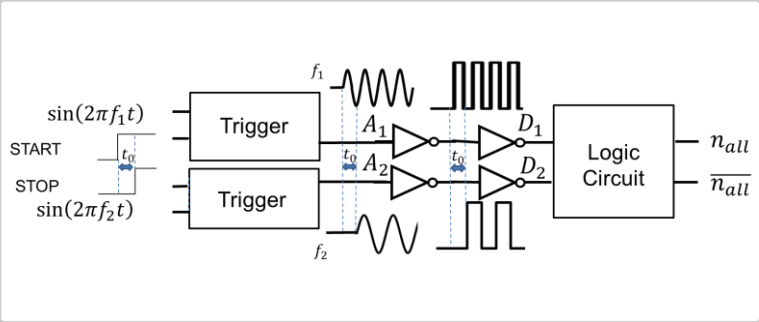
TDC Application Examples



Inter-vehicular distance measurement

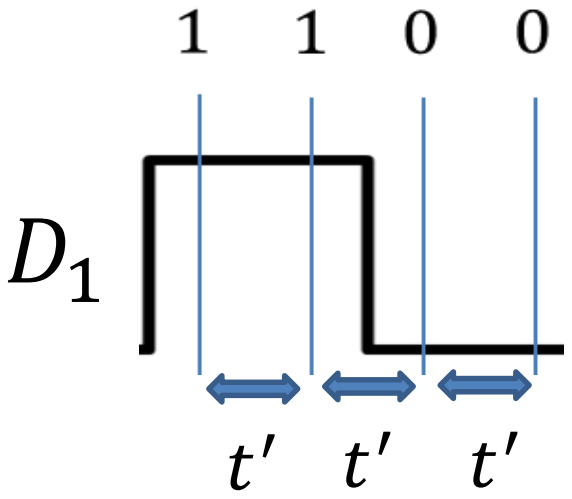
Satellite distance measurement

Comparison of TDC Architectures

	Conventional TDC	Proposed TDC
Circuit Architecture		
Delay Array	Necessary	Not necessary
Self Calibration	Required	Not required

Delay array have variations → Self-calibration is required

Comparison of frequencies



time resolution = $t'[s]$

Same Frequencies

$$Clock\ frequency \leq 1[GHz]$$

$$t' \geq \frac{1}{1[GHz]} = 1\ [ns]$$

Different Frequencies

$$t' = \left|\frac{1}{f_2} - \frac{1}{f_1}\right|$$

example

$f_1 = 1[MHz]$

$f_2 = 0.9999[MHz]$

$$t' \cong 0.1[ns]$$

Different frequencies → **time resolution** ⟺ **measurement time**

Trade off

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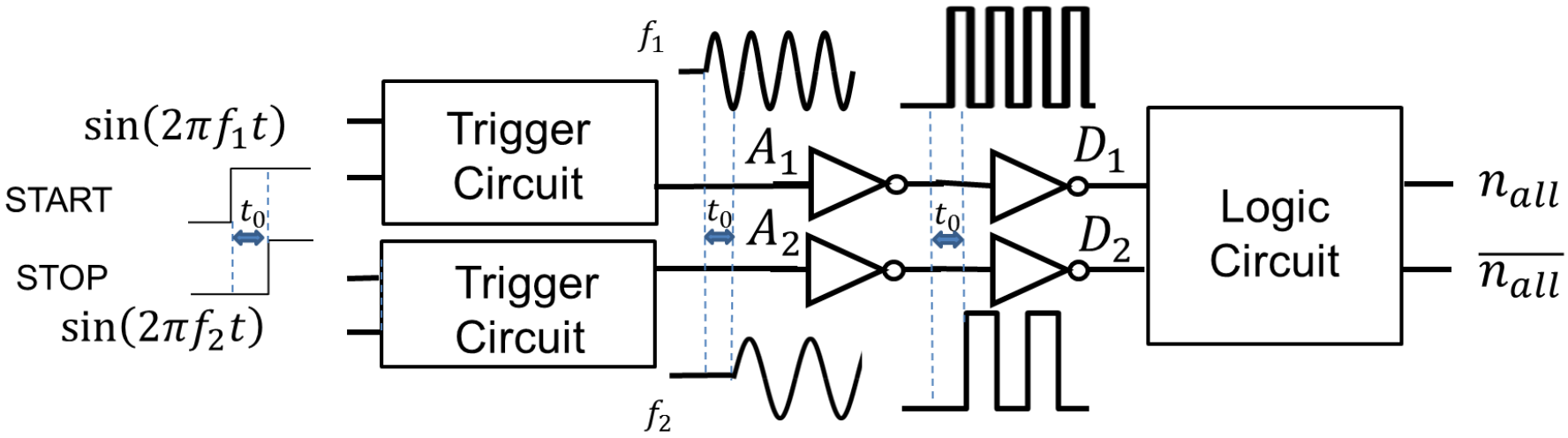
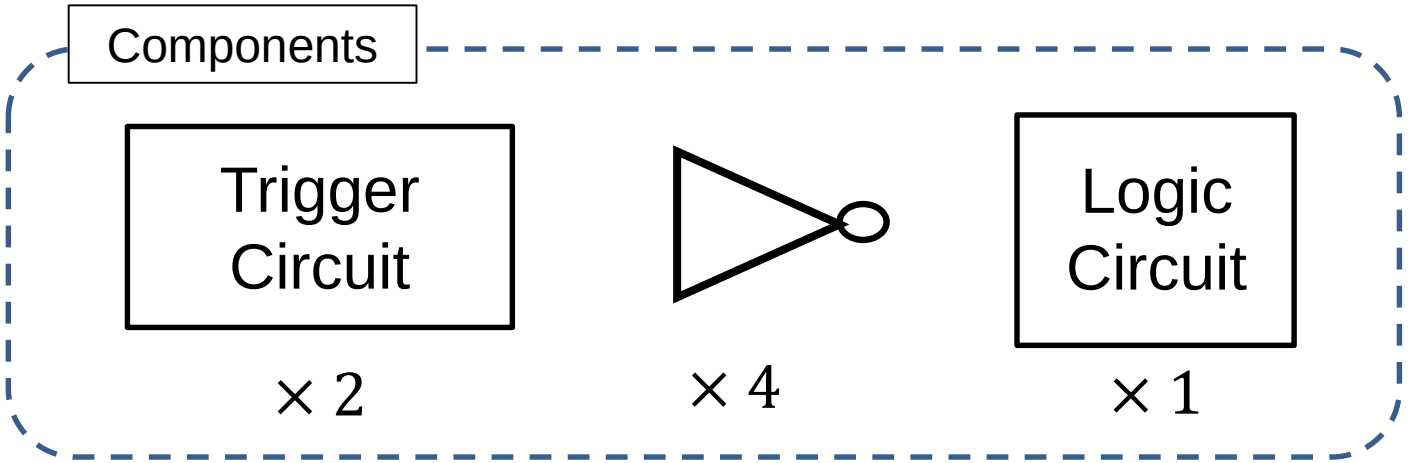
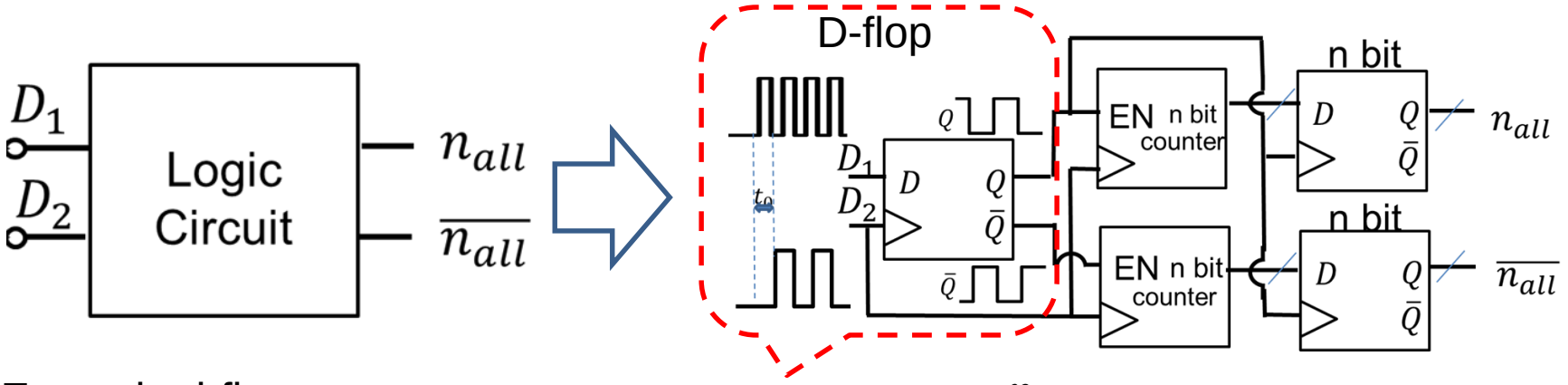
Proposed TDC Architecture

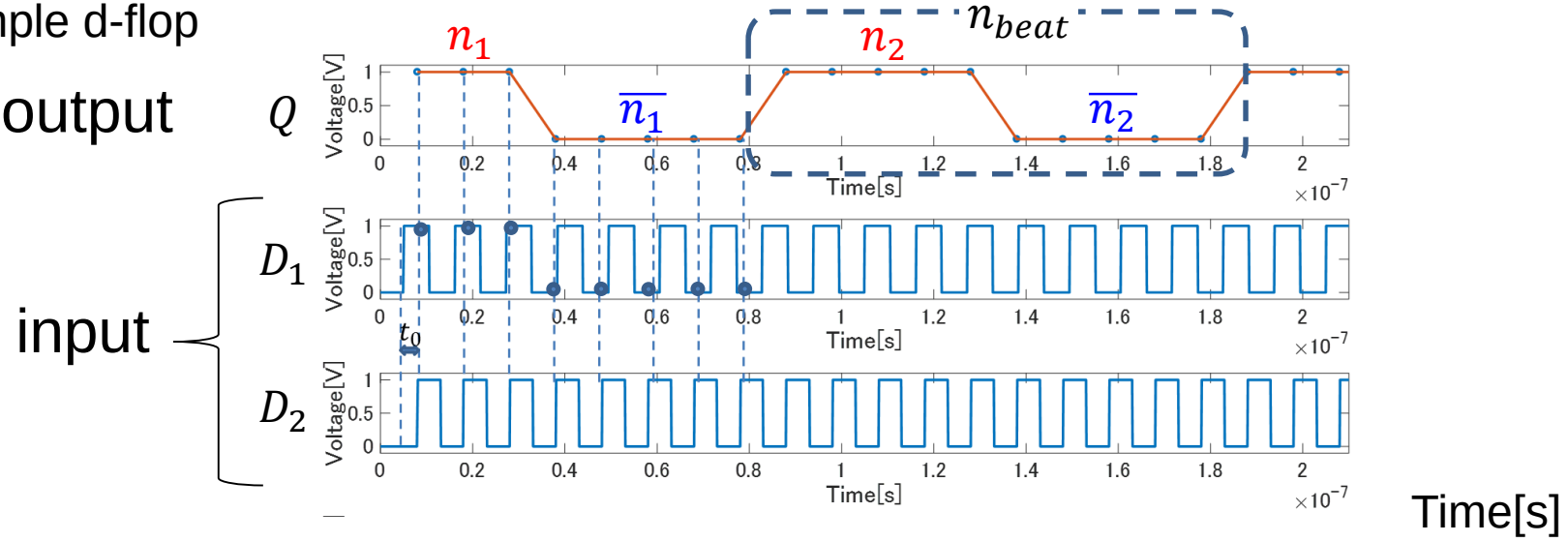




Basic Operation of Logic Circuit



Example d-flop



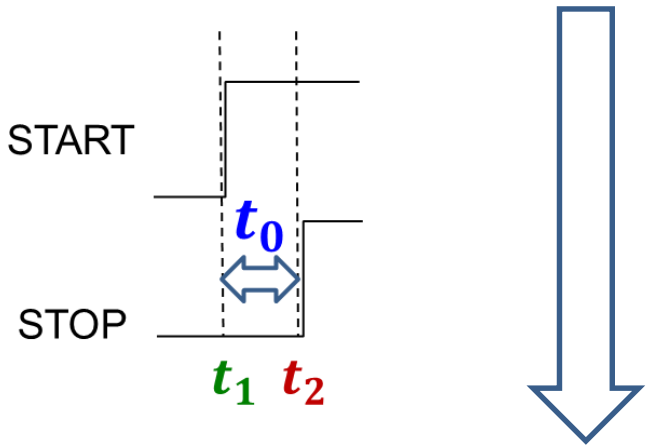
- $n_{all}(= n_1 + n_2 \ldots)$
- $\overline{n_{all}}(= \overline{n_1} + \overline{n_2} \ldots)$

- $n_{beat} \approx n_2 + \overline{n_2} = n_3 + \overline{n_3} = \cdots = \frac{f_2}{|f_2 - f_1|}$

How we calculate to timing difference t_0

- Proposed TDC Principle

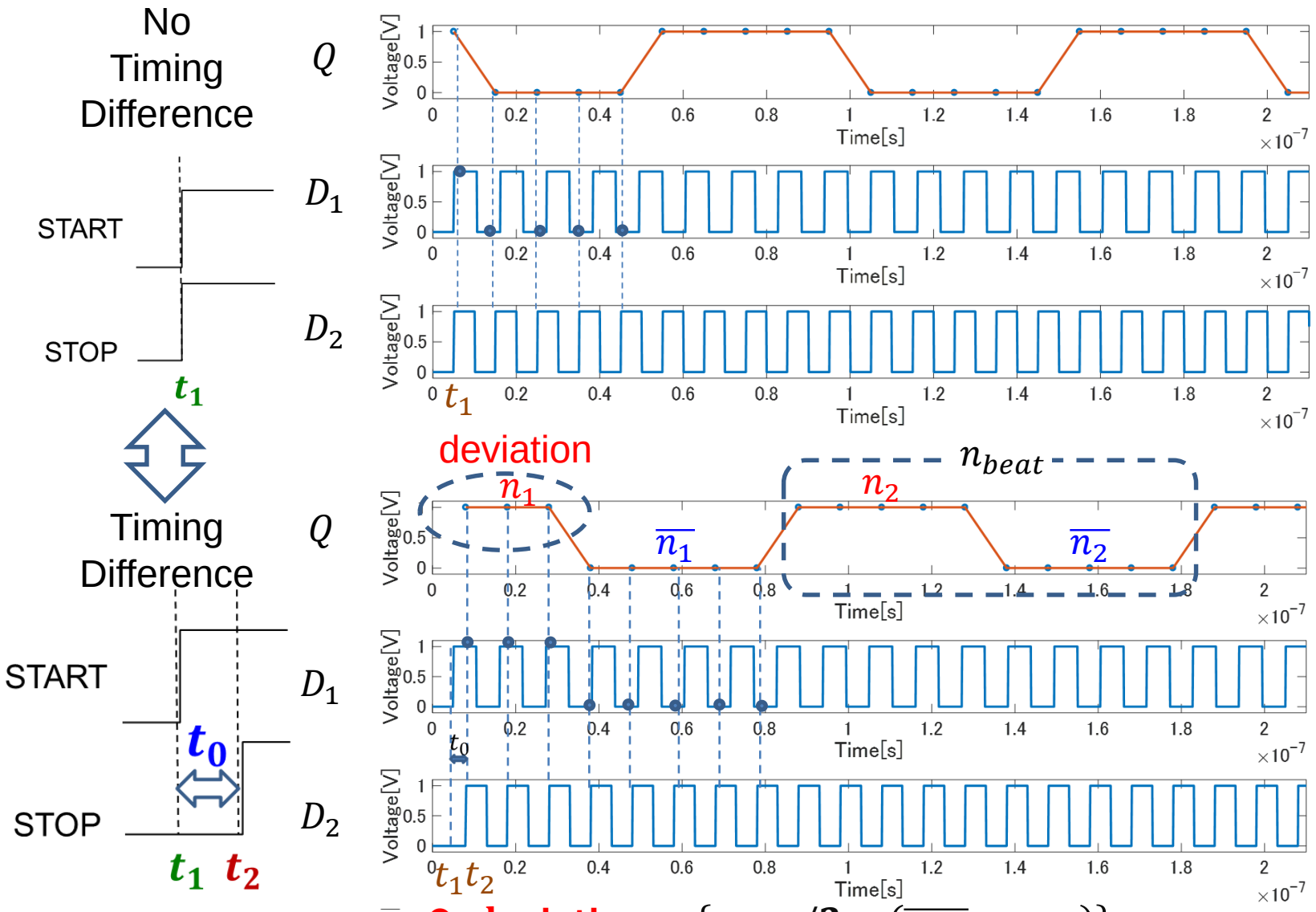
$t_0 =$ deviation points $\times$ one time difference



Details

$$t_0 = \{n_{beat}/2 - (\overline{n_{all}} - n_{all})\} \times t'$$

Timing difference generates deviation points

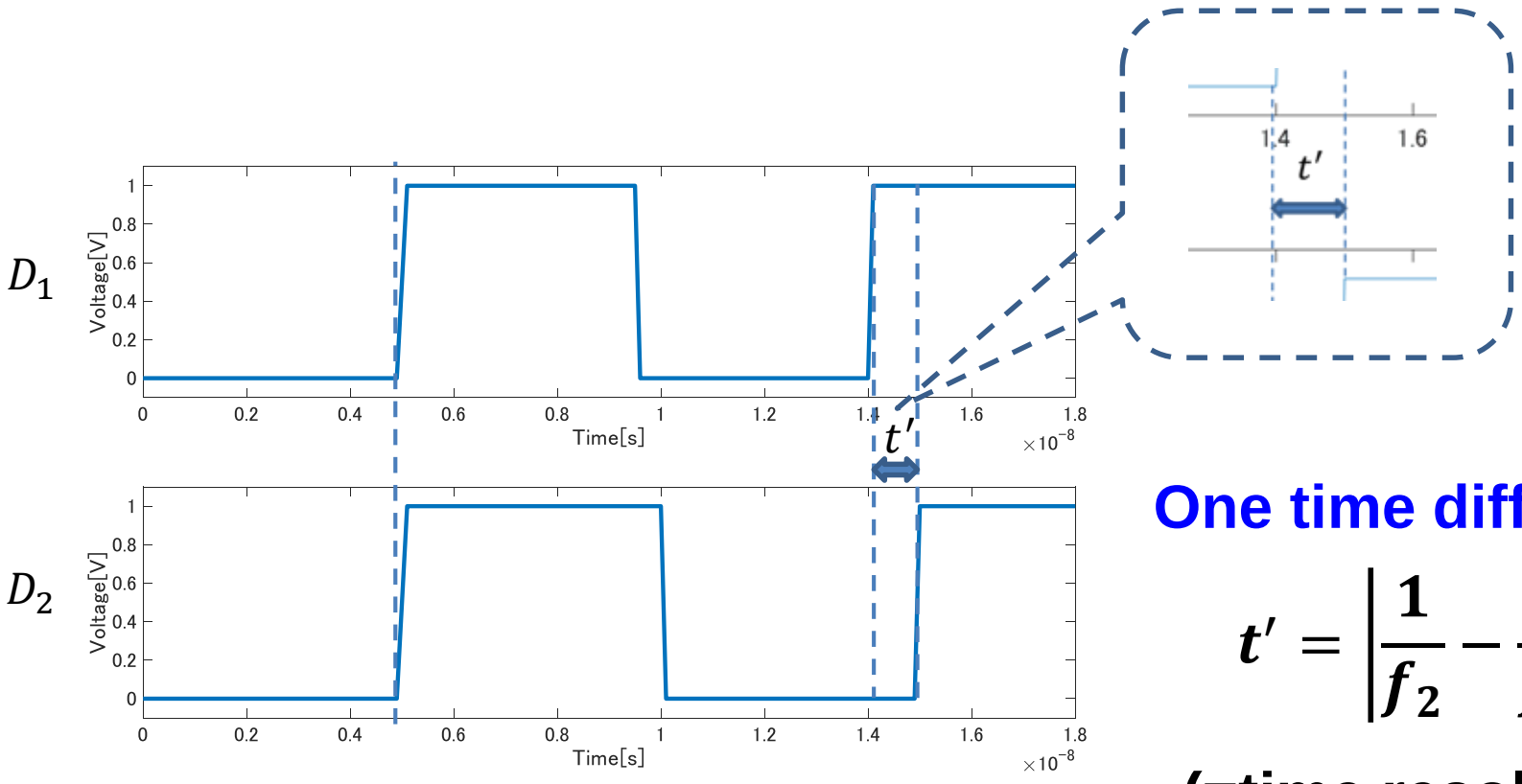


- **deviation** $= \{n_{beat}/2 - (\overline{n_{all}} - n_{all})\}$

$= \{(n_2 + \overline{n_2})/2 - ((\overline{n_1} + \overline{n_2} + \cdots) - (n_1 + n_2 + \cdots))\}$ $(\text{in case } f_1 < f_2)$

Time resolution is one time difference

◆ **One deviation points means**
One time difference t' between D_1 and D_2



One time difference

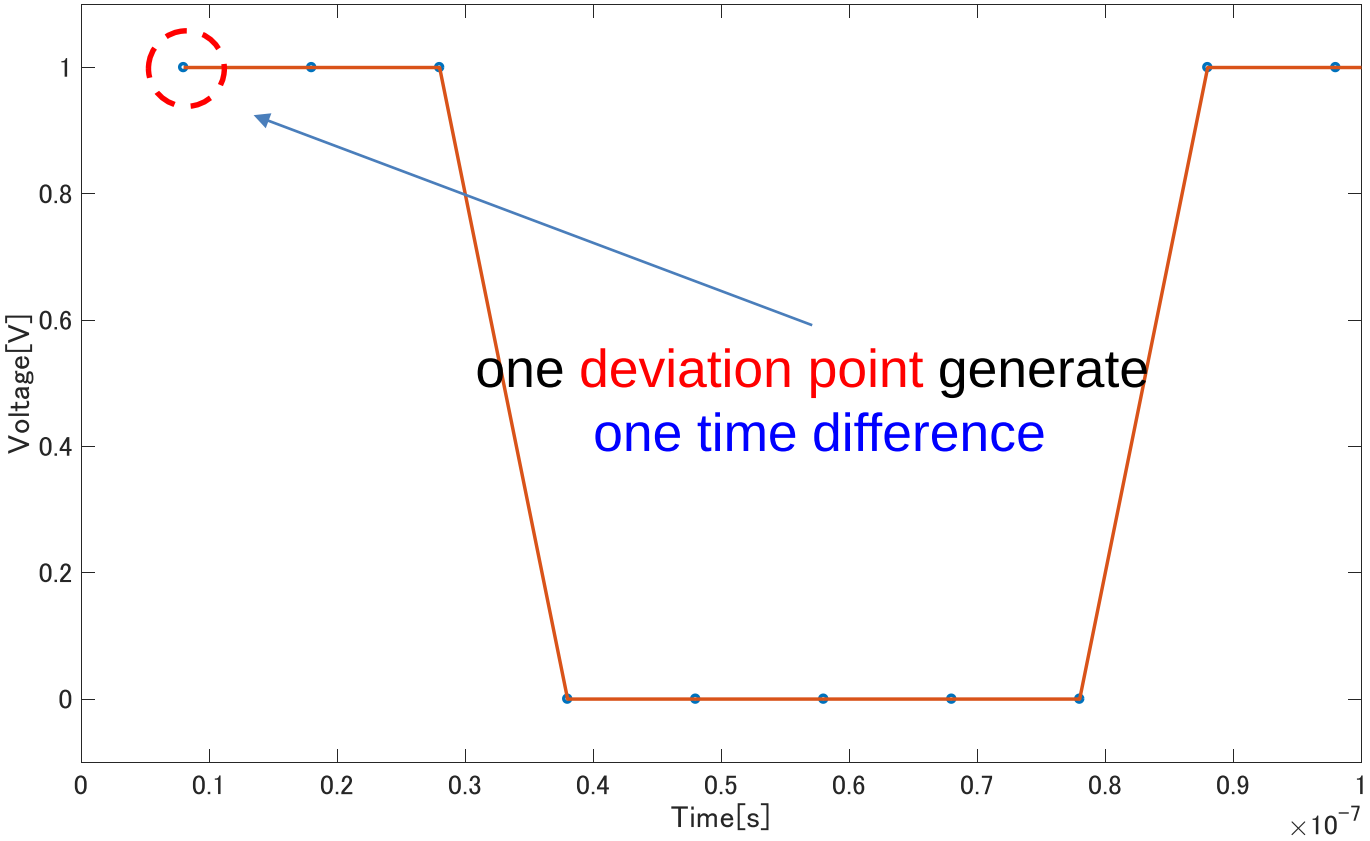
$$t' = \left| \frac{1}{f_2} - \frac{1}{f_1} \right|$$

(=time resolution)

t_0 = deviation points × one time difference

$$t_0 = \begin{cases} (\overline{n_{all}} - n_{all})t' & (\text{in } case\ f_1 > f_2) \\ \{n_{beat}/2 - (\overline{n_{all}} - n_{all})\}t' & (\text{in } case\ f_1 < f_2) \end{cases}$$

Q



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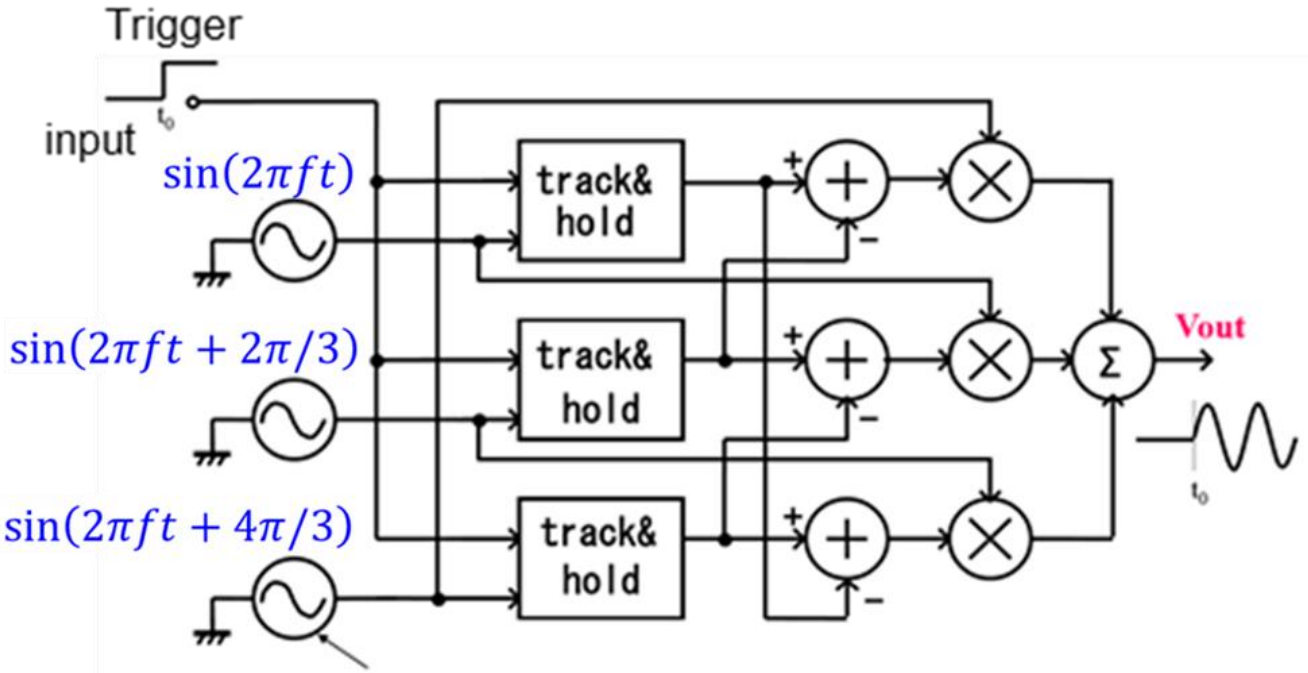
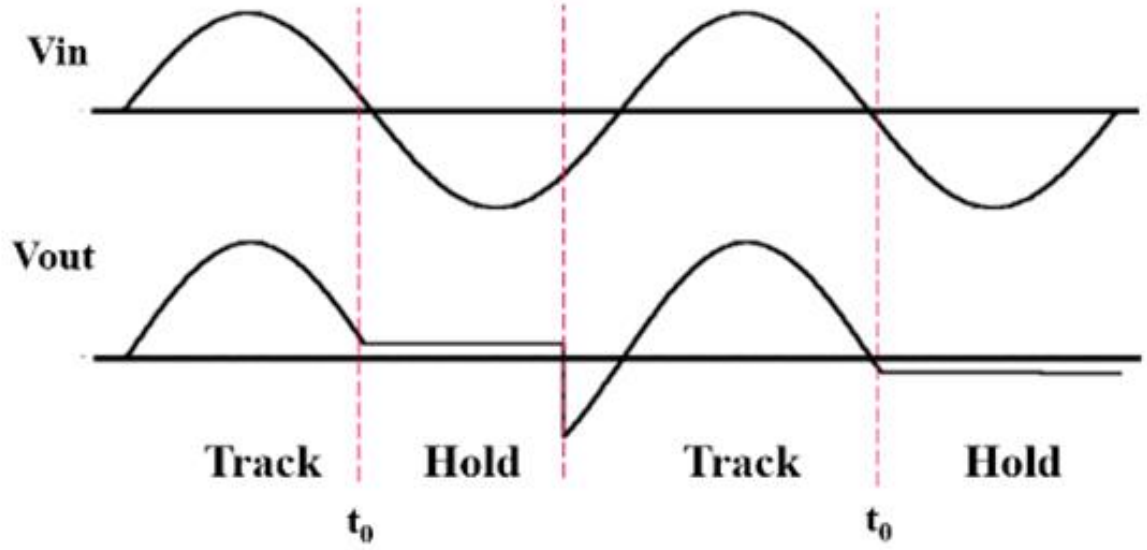
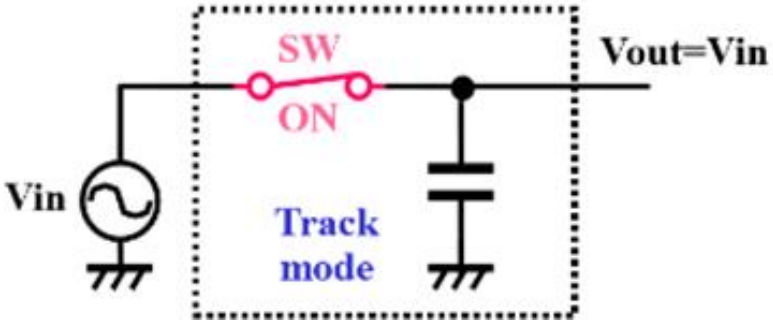
Trigger Circuit Architecture & Operation

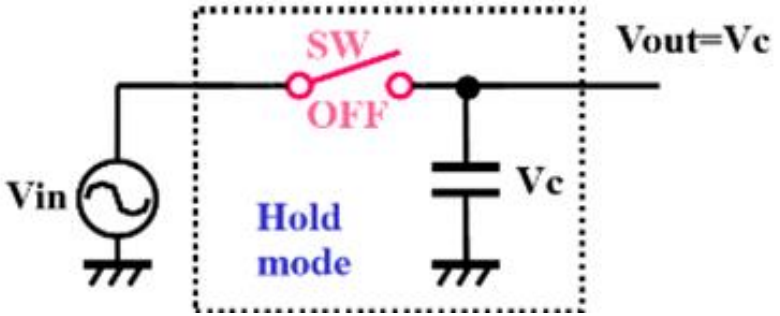


- Output starts to oscillate at rising timing edge of input
- Output waveform with no transient change

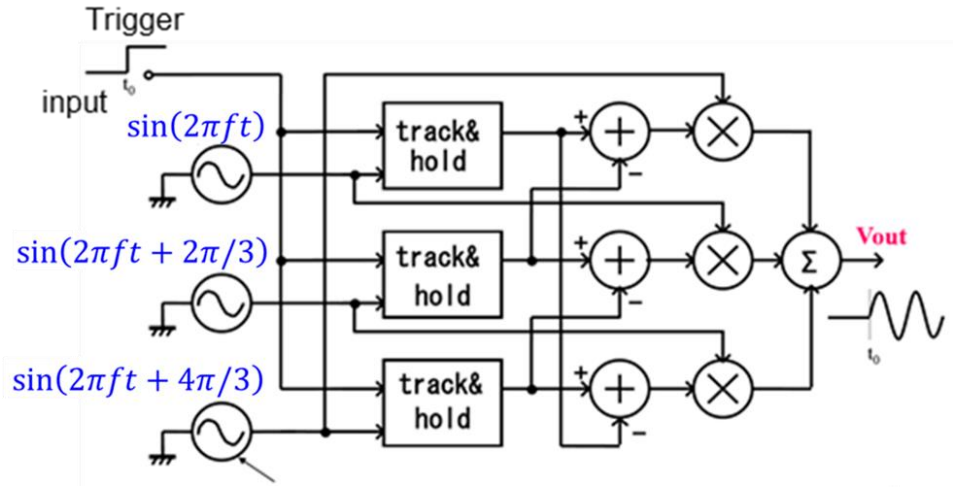
Track & Hold Circuit

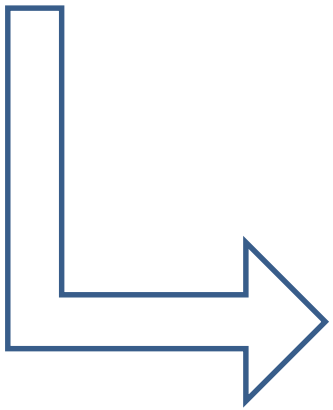


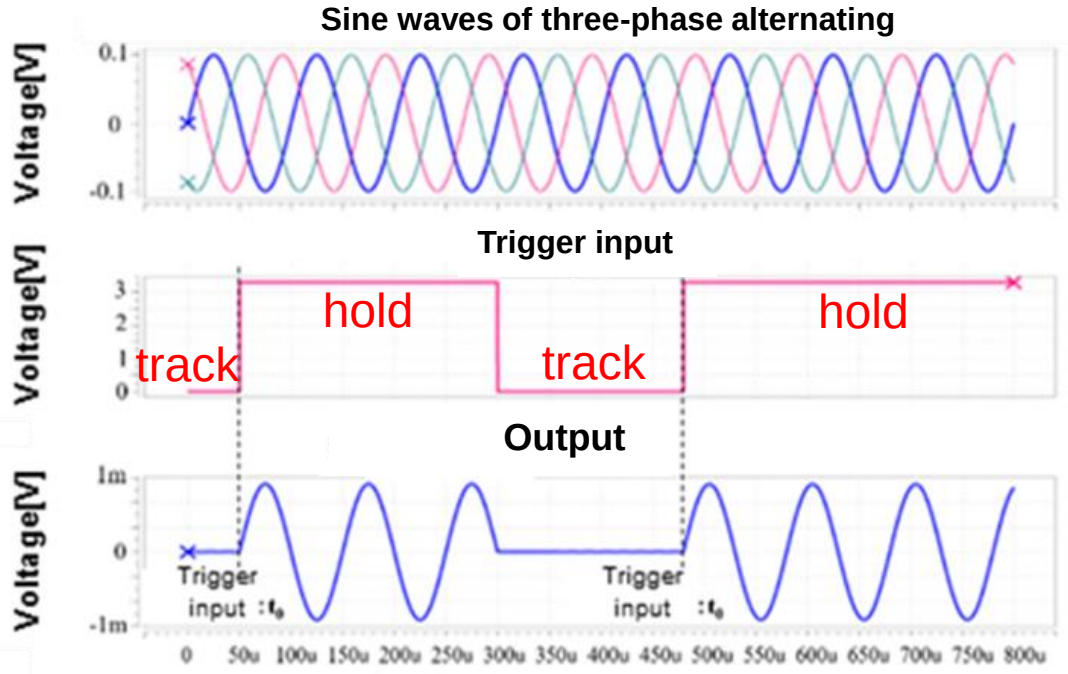




Trigger Circuit's Simulation Results







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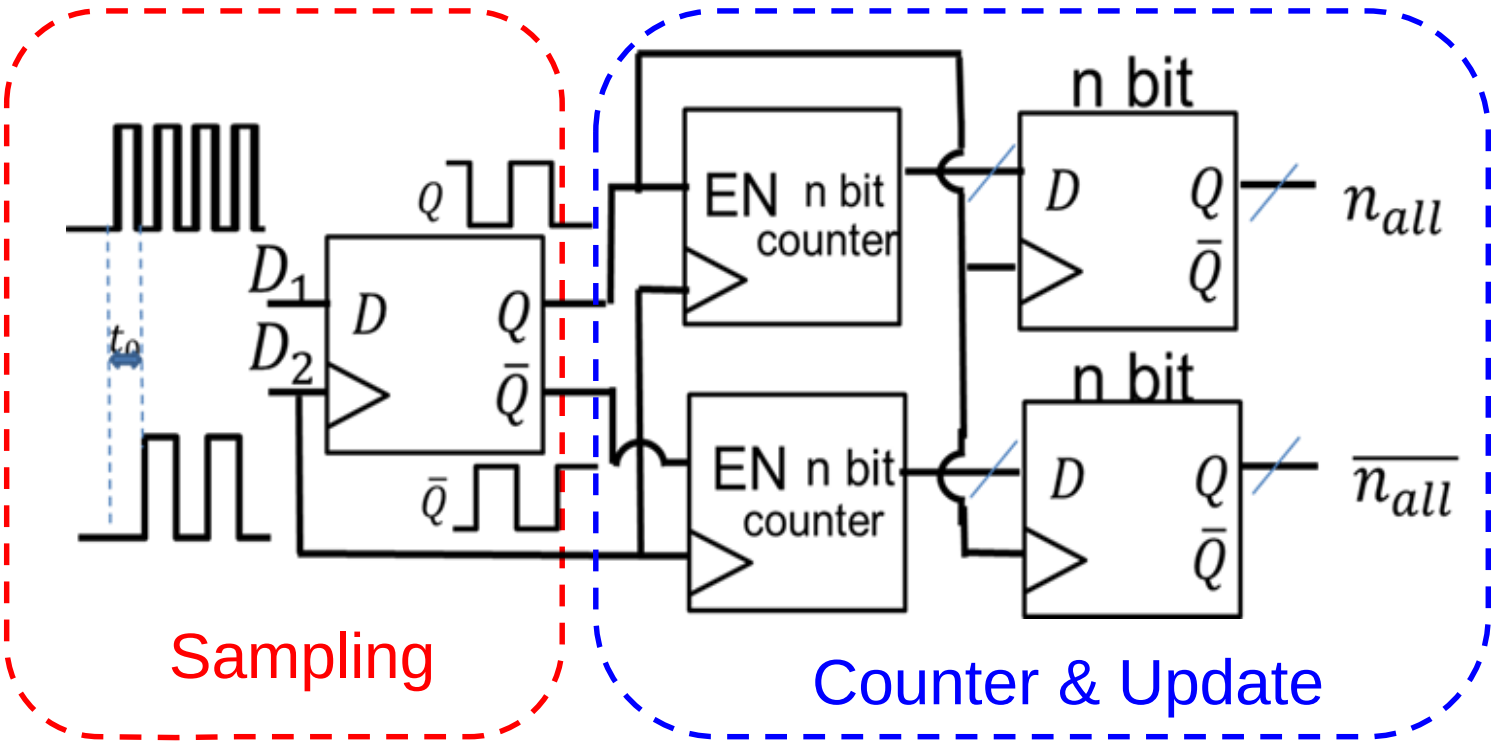
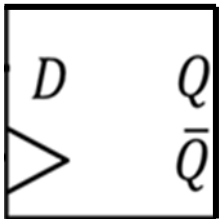
Logic Circuit Architecture



Components

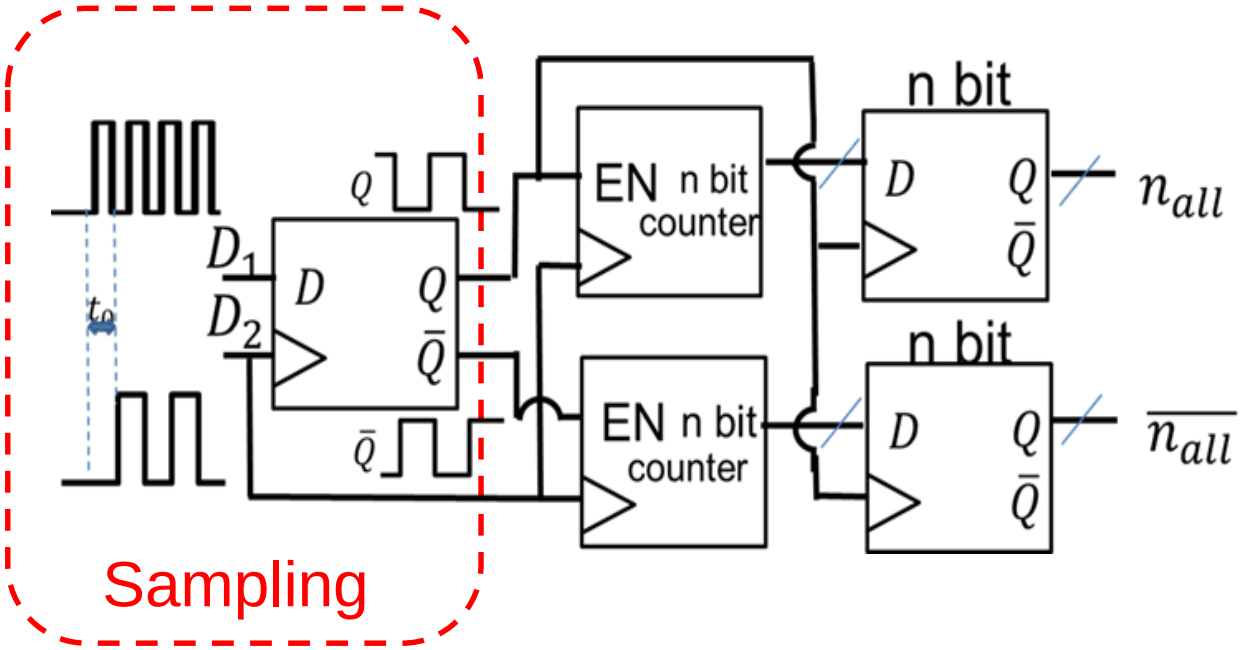


$\times$ *some*

$\times 2$

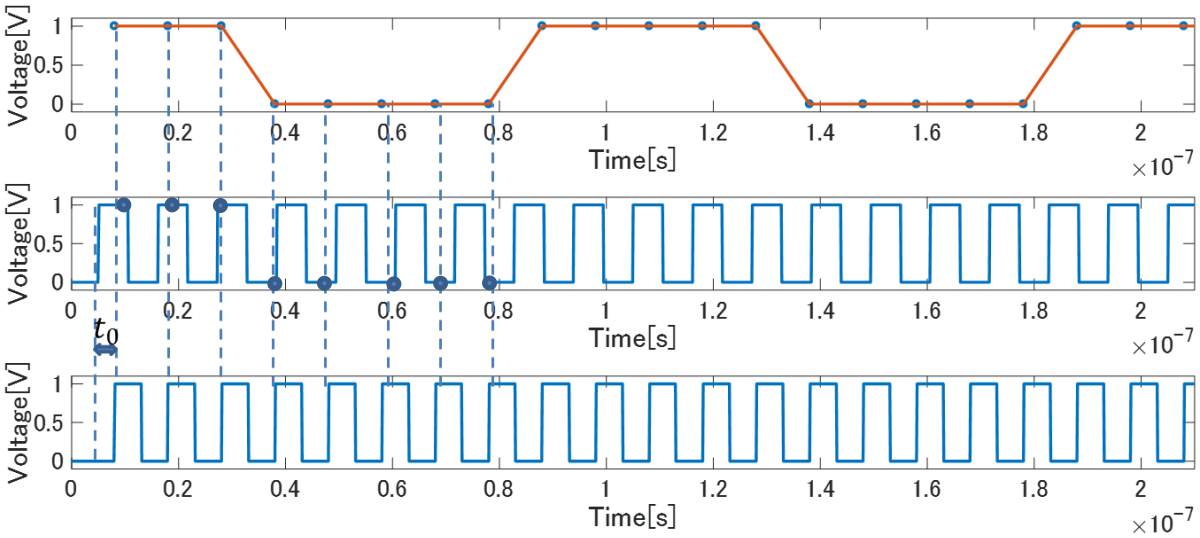
D-flop sampled D1 by clock D2

Example d-flop



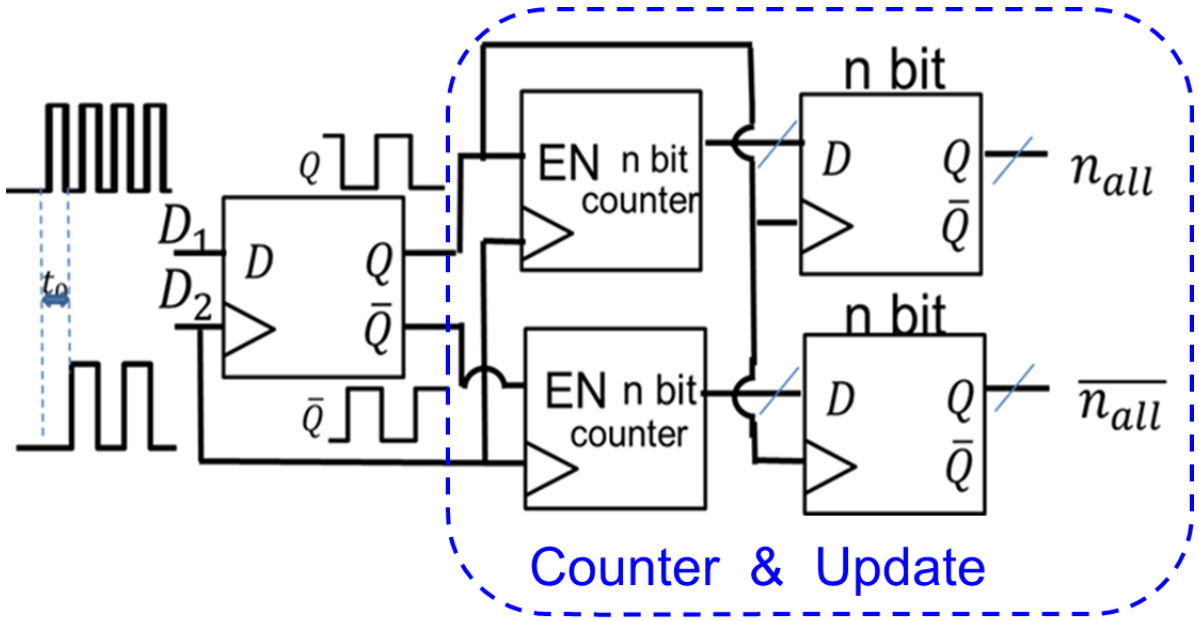
output Q

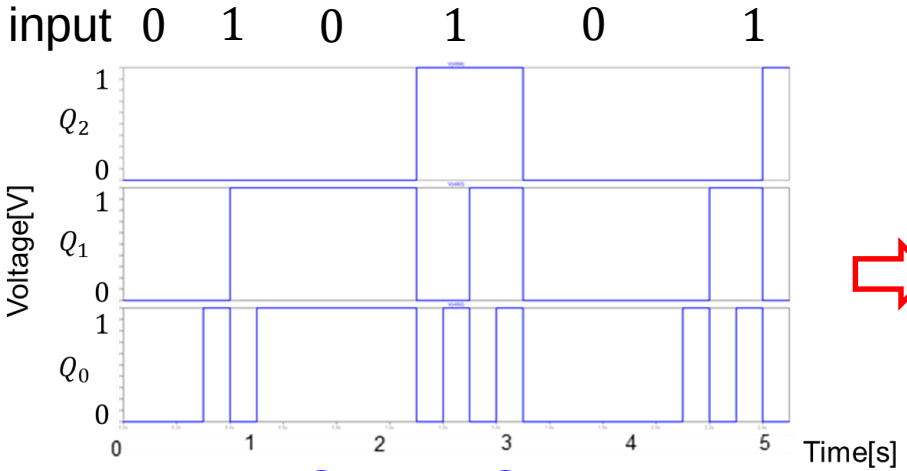
input D_1, D_2

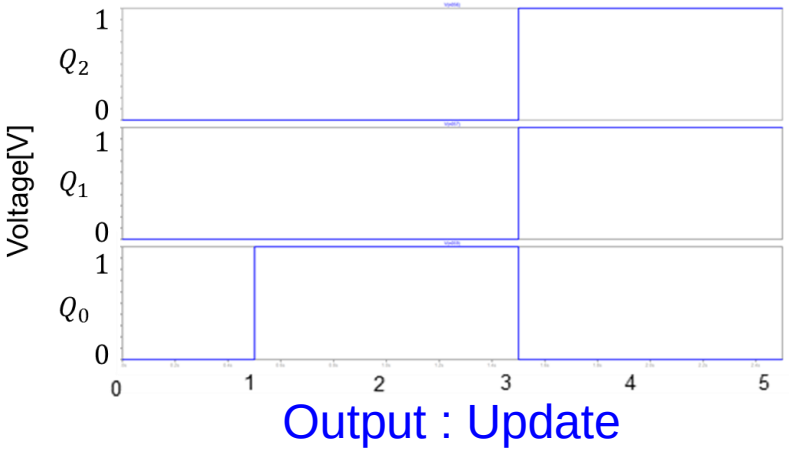


Time[s]

Counter & Update







Digital value

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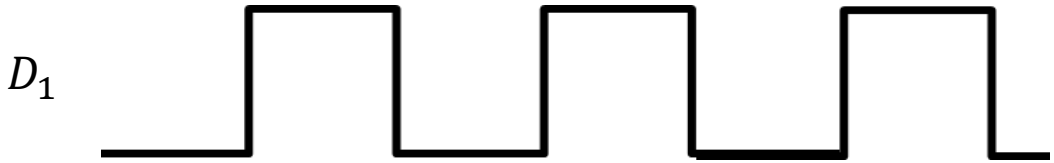
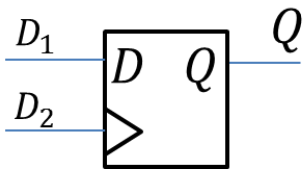
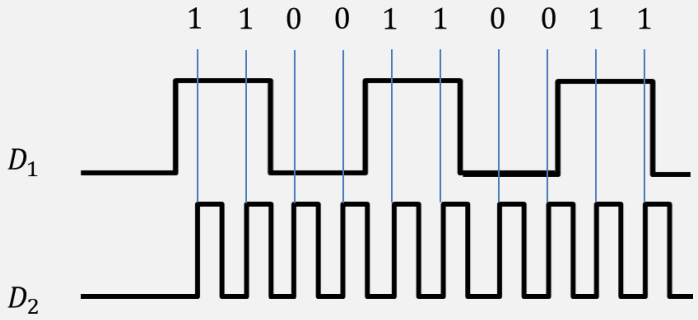
Time resolution image





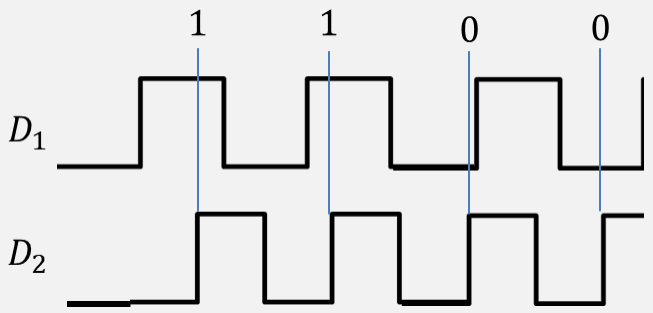
Sampling D_1 by clock D_2

$(in\ case\ f_1 \ll f_2)$



Fine time resolution

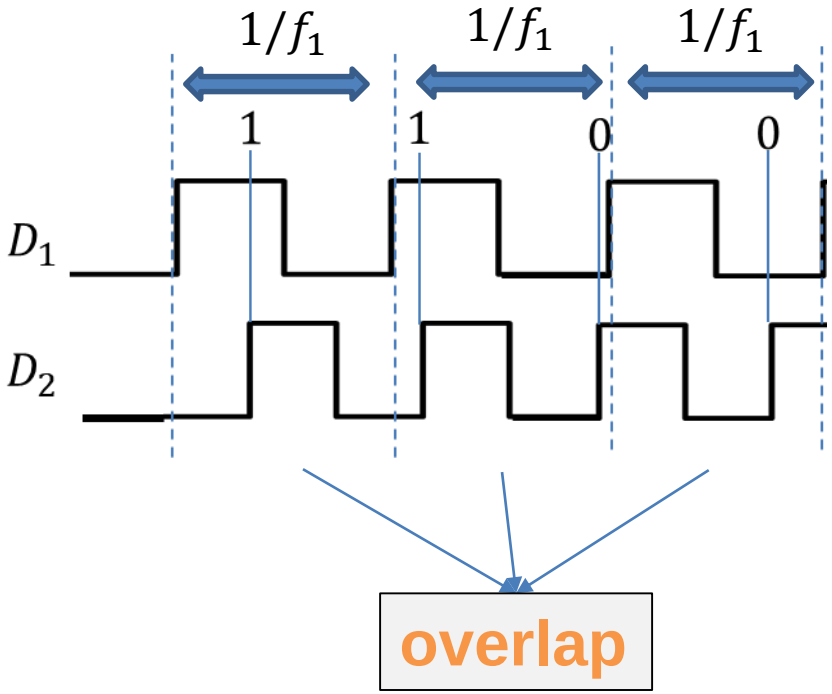
$(in\ case\ f_1 \approx f_2)$



Coarse time resolution ?

Overlapped outputs

$(in\ case\ f_1 \approx f_2)$

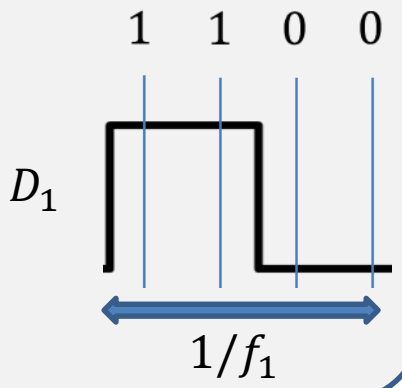


overlap

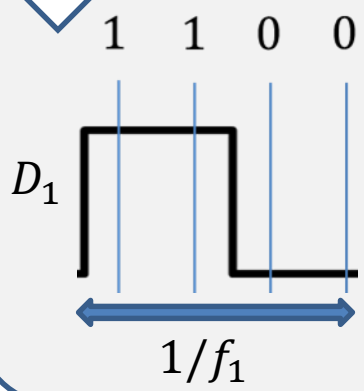
$(in\ case\ f_1 \ll f_2)$

Fine time resolution

Short measurement time



$(in\ case\ f_1 \approx f_2)$

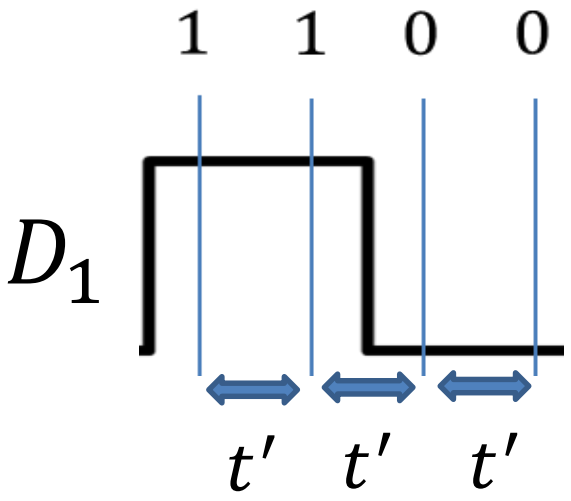


Fine time resolution

Long measurement time

Time Resolution of Proposed TDC

After overlap $(in\ case\ f_1 \approx f_2)$

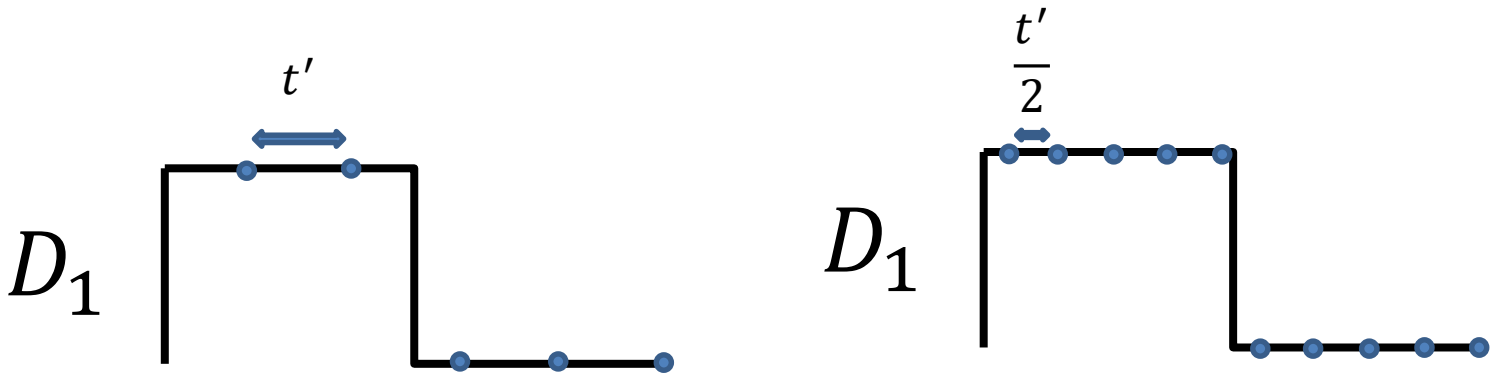


Time resolution = $t'[s]$

$$t' = \left|\frac{1}{f_2} - \frac{1}{f_1}\right| = \left|\frac{f_1 - f_2}{f_1 f_2}\right| \Rightarrow \lim_{f_1 \to f_2} t' = \text{Fine time resolution}$$

When $f_1 \approx f_2$, the number of n_{beat} increase

After overlap example

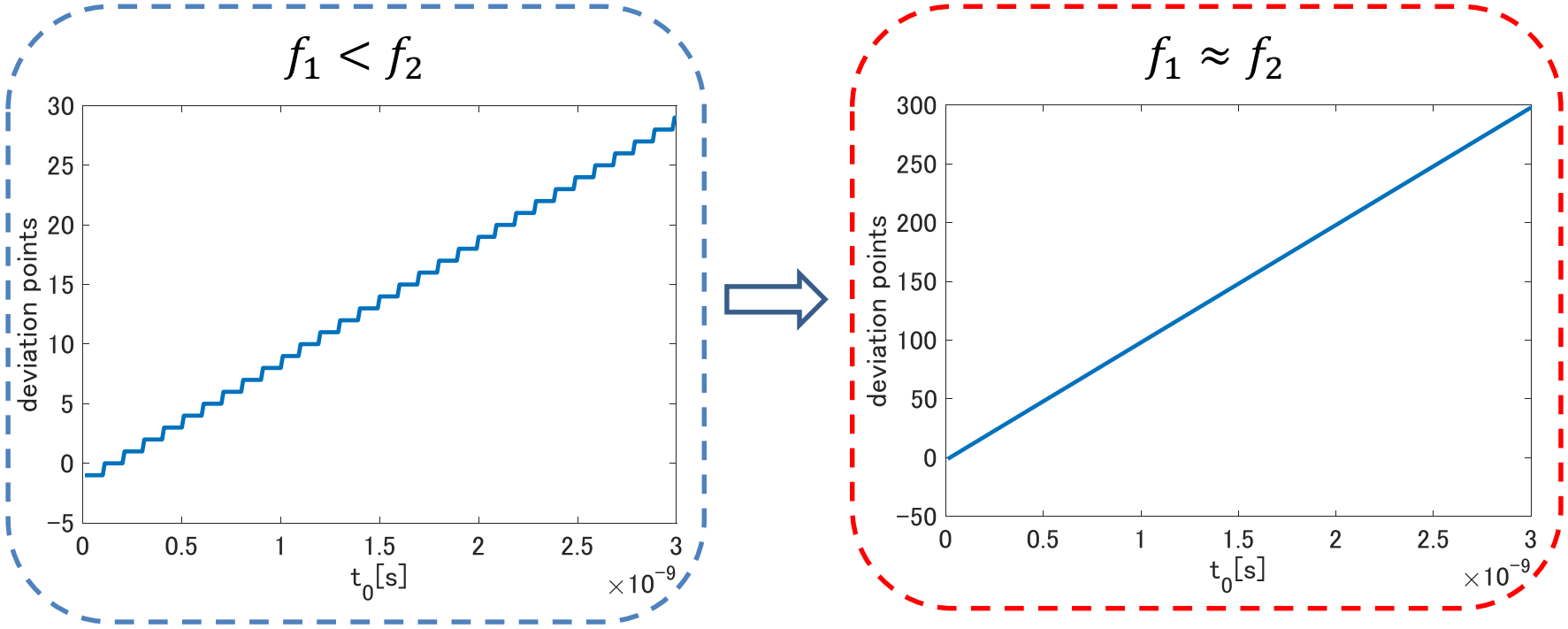


$n_{beat} = 5$ $\quad$ $n_{beat} = 10$

increase $n_{beat} \approx \frac{f_2}{|f_2 - f_1|} \Leftrightarrow f_1 \approx f_2$

Fine time resolution & High linearity

Linearity of Proposed TDC

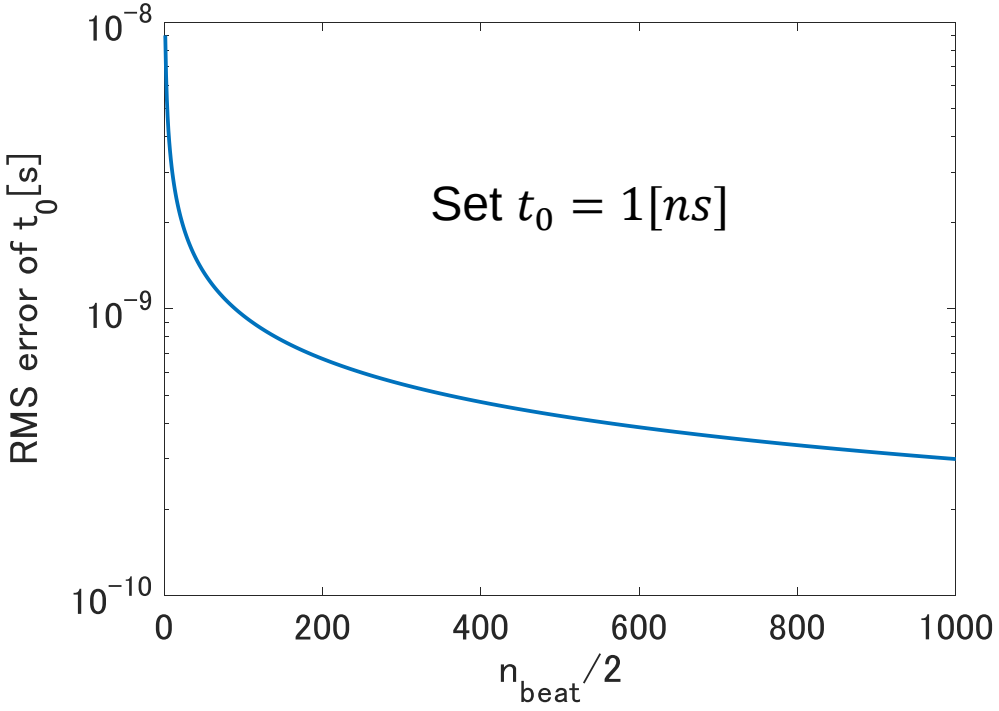


Low Linearity ⇒ High Linearity

RMS Error of Proposed TDC

Root Mean Squared (RMS) error of t_0 $= \sqrt{\frac{1}{n_{beat}/2}\sum_{i=1}^{n_{beat}/2}(t_i)^2}$

- t_i shows deviation between set t_0 and calculated t_0



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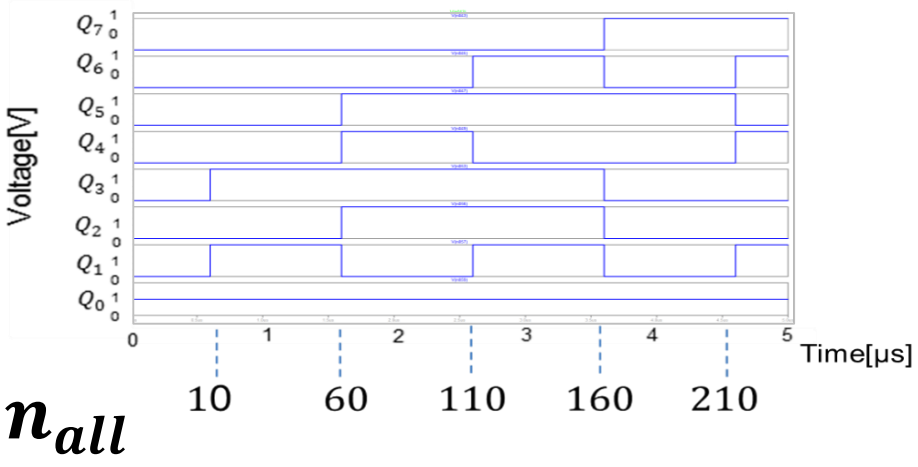
SPICE Simulation Verification of Proposed TDC

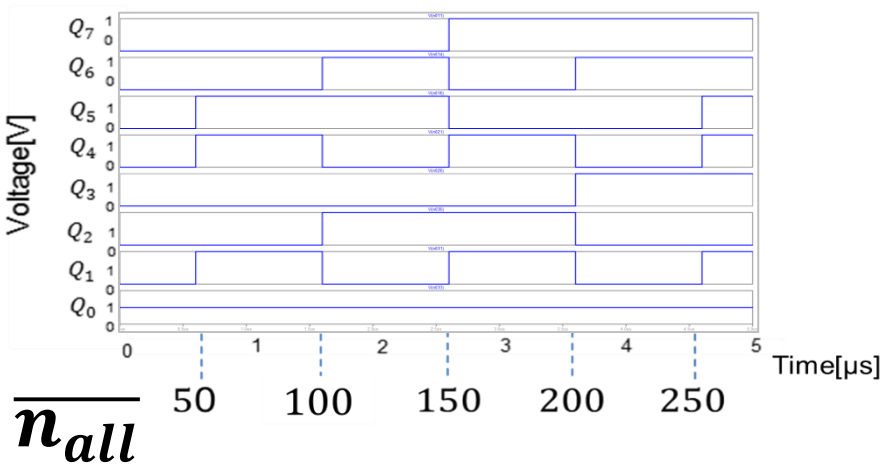
◆ Simulation Conditions

$$f_1 = 99[MHz], f_2 = 100[MHz], t_0 = 1[ns]$$

◆ SPICE Simulation Results



$\boldsymbol{n_{all}}$



$\overline{\boldsymbol{n_{all}}}$

At 5[μs] $\boldsymbol{n_{all} = 210}$, $\overline{\boldsymbol{n_{all}}} = \boldsymbol{250}$

⇨ $t_0 = 1.01$[ns] Error is **1**[%]

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Summary

◆TDC is proposed:

- Using asynchronous two sine waves
- With different frequencies
- No delay line
- No self-calibration required

Future task

◆Perform simulations of entire TDC including trigger circuits.

◆ Considering the case of t0 is larger than $1/(2f_1)$.

Thank you for your attention