Time-to-Digital Converter Architecture Using Asynchronous Two Sine Waves with Different Frequencies

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Outline

- Research Objective
- Proposed TDC Principle
- Individual Circuit
  - Trigger Circuit
  - Logic Circuit
- Resolution of Proposed TDC
- SPICE Simulation verification
- Conclusion
Outline

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Time-to-Digital Converter

- Time-to-digital converter (TDC) measures timing difference $t_0$ between $t_1$, $t_2$ and outputs as a digital value $D_{out}$
TDC Application Examples

Inter-vehicular distance measurement

Satellite distance measurement
# Comparison of TDC Architectures

<table>
<thead>
<tr>
<th></th>
<th>Conventional TDC</th>
<th>Proposed TDC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Circuit Architecture</strong></td>
<td><img src="image1.png" alt="Conventional TDC Circuit" /></td>
<td><img src="image2.png" alt="Proposed TDC Circuit" /></td>
</tr>
<tr>
<td><strong>Delay Array</strong></td>
<td>Necessary 🥟</td>
<td>Not necessary 😊</td>
</tr>
<tr>
<td><strong>Self Calibration</strong></td>
<td>Required 😞</td>
<td>Not required 😊</td>
</tr>
</tbody>
</table>

Delay array have **variations** → Self-calibration is required 😊
Comparison of frequencies

Same Frequencies

Clock frequency $\leq 1[GHz]$

$t' \geq \frac{1}{1[GHz]} = 1[ns]$

Different Frequencies

$t' = \left| \frac{1}{f_2} - \frac{1}{f_1} \right|$

example

$f_1 = 1[MHz]$  
$f_2 = 0.9999[MHz]$  

$t' \cong 0.1[ns]$  

Different frequencies $\rightarrow$ time resolution $\leftrightarrow$ measurement time  

Trade off
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Proposed TDC Architecture

Components

- Trigger Circuit × 2
- Logic Circuit × 4
- Logic Circuit × 1
Basic Operation of Logic Circuit

- $n_{\text{all}}(= n_1 + n_2 \ldots)$
- $\overline{n_{\text{all}}}(= \overline{n_1} + \overline{n_2} \ldots)$
- $n_{\text{beat}} \approx n_2 + \overline{n_2} = n_3 + \overline{n_3} = \ldots = \frac{f_2}{|f_2 - f_1|}$

Example d-flop

output

$Q$

input

$D_1$

$D_2$
How we calculate to timing difference $t_0$

- Proposed TDC Principle

$$t_0 = \text{deviation points} \times \text{one time difference}$$

Details

$$t_0 = \frac{n_{\text{beat}}}{2} - (\overline{n_{\text{all}}} - n_{\text{all}}) \times t'$$
Timing difference generates deviation points

\[ \text{deviation} = \left\{ \frac{n_{\text{beat}}}{2} - \left( \frac{n_{\text{all}}}{2} - n_{\text{all}} \right) \right\} \]

\[ = \left\{ \frac{n_2 + n_2}{2} - \left( \left( \frac{n_1 + n_2}{2} + \cdots \right) - \left( n_1 + n_2 + \cdots \right) \right) \right\} \quad \text{(in case } f_1 < f_2) \]
One deviation points means

One time difference $t'$ between $D_1$ and $D_2$

\[ t' = \left| \frac{1}{f_2} - \frac{1}{f_1} \right| \]

(=time resolution)
\( t_0 = \text{deviation points} \times \text{one time difference} \)

\[
t_0 = \begin{cases} 
(\overline{n_{all}} - n_{all})t' & \text{(in case } f_1 > f_2) \\
\{n_{beat}/2 - (\overline{n_{all}} - n_{all})\}t' & \text{(in case } f_1 < f_2) 
\end{cases}
\]
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Trigger Circuit Architecture & Operation

- Output starts to oscillate at rising timing edge of input
- Output waveform with no transient change
Track & Hold Circuit

Vin

Vout

Track

Hold

Track

Hold

Vout=Vin

Vout=Vc

SW

ON

SW

OFF

Track mode

Hold mode

Vin

Vc
Trigger Circuit’s Simulation Results

Sine waves of three-phase alternating

Trigger input

Output

track

hold

track

hold
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Logic Circuit Architecture

Components

\( D \quad Q \quad \bar{Q} \times \text{some} \)

\( \text{EN n bit counter} \times 2 \)
D-flop sampled D1 by clock D2

Example d-flop

output

\[ Q \]

input

\[ D_1 \]

\[ D_2 \]
Counter & Update

Output: Counter

Digital value

Output: Update
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Time resolution image

Sampling \( D_1 \) by clock \( D_2 \)

\[(in \ case \ f_1 \ll f_2)\]

Fine time resolution

\[(in \ case \ f_1 \approx f_2)\]

Coarse time resolution?
Overlapped outputs

\[ (in \ case \ f_1 \approx f_2) \]

\[ D_1 \]

\[ D_2 \]

\[ (in \ case \ f_1 \ll f_2) \]

Fine time resolution

Short measurement time

\[ 1/f_1 \]

\[ (in \ case \ f_1 \approx f_2) \]

Fine time resolution

Long measurement time

\[ 1/f_1 \]
After overlap (in case \( f_1 \approx f_2 \))

\[
D_1
\]

\[
t' = \left| \frac{1}{f_2} - \frac{1}{f_1} \right| = \left| \frac{f_1 - f_2}{f_1 f_2} \right|
\]

\[
\lim_{f_1 \rightarrow f_2} t' = \text{Fine time resolution}
\]
When $f_1 \approx f_2$, the number of $n_{\text{beat}}$ increase

After overlap example

$n_{\text{beat}} = 5$

$n_{\text{beat}} = 10$

increase $n_{\text{beat}} \approx \frac{f_2}{|f_2 - f_1|} \iff f_1 \approx f_2$

Fine time resolution & High linearity
Linearity of Proposed TDC

\[ f_1 < f_2 \]

Low Linearity

\[ f_1 \approx f_2 \]

High Linearity
Root Mean Squared (RMS) error of $t_0 = \sqrt{\frac{1}{n_{\text{beat}/2}} \sum_{i=1}^{n_{\text{beat}/2}} (t_i)^2}$

- $t_i$ shows deviation between set $t_0$ and calculated $t_0$

Set $t_0 = 1[ns]$
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SPICE Simulation Verification of Proposed TDC

◆ Simulation Conditions

\[ f_1 = 99\,[MHz], \, f_2 = 100\,[MHz], \, t_0 = 1\,[ns] \]

◆ SPICE Simulation Results

At 5[\mu s] \, n_{all} = 210, \, \overline{n_{all}} = 250

\[ t_0 = 1.01\,[ns] \quad \text{Error is} \, 1\,[\%] \]
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Summary

◆ TDC is proposed:
  - Using asynchronous two sine waves
  - With different frequencies
  - No delay line
  - No self-calibration required

Future task

◆ Perform simulations of entire TDC including trigger circuits.
◆ Considering the case of t0 is larger than \(1/(2f_1)\).
Thank you for your attention