*International Conference on Mechanical, Electrical and Medical Intelligent System 2017*
**Invited**

# A Low Switching Loss 40 V Dual RESURF LDMOS Transistor with Low Specific On-Resistance

Jun-ichi Matsuda, Jun-ya Kojima, Nobukazu Tsukiji,
Masataka Kamiyama, and Haruo Kobayashi
Gunma University

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# Outline

1. Objective and Background
2. Conventional and Proposed LDMOS Transistor Structures
3. Simulation Results
   - Electric characteristics
     - $I_{DS}$-$V_{DS}$, Breakdown, Specific on-resistance vs. breakdown voltage
   - Hot carrier endurance
   - Total power dissipation
4. Summary

Simulation: 3D device simulator **Advance/DESSERT** developed by AdvanceSoft Corporation

# Objective and Background

**Objective:**

- To obtain a 40 V LDMOS transistor for automotive applications to meet the requirements for **(1) high hot carrier endurance, (2) wide SOA, (3) low specific on-resistance, and (4) low switching loss**

**Uses of LDMOS transistors:**

- 40 V LDMOS transistors are widely used as switching devices of power converters for automotive as well as consumer applications.
- Automotive applications have to meet the above requirements under **harsh environments**.

**Conventional device:**

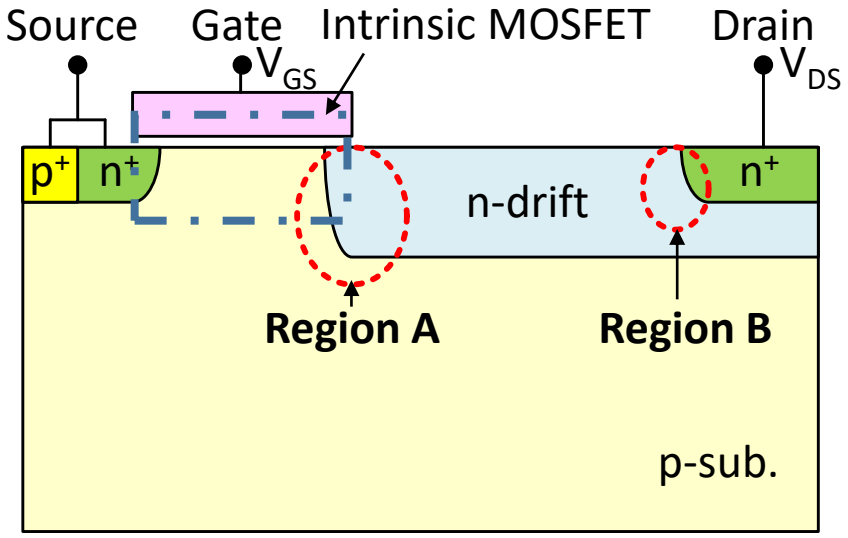
- We proposed a dual RESURF 30-50 V LDMOS transistor to improve a basic LDMOS transistor in 2015.
- This device meets the requirements of **(1) high hot carrier endurance, (2) wide SOA, and (3) low specific on-resistance**.
- However it does not meet the requirement of **(4) low switching loss**.

**Proposed device:**

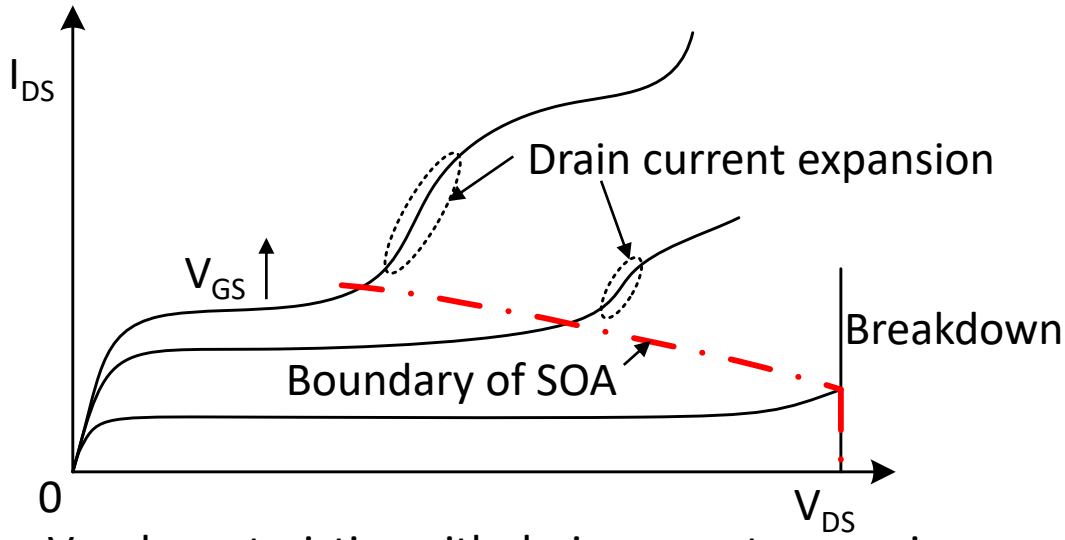
- **We have further improved the conventional device to reduce the switching loss.**

Note: SOA (safe operating area), RESURF (reduced surface field)

# Problems of a Basic LDMOS Transistor




A cross-section of a basic n-LDMOS transistor




$I_{DS}$-$V_{DS}$ characteristics with drain current expansion

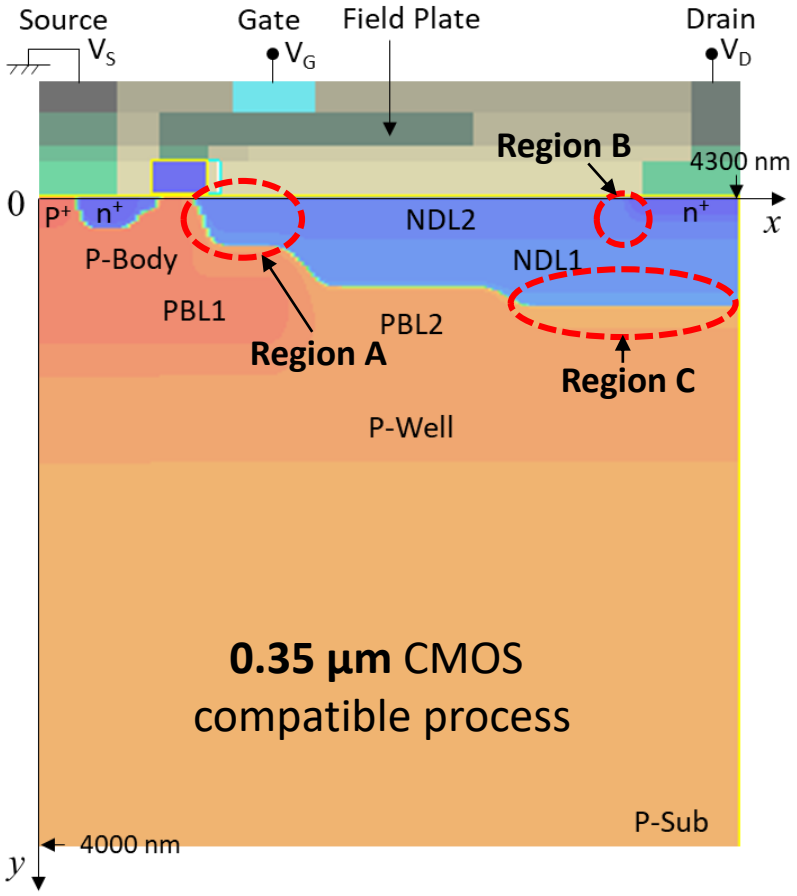
**Problems**

(1) **Low hot carrier endurance** due to **DAHC** (drain avalanche hot carriers)
⇒ Caused by a high electric field in **Region A**

(2) **Drain current expansion (CE) leading to a narrow SOA**
⇒ Caused by a high electric field in **Region B due to Kirk effect**

(3) **High specific on-resistance**
⇒ Caused by a low impurity concentration in the n-drift region

# Conventional LDMOS Transistor Structure




Cross-section of the conventional device
(One cell size: 3.725 µm × 0.3 µm)

■ P-buried Layers (**Dual RESURF** Structure)

- PBL1: Enhances the RESURF effect in **Region A, leading to high hot carrier endurance**
- PBL2: ① Causes a uniform electric field in the drift region
  ② Avoids premature breakdown in **Region C**

■ N-drift Layers

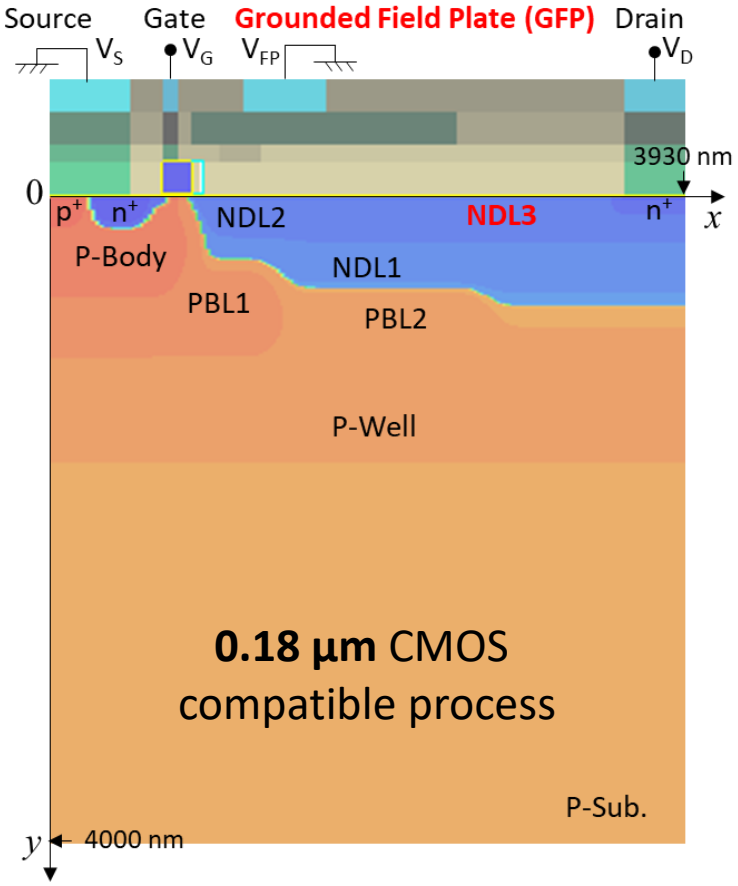
- NDL1: The basic layer of the drift region
- NDL2: **Reduces specific on-resistance and suppresses CE due to a low electric field in Region B**

■ Field Plate (**connected to the gate**)

- Complements the RESURF effect in the drift region
- **Increases the Miller capacitance, leading to a large switching loss**

**Reduction of the switching loss is required.**

# Proposed LDMOS Transistor Structure



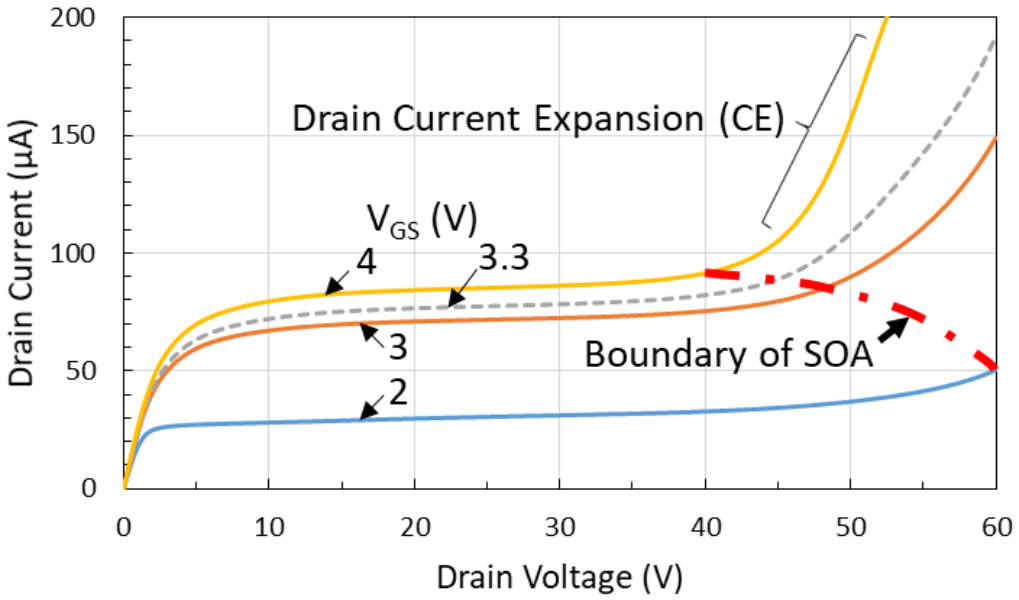

Cross-section of the proposed device
(One cell size: 3.555 µm × 0.3 µm)

■ P-buried Layers (Dual RESURF Structure)
- PBL1 and PBL2: Same as the conventional device

■ N-drift Layers
- NDL1 and NDL2: Same as the conventional device
- **NDL3: Reduces specific on-resistance and suppresses CE**
  (Needed to reduce the specific on-resistance increased by GFP)

■ Field Plate (**connected to the ground**): **GFP**
- Complements the RESURF effect in the drift region
- **Reduces the Miller capacitance, leading to a smaller switching loss**

# $I_{DS}$ - $V_{DS}$ Characteristics of the Proposed Device




Drain current $I_{DS}$ vs. drain voltage $V_{DS}$
(one cell)

■SOA excluding CE region

$V_{DS} \leqq 40V$ at $V_{GS} = 4V$（maximum gate voltage rating）

$V_{DS} \leqq 45V$ at $V_{GS} = 3.3V$（gate operation voltage）

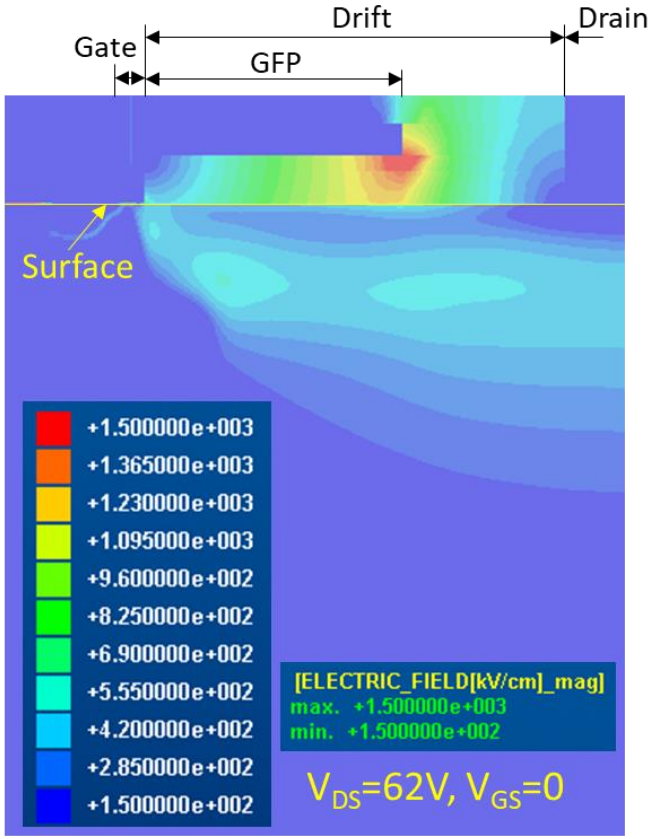
⇒ **Wide SOA enough for 40 V operation**

■Specific on-resistance (Linear region)

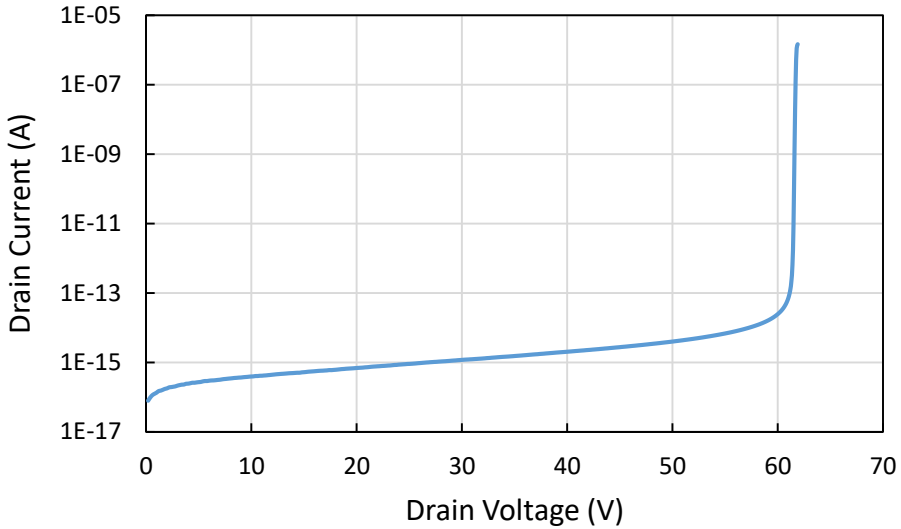
$R_{on}A = 40.9\ m\Omega \cdot mm^2$ at $V_{GS} = 3.3V$（the proposed device）

Cf. $R_{on}A = 44.8\ m\Omega \cdot mm^2$ at $V_{GS} = 5V$ (the conventional device)

# Breakdown Characteristics of the Proposed Device




Electric field distribution upon breakdown



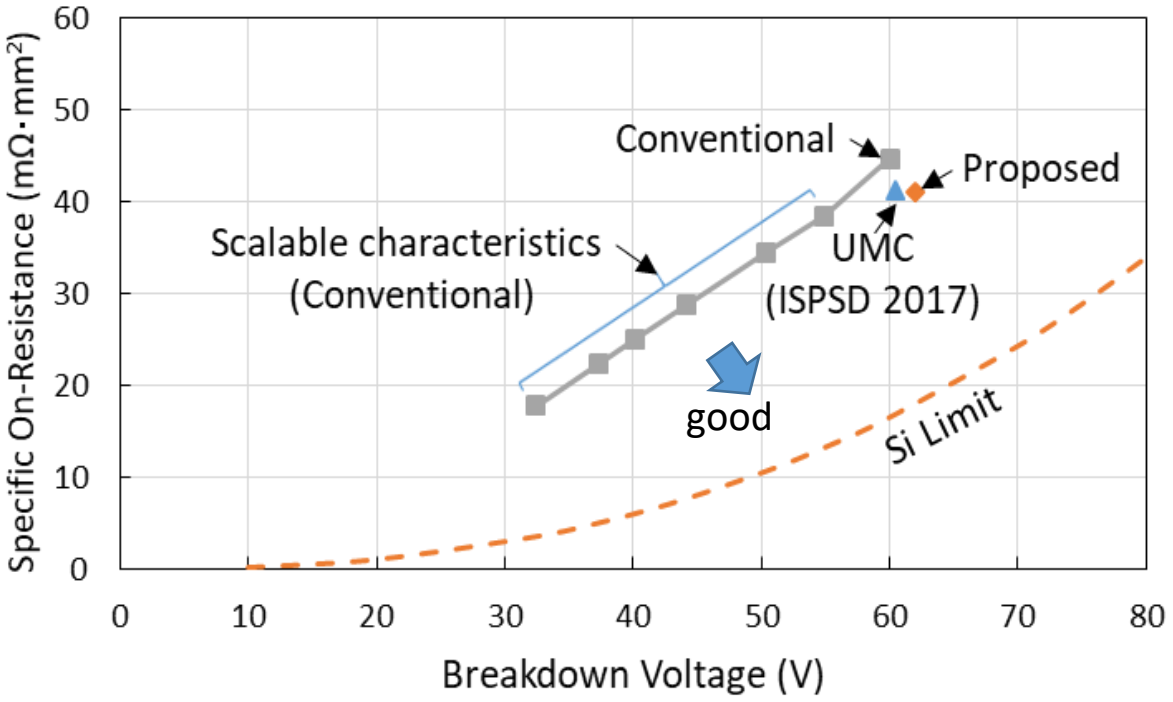

An $I_{DS}$–$V_{DS}$ characteristic at $V_{GS}$=0 V (one cell)

- Breakdown voltage $BV_{DS}$ = 62 V
  ⇒ **High enough for 40 V operation**
- High electric field regions upon breakdown
  ⇒ All in the **bulk** (The breakdown location is in the bulk.)

**The proposed device would have a good ESD performance.**

Note: ESD (electro static discharge)

# $R_{on}A$ - $BV_{DS}$ Characteristics

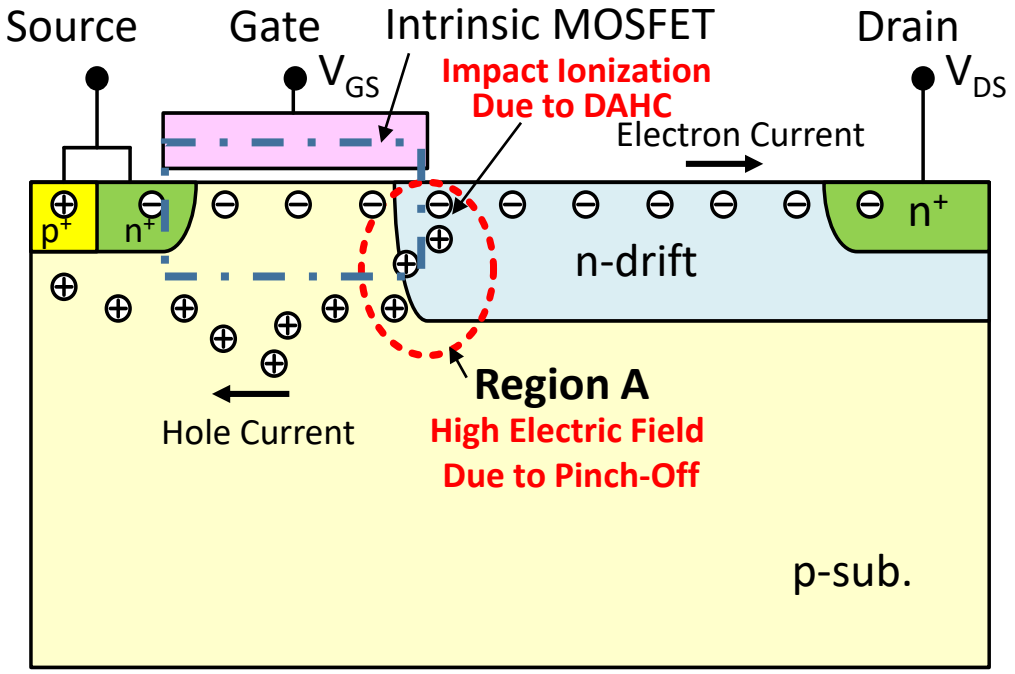



$R_{on}A$ – $BV_{DS}$ Characteristics

■ $R_{on}A$ - $BV_{DS}$ of the proposed device
⇒ Almost the same as
that of UMC presented at ISPSD2017
⇒ **State-of-the-art level**

Note: In this simulation, contact and wiring resistances are not considered.

# Hot Carrier Endurance



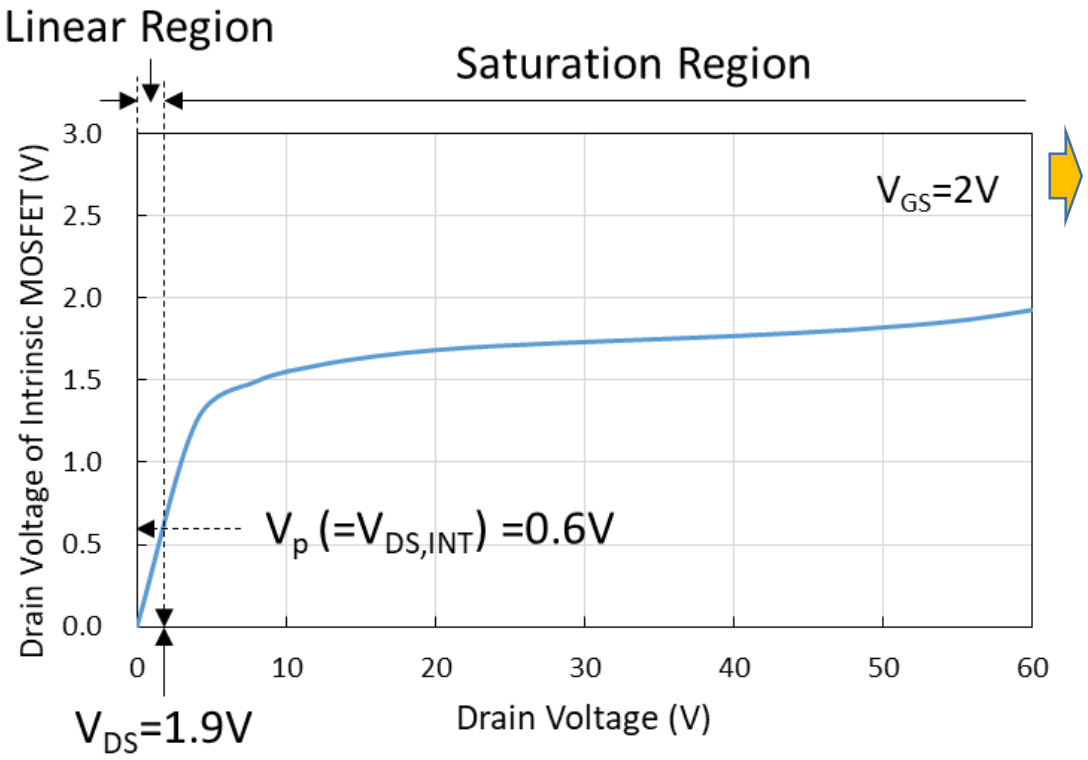

Mechanism of hot carrier generation in an LDMOS transistor

- Hot carriers generated in **Region A** by impact ionization
  ⇒ Cause damage to intrinsic MOSFET characteristics

- Large degradation of hot carrier endurance
  ⇒ Occurs when the intrinsic MOSFET is in the saturation state by **pinch-off** at a low gate voltage, in this case $V_{GS} \fallingdotseq 2$ V.

**Let us go over if the saturation state of the intrinsic MOSFET biased at $V_{GS}$ = 2 V is due to pinch-off.**

# Drain voltage of the intrinsic MOSFET $V_{DS,INT}$ vs. $V_{DS}$



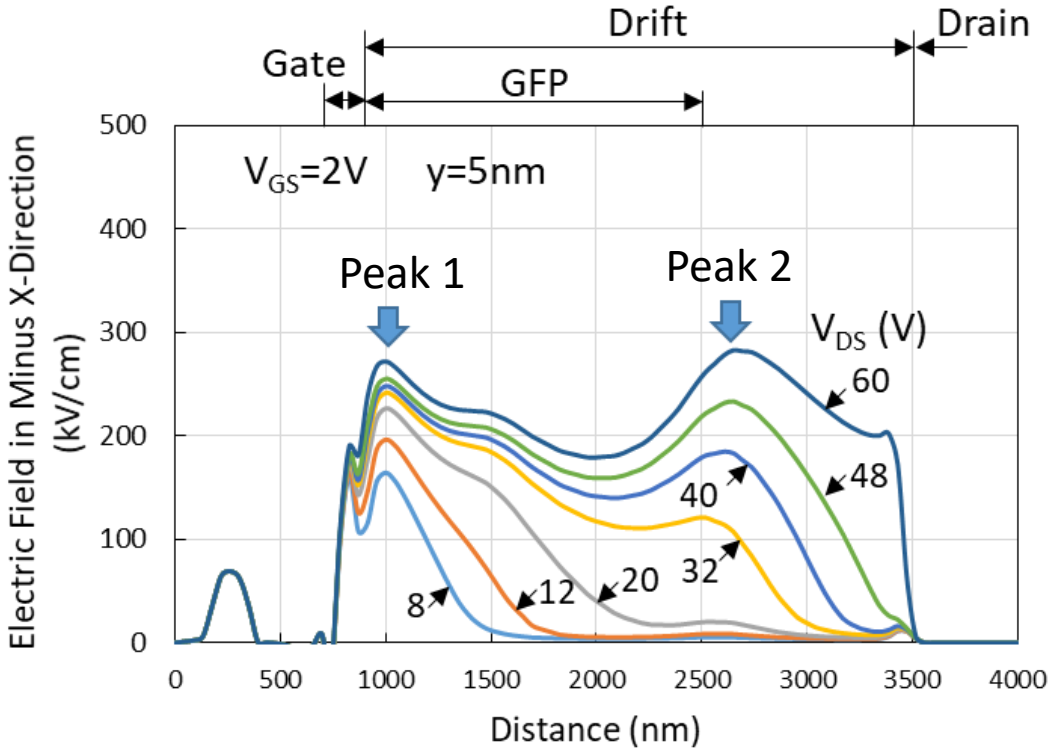

Drain voltage of the intrinsic MOSFET **$V_{DS,INT}$** vs. **$V_{DS}$**

- The pinch-off voltage of the intrinsic MOSFET $V_p$ at $V_{GS}$=2V
  - ⇒ **$V_p$ (=$V_{DS,INT}$) =0.6V** (from the calculation)
  - ⇒ **Corresponds to $V_{DS}$=1.9V** (from the left Figure)
- The saturation voltage $V_{DSAT}$ at $V_{GS}$=2V
  - ⇒ **$V_{DSAT}$(=$V_{DS}$)≒2V** (from $I_{DS}$ – $V_{DS}$ characteristics)
- The saturation state of the intrinsic MOSFET at $V_{GS}$ = 2 V
  - ⇒ Due to **pinch-off**.

**Hot carrier endurance**

**might degrade in this saturation state.**

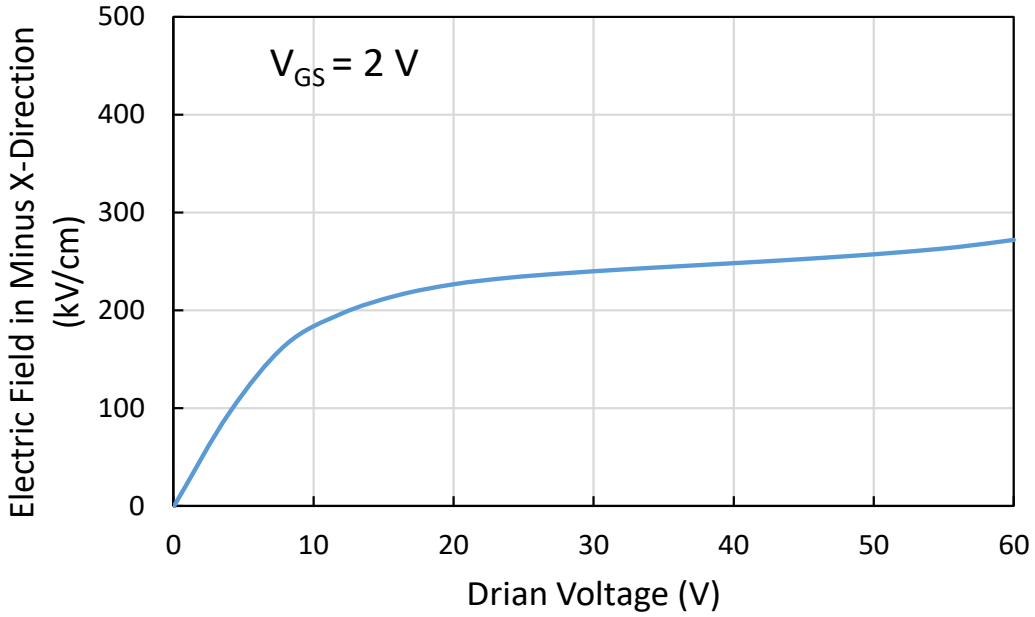
# Profiles of the Electric Field in the X-Direction along the Surface $E_x$ for the Proposed Device




The dependence of $E_x$ profiles on $V_{DS}$

- $E_x$ profiles have mainly two peaks
  - (1) **Peak 1:** at $x \fallingdotseq 1000$nm (near drain-side gate edge)
  - (2) **Peak 2:** for $2500\ \text{nm} \leqq x \leqq 2700\ \text{nm}$ (near GFP edge)
  - ⇒ **Increase with increasing $V_{DS}$**

# $V_{DS}$ Dependence of $E_x$ at x=1000 nm (Peak 1)

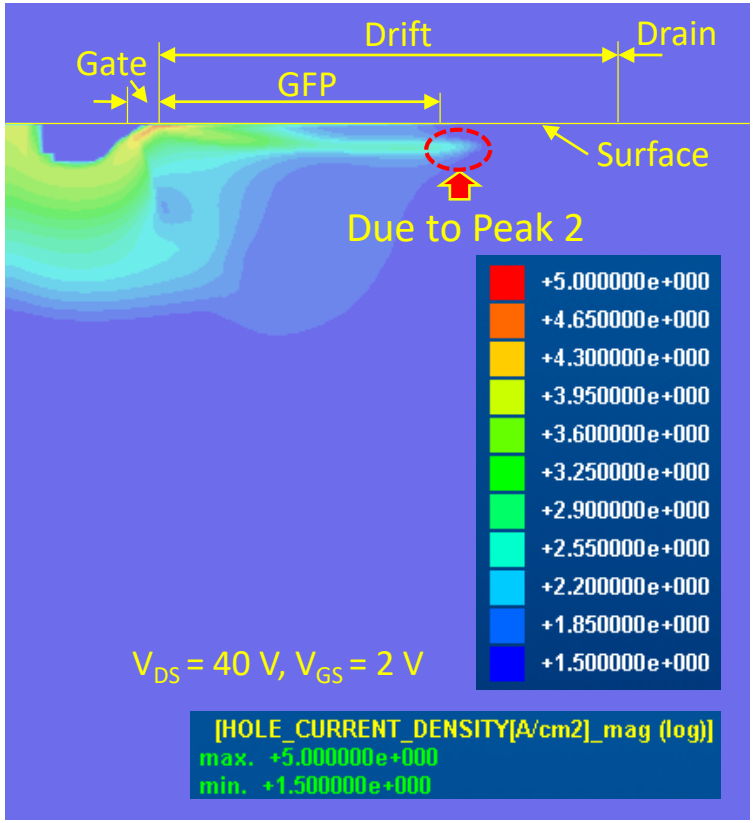



$V_{DS}$ Dependence of $E_x$ at x=1000 nm (Peak 1)

- $E_x$ at x=1000 nm (**Peak 1**)
  ⇒**Tends to saturate** with increasing $V_{DS}$ due to the RESURF effect enhanced by **PBL1**

**The proposed device would likely be able to have high hot carrier endurance.**

# Hole Current Density Distribution (Peak 2)



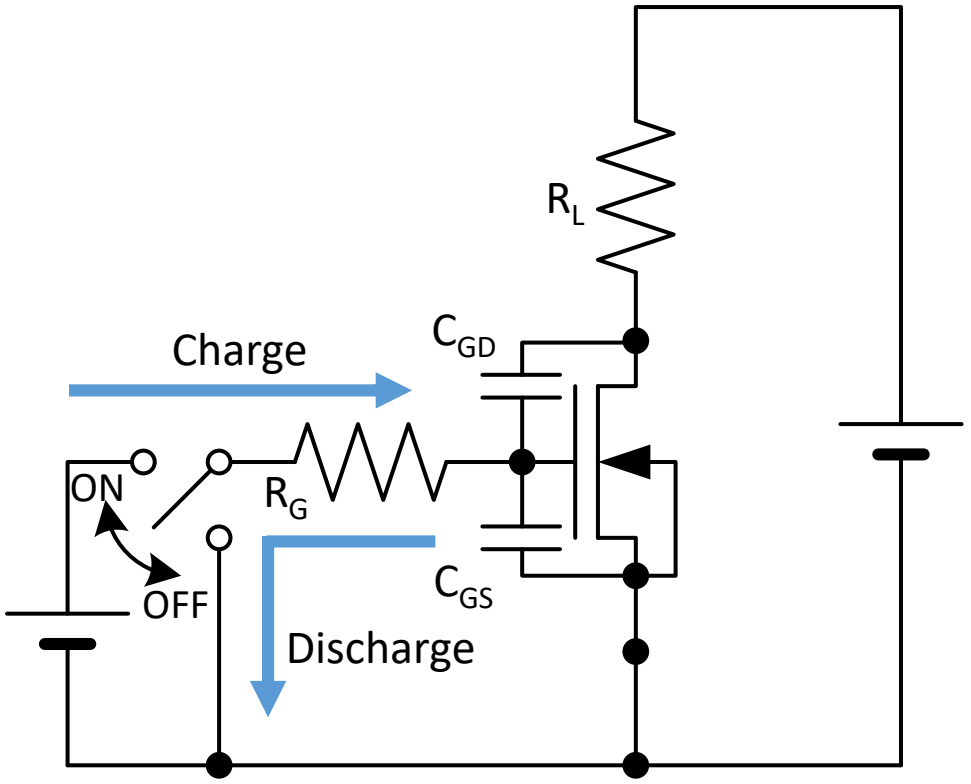

Hole current density distribution
due to impact ionization at $V_{DS}$=40V, $V_{GS}$=2V

■ $E_x$ for 2500 nm ≦ x ≦ 2700 nm (**Peak 2**)
⇒Largely increases with increasing $V_{DS}$ for $V_{DS}$≧20 V

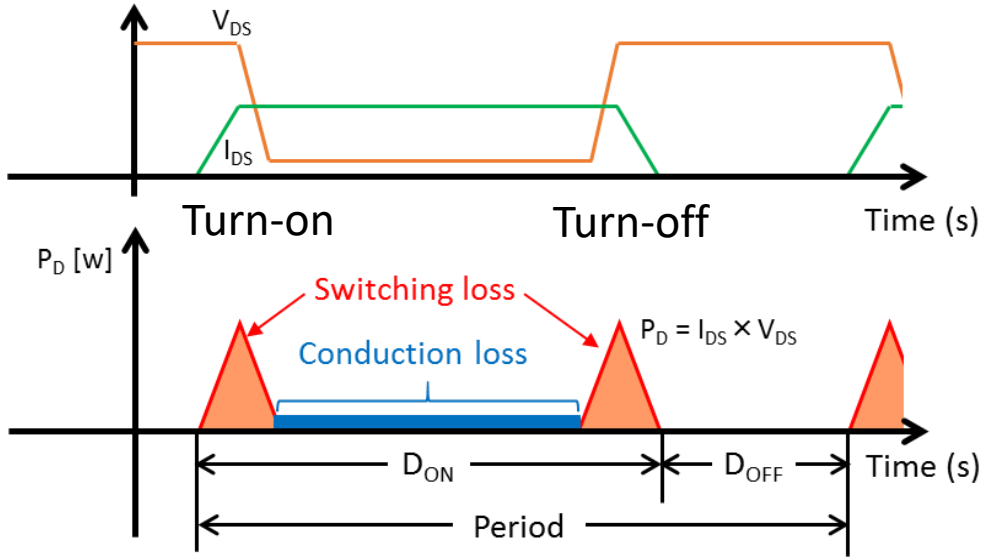
■ High hole current density due to Peak 2
⇒ Occurs in the bulk

**Peak 2 would cause no damage to the surface and the intrinsic MOSFET.**

# Total Power Dissipation




Gate charge during turn-on and gate discharge during turn-off




Switching and conduction losses

■ Total power dissipation consists of

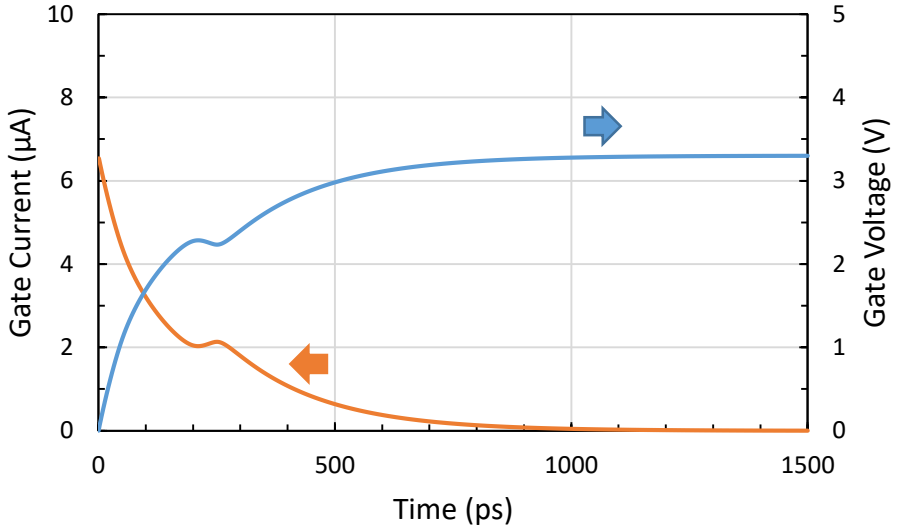
(1) Gate driving loss due to charging and discharging the gate capacitances ($C_{GS}$ and $C_{GD}$) through $R_G$

(2) Switching loss during turn-on and turn-off

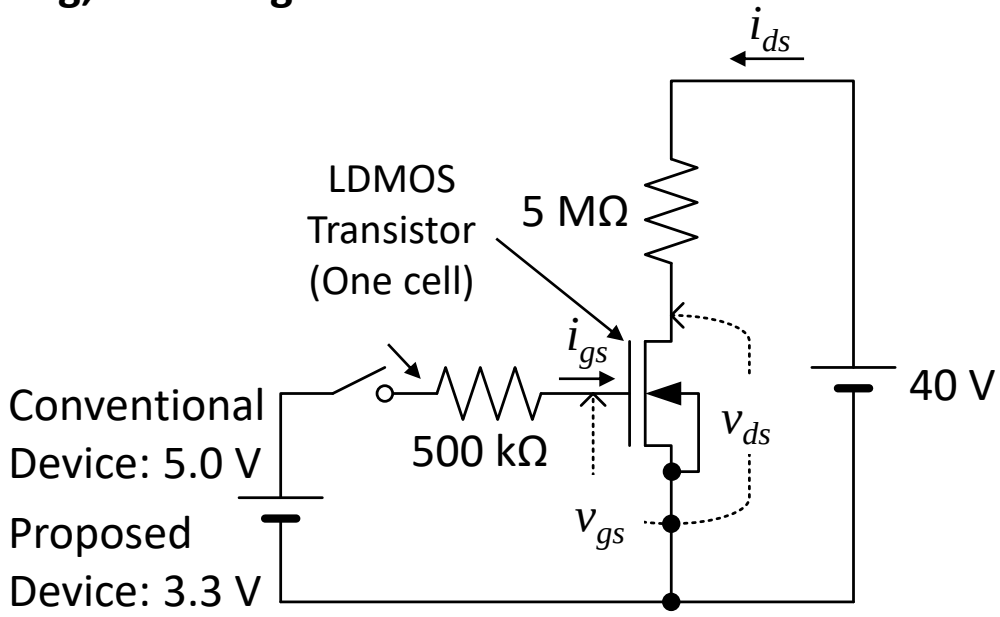
(3) Conduction loss

# FOM of the Proposed Device

**FOM ($R_{on}A \cdot Q_g/A$) represents performance for gate driving, switching and conduction losses.**




Turn-on characteristics of the gate current and the gate voltage (one cell)




The circuit used to obtain turn-on characteristics

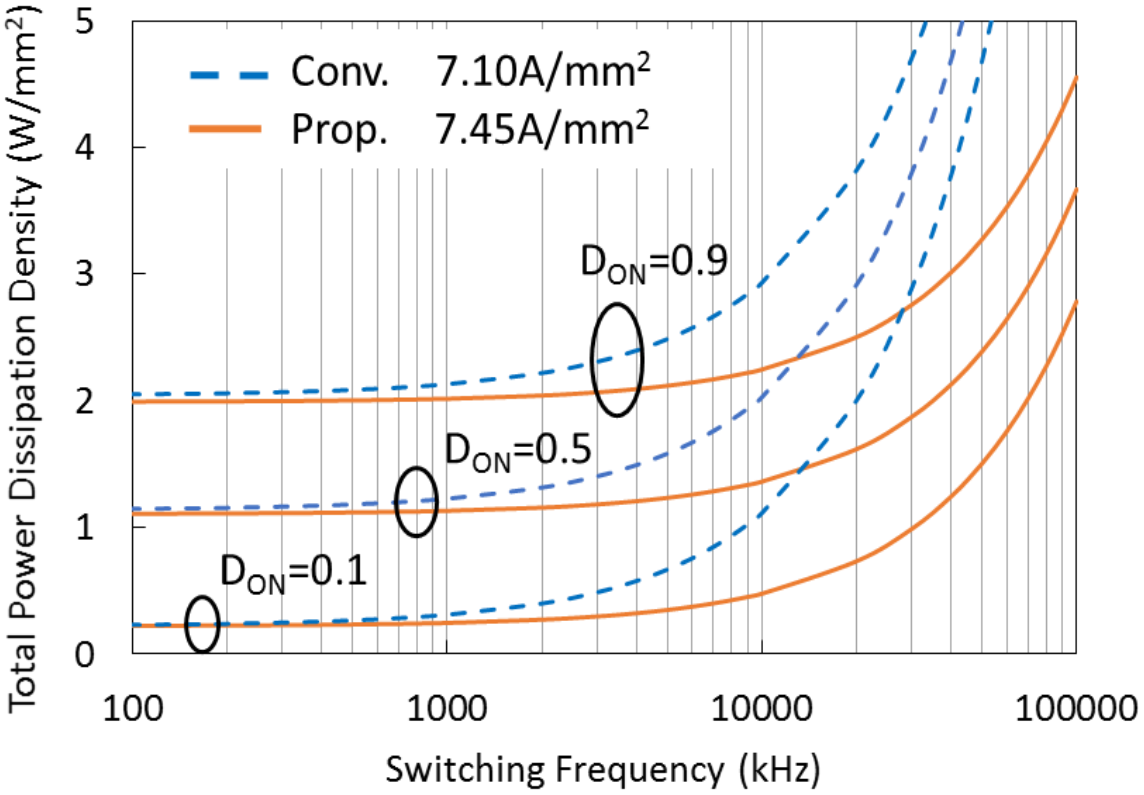
■Gate charge density ($Q_g/A$) = 1.18 nC/mm$^2$, Cf. $Q_g/A$ = 3.13 nC/mm$^2$ (the conventional device)

⇒ **The gate driving and switching losses of the proposed device are much lower than those of the conventional device.**

■FOM = 48.2 mΩ·nC ⇒ **About 1/3 that of the conventional device** (=141 mΩ·nC)

⇒ **The total power dissipation of the proposed device is much lower than that of the conventional device.**

# Switching Frequency Dependence of the Total Power Dissipation Density




Switching frequency dependence of the total power dissipation density $P_{DT}$

■ **f ≦ 1 MHz**

**$P_{DT}$ (Conventional) ≒ $P_{DT}$ (Proposed)**

■ **f > 1 MHz**

**$P_{DT}$ (Conventional) > $P_{DT}$ (Proposed)**

**$P_{DT}$ of the proposed device is much lower than that of the conventional device with increasing the switching frequency.**

**As for DC-DC converters using LDMOS transistors as the switching devices, a range of the switching frequency is usually from 1 MHz to several MHz. In this range, the proposed device is superior to the conventional device.**

# Summary

**The proposed 40 V LDMOS transistor**

- Has **much lower total power dissipation density (or gate driving and switching losses)** than the conventional device with increasing the switching frequency
- Has a **state-of-the-art level characteristic** for specific on-resistance vs. breakdown voltage
- Has **a wide SOA** enough for 40 V operation
- would likely be able to have **high hot carrier endurance**
- **Adequate for harsh environment automotive applications**

# Acknowledgement

We would like to express sincere thanks to AdvanceSoft Corporation for lending us 3D TCAD simulator.

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**Thank you very much for your kind attention.**