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Special Session Paper

# Innovative Practices Session 10B
# Innovative Practices in Asia -2: From Cost Perspective

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## I. Optical Interconnection Test Method

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Drastically increasing network traffic within datacenters requires high volume manufacturing of 100-Gb/s optical transceivers. This paper proposes a high throughput test method for optical transceivers using Automated Test Equipment (ATE) with both an optical and an electrical frontend. By using the proposed solution >4x higher throughput can be achieved. We also will report on a non-contact optical contactor we developed for high volume manufacturing that enables 100k times contact without replacement.

## II. Signal Generation with Specified Harmonics Suppression Using Only Single Digital Output Pin

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Advantest Corporation

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Gunma Univ.

This talk will describe single-tone and two-tone signal generation techniques with suppression of specified HDs and IMDs, using only single digital output pin of ATE. Their algorithms, simulation and experimental results as well as possible applications will be explained.

## III. A Practical and Cost Effective Approach for 2.5D FPGA-Transceiver EMIB Testing

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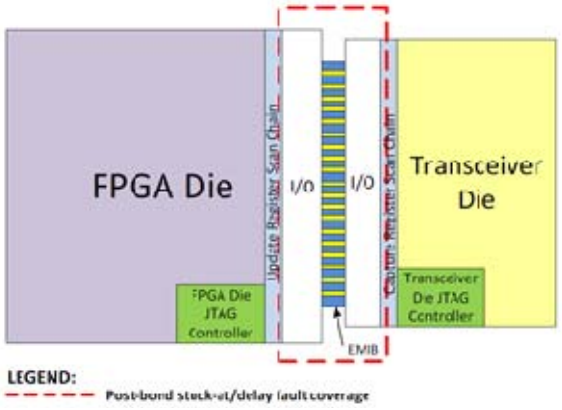
Semiconductor industry has been putting tremendous efforts on 2.5D technology in accordance with the increasing demand for better capacity and system performance. This technology enables several dies to communicate up to the speed of Gigabits per second while reducing the cost for a system with heterogeneous components. However, such new technology also poses great challenges whereby the manufacturing of this interconnect structure is a complicated and defect-prone process. Therefore, the success of 2.5D is greatly dependent on Design for Testability (DFT) to ensure excellence in product quality and reliability as well as keeping the yield loss and overall cost low.

This paper introduces a practical and cost-effective test methodology on Intel's patented, state-of the-art Embedded Multi-Die Interconnect Bridge (EMIB) that can be adopted by 2.5D FPGA/transceiver product which is made possible based on extension to the IEEE1149.1 Standard together with Automated Test Pattern Generator (ATPG) methodology. This fault testing methodology is tailored for the post-bond testing. The test is able to detect physical defects in the EMIB, such as missing micro-bumps or misalignments between dies, micro-bumps and the interconnect bridge. However, in complex nanometer design nowadays, defects not only can arise during the process of die bonding and assembly, process variation is found to be one of the main contribution to defects as well. Therefore, in order to ensure maximum test coverage on EMIB, stuck-at test and at-speed test is conducted to target different kind of defects including shorts, opens and delay faults.




This test methodology is proven reliable with the simulation results showing that various defects can be detected and diagnosed effectively using the proposed methods. Besides, the boundary scan cell proposed here utilizes only half of the registers required by the standard boundary scan cells thus reduces the die area by 50%.

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