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Fibonacci Sequence Weighted SAR ADC as Golden Section Search

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K. Asami, H. Kobayashi



Kobayashi
Laboratory

Gunma University



OUT LINE

- Introduction
- SAR ADC & Redundancy Design
- Golden Section Search & Fibonacci Search
- Fibonacci Sequence Weighted SAR ADC
- SAR ADC Based on Fibonacci Search
- Proof & Simulation
- Conclusion

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Background



Automotive electronics are in spotlight



High-speed, Reliable

“SAR ADC” in microcontroller is needed.

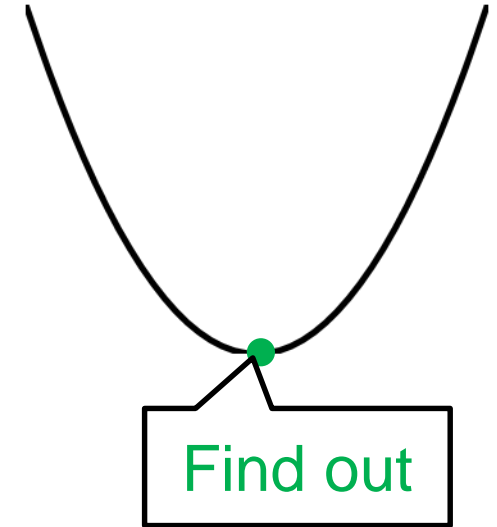
In my laboratory _____

We have discovered various properties of SAR ADC using **Fibonacci sequence**.

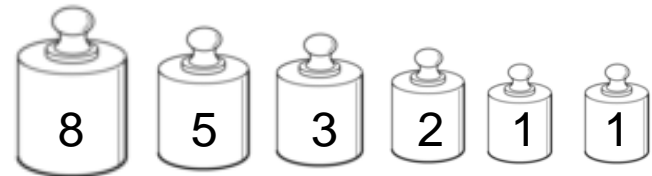
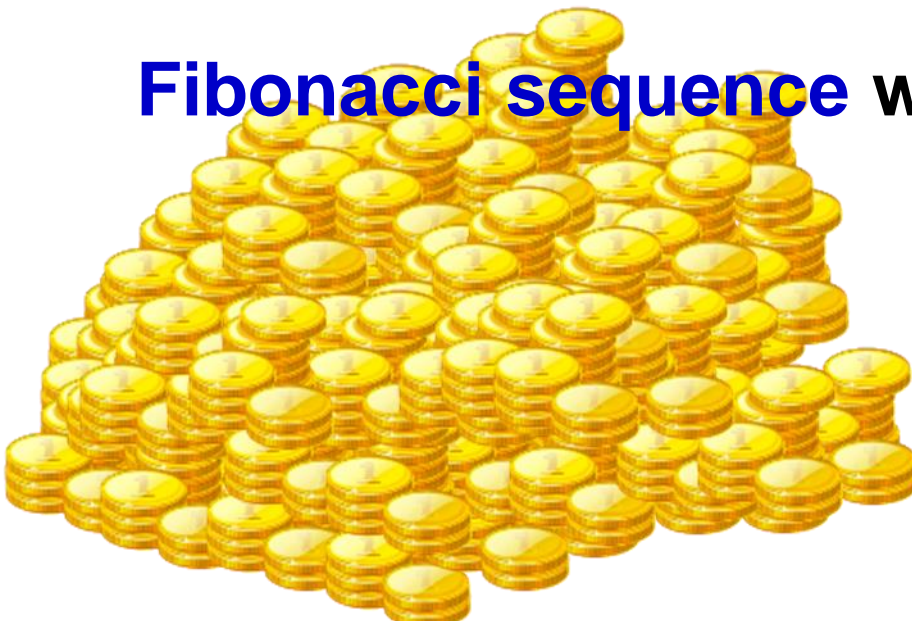
New Discovery

SAR ADC based on
golden section search
using unimodal function

 **equivalent**



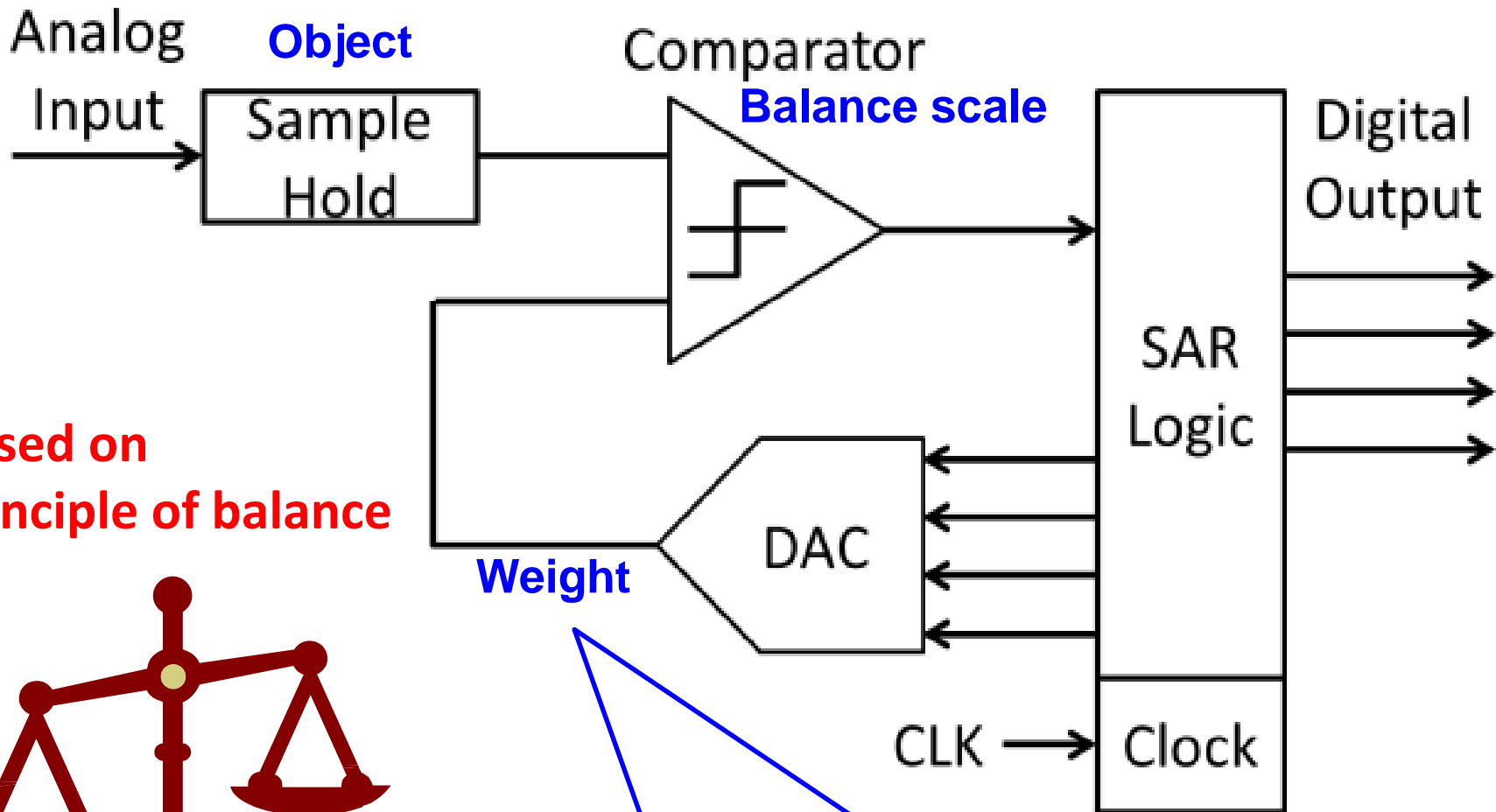
Fibonacci sequence weighted SAR ADC



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SAR ADC Configuration



Based on principle of balance



Generally use binary weight
(1, 2, 4, 8, 16, 32, 64 ...)

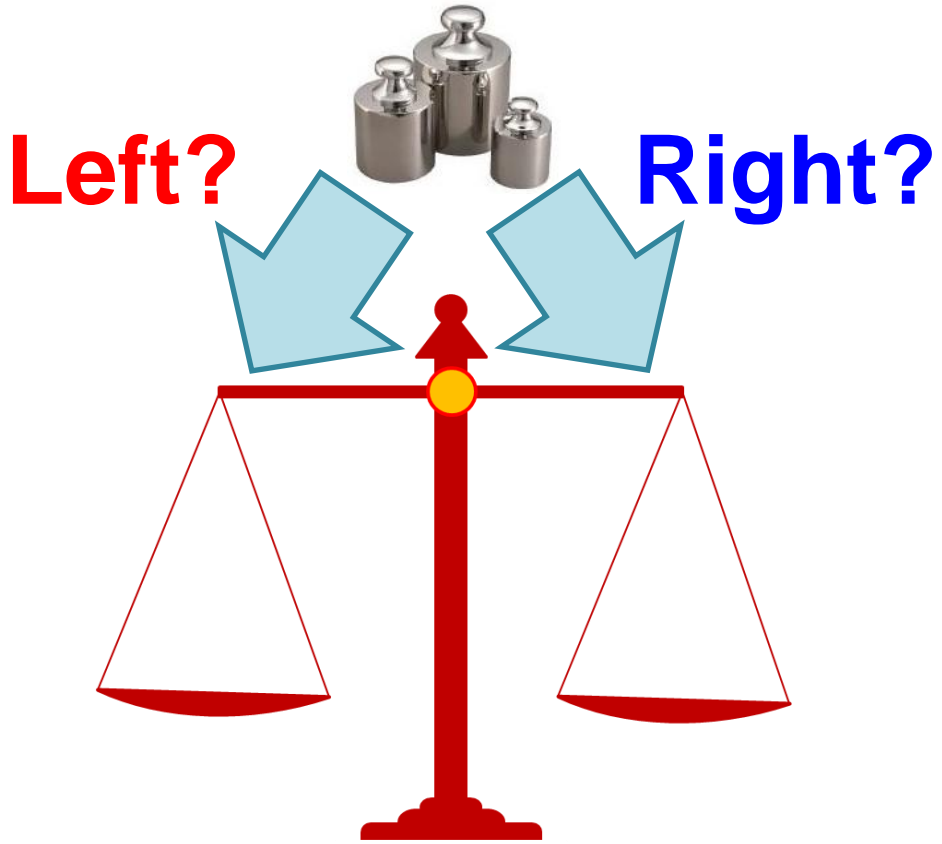


Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input: 7.3 [V]
- Binary weight :

16, 8, 4, 2, 1



| Step | 1st | 2nd | 3rd | 4th | 5th | output |
|-------------|-----|-----|-----|-----|-----|--------|
| Weight p(k) | 16 | 8 | 4 | 2 | 1 | |
| 31 | | | | | | 31 |
| 30 | | | | | | 30 |
| 29 | | | | | | 29 |
| 28 | | | | | | 28 |
| 27 | | | | | | 27 |
| 26 | | | | | | 26 |
| 25 | | | | | | 25 |
| 24 | | | | | | 24 |
| 23 | | | | | | 23 |
| 22 | | | | | | 22 |
| 21 | | | | | | 21 |
| 20 | | | | | | 20 |
| 19 | | | | | | 19 |
| 18 | | | | | | 18 |
| 17 | | | | | | 17 |
| 16 | | | | | | 16 |
| 15 | | | | | | 15 |
| 14 | | | | | | 14 |
| 13 | | | | | | 13 |
| 12 | | | | | | 12 |
| 11 | | | | | | 11 |
| 10 | | | | | | 10 |
| 9 | | | | | | 9 |
| 8 | | | | | | 8 |
| 7 | | | | | | 7 |
| 6 | | | | | | 6 |
| 5 | | | | | | 5 |
| 4 | | | | | | 4 |
| 3 | | | | | | 3 |
| 2 | | | | | | 2 |
| 1 | | | | | | 1 |
| 0 | | | | | | 0 |

Level



Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input: 7.3 [V]
- Binary weight :

8, 4, 2, 1



Right



| Step | 1st | 2nd | 3rd | 4th | 5th | output |
|-------------|-----|-----|-----|-----|-----|--------|
| Weight p(k) | 16 | 8 | 4 | 2 | 1 | |
| 31 | | | | | | 31 |
| 30 | | | | | | 30 |
| 29 | | | | | | 29 |
| 28 | | | | | | 28 |
| 27 | | | | | | 27 |
| 26 | | | | | | 26 |
| 25 | | | | | | 25 |
| 24 | | | | | | 24 |
| 23 | | | | | | 23 |
| 22 | | | | | | 22 |
| 21 | | | | | | 21 |
| 20 | | | | | | 20 |
| 19 | | | | | | 19 |
| 18 | | | | | | 18 |
| 17 | | | | | | 17 |
| 16 | | | | | | 16 |
| 15 | | | | | | 15 |
| 14 | | | | | | 14 |
| 13 | | | | | | 13 |
| 12 | | | | | | 12 |
| 11 | | | | | | 11 |
| 10 | | | | | | 10 |
| 9 | | | | | | 9 |
| 8 | | | | | | 8 |
| 7 | | | | | | 7 |
| 6 | | | | | | 6 |
| 5 | | | | | | 5 |
| 4 | | | | | | 4 |
| 3 | | | | | | 3 |
| 2 | | | | | | 2 |
| 1 | | | | | | 1 |
| 0 | | | | | | 0 |

Down!

Level

0

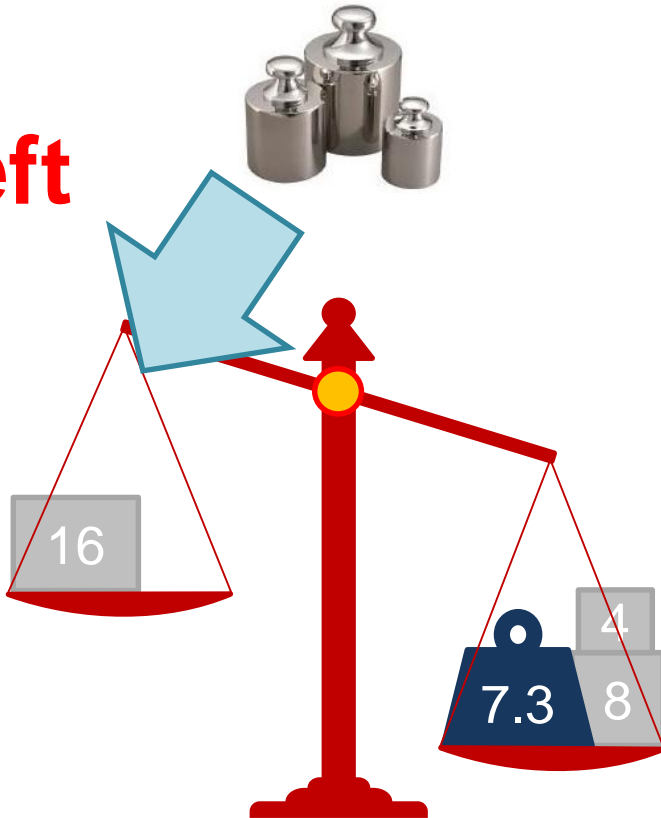
Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input: 7.3 [V]
- Binary weight :

2, 1

Left



| Step | 1st | 2nd | 3rd | 4th | 5th | output |
|-------------|-----|-----|-----|-----|-----|--------|
| Weight p(k) | 16 | 8 | 4 | 2 | 1 | |
| 31 | | | | | | 31 |
| 30 | | | | | | 30 |
| 29 | | | | | | 29 |
| 28 | | | | | | 28 |
| 27 | | | | | | 27 |
| 26 | | | | | | 26 |
| 25 | | | | | | 25 |
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| 8 | | | | | | 8 |
| 7 | | | | | | 7 |
| 6 | | | | | | 6 |
| 5 | | | | | | 5 |
| 4 | | | | | | 4 |
| 3 | | | | | | 3 |
| 2 | | | | | | 2 |
| 1 | | | | | | 1 |
| 0 | | | | | | 0 |

| Level | 1st | 2nd | 3rd | 4th | 5th |
|-------|-----|-----|-----|-----|-----|
| 16 | | | | | |
| 15 | | | | | |
| 14 | | | | | |
| 13 | | | | | |
| 12 | | | | | |
| 11 | | | | | |
| 10 | | | | | |
| 9 | | | | | |
| 8 | | | | | |
| 7 | | | | | |
| 6 | | | | | |
| 5 | | | | | |
| 4 | | | | | |
| 3 | | | | | |
| 2 | | | | | |
| 1 | | | | | |
| 0 | | | | | |

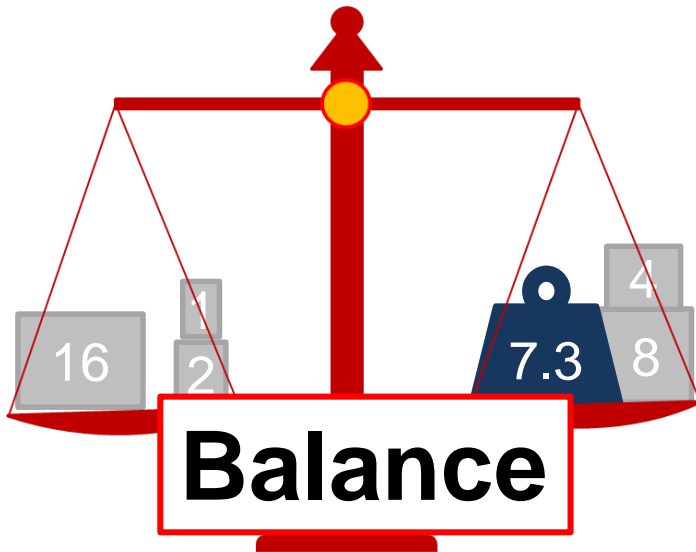
Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input: 7.3 [V]
- Binary weight :

$$7.3 \Rightarrow 00111 \Rightarrow 7$$

$$16 - 8 - 4 + 2 + 1 + 0.5 - 0.5 = 7$$



| Step | 1st | 2nd | 3rd | 4th | 5th | output |
|-------------|-----|-----|-----|-----|-----|--------|
| Weight p(k) | 16 | 8 | 4 | 2 | 1 | |
| 31 | | | | | | 31 |
| 30 | | | | | | 30 |
| 29 | | | | | | 29 |
| 28 | | | | | | 28 |
| 27 | | | | | | 27 |
| 26 | | | | | | 26 |
| 25 | | | | | | 25 |
| 24 | | | | | | 24 |
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| 15 | | | | | | 15 |
| 14 | | | | | | 14 |
| 13 | | | | | | 13 |
| 12 | | | | | | 12 |
| 11 | | | | | | 11 |
| 10 | | | | | | 10 |
| 9 | | | | | | 9 |
| 8 | | | | | | 8 |
| 7 | | | | | | 7 |
| 6 | | | | | | 6 |
| 5 | | | | | | 5 |
| 4 | | | | | | 4 |
| 3 | 0 | 0 | 1 | 1 | 1 | 3 |
| 2 | 0 | 0 | 1 | 1 | 1 | 2 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | | | | | | 0 |

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SAR ADC Redundancy Design

Redundancy

→ Surplus, Extra



Using time redundancy

- Extra comparison steps
- Change reference to Non-binary voltages



Enable digital error correction!

| Step | 1st | 2nd | 3rd | 4th | 5th | 6th | output |
|---------------|-----|-----|----------|-----|-----|-----|--------|
| Weight $p(k)$ | 16 | 10 | 6 | 3 | 2 | 1 | |
| 31 | | | ↓ | | | | 31 |
| 30 | | | | | | | 30 |
| 29 | | | | | | | 29 |
| 28 | | | | | | | 28 |
| 27 | | | | | | | 27 |
| 26 | | | ▲ $q(2)$ | | | | 26 |
| 25 | | | ↓ | | | | 25 |
| 24 | | | | | | | 24 |
| 23 | | | | | | | 23 |
| 22 | | | | | | | 22 |
| 21 | | | | | | | 21 |
| 20 | | | | | | | 20 |
| 19 | | | ▲ $q(3)$ | | | | 19 |
| 18 | | | ↓ | | | | 18 |
| 17 | | | | | | | 17 |
| 16 | | | | | | | 16 |
| 15 | | | | | | | 15 |
| 14 | | | | | | | 14 |
| 13 | | | | | | | 13 |
| 12 | | | | | | | 12 |
| 11 | | | | | | | 11 |
| 10 | | | | | | | 10 |
| 9 | | | | | | | 9 |
| 8 | | | | | | | 8 |
| 7 | | | | | | | 7 |
| 6 | | | | | | | 6 |
| 5 | | | | | | | 5 |
| 4 | | | | | | | 4 |
| 3 | | | | | | | 3 |
| 2 | | | | | | | 2 |
| 1 | | | | | | | 1 |
| 0 | | | | | | | 0 |

Level

$q(k)$: k -th step correctable difference

Redundancy Design Operation(No Error)

4bit-5step SAR ADC

- Analog input: 6.3
- Redundant weight :
16, 10, 6, 3, 2, 1

Correctable expression

$$6.3 \Rightarrow 010001 \Rightarrow 6$$

$$16 - 10 + 6 - 3 - 2 - 1 + 0.5 - 0.5 = 6$$

| Step | 1st | 2nd | 3rd | 4th | 5th | 6th | output |
|---------------|-----|-----|-----|-----|-----|-----|--------|
| Weight $w(k)$ | 16 | 10 | 6 | 3 | 2 | 1 | |
| 31 | | | | | | | 31 |
| 30 | | | | | | | 30 |
| 29 | 0 | 1 | 0 | 0 | 0 | 1 | 29 |
| 28 | | | | | | | 28 |
| 27 | | | | | | | 27 |
| 26 | | | | | | | 26 |
| 25 | | | | | | | 25 |
| 24 | | | | | | | 24 |
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| 22 | | | | | | | 22 |
| 21 | | | | | | | 21 |
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| 19 | | | | | | | 19 |
| 18 | | | | | | | 18 |
| 17 | | | | | | | 17 |
| 16 | | | | | | | 16 |
| 15 | | | | | | | 15 |
| 14 | | | | | | | 14 |
| 13 | | | | | | | 13 |
| 12 | | | | | | | 12 |
| 11 | | | | | | | 11 |
| 10 | | | | | | | 10 |
| 9 | | | | | | | 9 |
| 8 | | | | | | | 8 |
| 7 | | | | | | | 7 |
| 6 | | | | | | | 6 |
| 5 | | | | | | | 5 |
| 4 | | | | | | | 4 |
| 3 | | | | | | | 3 |
| 2 | | | | | | | 2 |
| 1 | | | | | | | 1 |
| 0 | | | | | | | 0 |

Level

Redundancy Design Operation(One Error)

4bit-5step SAR ADC

- Analog input: 6.3
- Redundant weight :
16, 10, 6, 3, 2, 1

Correctable expression

$6.3 \Rightarrow 010001 \Rightarrow 6$



Another expression

$6.3 \Rightarrow 001111 \Rightarrow 6$

$16 - 10 - 6 + 3 + 2 + 1 + 0.5 - 0.5 = 6$

Error correction

➔ High-Reliability

| Step | 1st | 2nd | 3rd | 4th | 5th | 6th | output |
|-------------|-----|-----|-----|-----|-----|-----|--------|
| Weight p(k) | 16 | 10 | 6 | 3 | 2 | 1 | |
| 31 | | | | | | | 31 |
| 30 | | | | | | | 30 |
| 29 | 0 | 1 | 0 | 0 | 0 | 1 | 29 |
| 28 | | | | | | | 28 |
| 27 | | | | | | | 27 |
| 26 | | | | | | | 26 |
| 25 | | | | | | | 25 |
| 24 | | | | | | | 24 |
| 23 | | | | | | | 23 |
| 22 | | | | | | | 22 |
| 21 | | | | | | | 21 |
| 20 | | | | | | | 20 |
| 19 | | | | | | | 19 |
| 18 | | | | | | | 18 |
| 17 | | | | | | | 17 |
| 16 | | | | | | | 16 |
| 15 | | | | | | | 15 |
| 14 | | | | | | | 14 |
| 13 | | | | | | | 13 |
| 12 | | | | | | | 12 |
| 11 | | | | | | | 11 |
| 10 | | | | | | | 10 |
| 9 | | | | | | | 9 |
| 8 | | | | | | | 8 |
| 7 | | | | | | | 7 |
| 6 | | | | | | | 6 |
| 5 | | | | | | | 5 |
| 4 | | | | | | | 4 |
| 3 | | | | | | | 3 |
| 2 | | | | | | | 2 |
| 1 | | | | | | | 1 |
| 0 | | | | | | | 0 |
| | 0 | 0 | 1 | 1 | 1 | 1 | |

Misjudgment

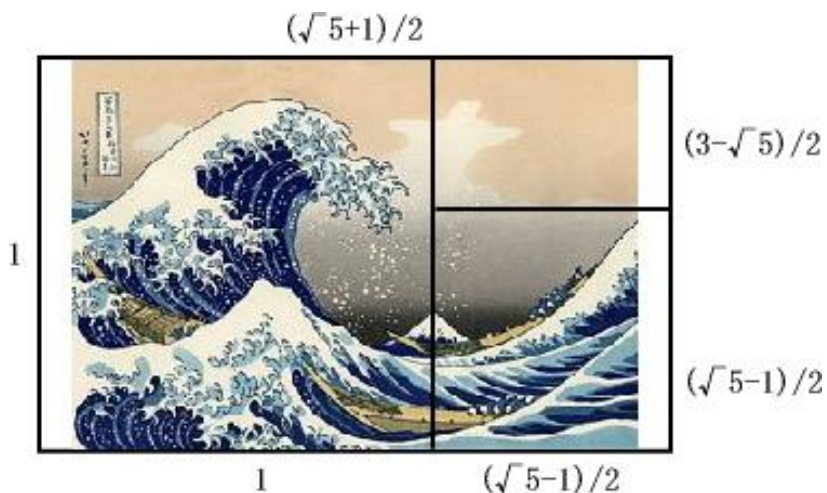
0 0 1 1 1 1

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Golden Ratio

- Ratio satisfying $a:b = b:(a + b)$
- $\phi = \frac{b}{a} = \frac{1+\sqrt{5}}{2} = 1.618033988749895 \dots$
- The most beautiful ratio



Fibonacci Sequence

Definition ($n=0,1,2,3\dots$)

$$F_0 = 0$$

$$F_1 = 1$$

$$F_{n+2} = F_n + F_{n+1}$$



Fibonacci number

0, 1, 1, **2**, 3, 5, **8**, 13, 21, 34, **55** ...

+ ↗
+ ↗
+ ↗

Property

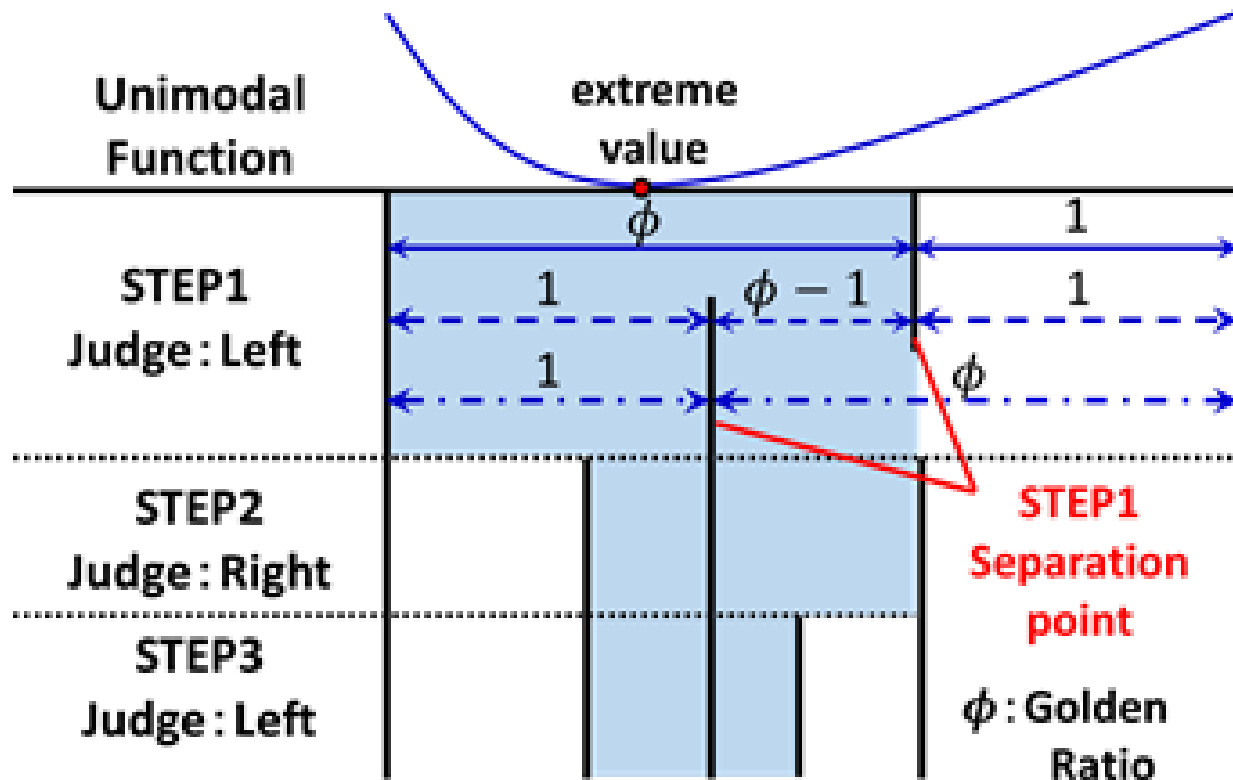
The closest terms ratio converges to **“Golden Ratio”** !

$$\lim_{n \rightarrow \infty} \frac{F_n}{F_{n-1}} = 1.6180339887 \dots = \phi$$

Golden Section Search

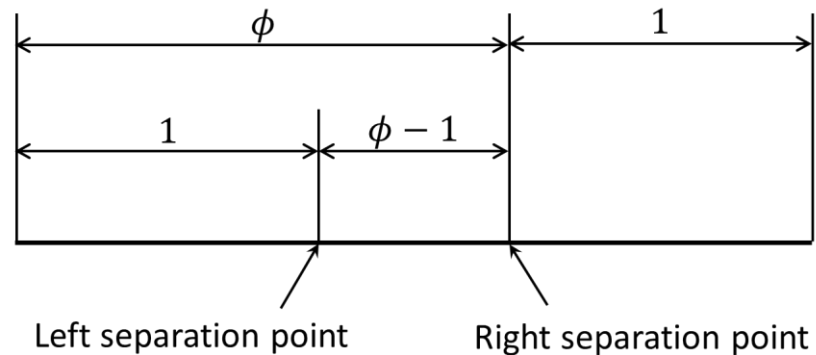
Finding of effectively extreme value of unimodal function

Division ratio = Golden ratio



Fibonacci Search

Golden Section Search (ϕ :Golden ratio)



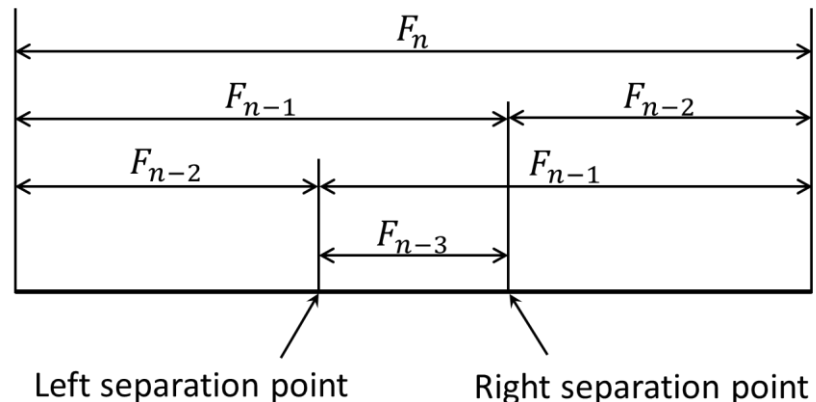
ADC treats only integers



Difficult to realize

Performing golden division with only integers

Fibonacci search (F_x :Fibonacci number)



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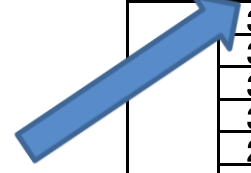
Fibonacci Sequence Weighted SAR ADC

Fibonacci sequence SAR ADC

Weight is Fibonacci sequence

| Step | 1st | 2nd | 3rd | 4th | 5th | 6th | 7th |
|---------------|-----|-----|-----|-----|-----|-----|-----|
| Weight $p(k)$ | 16 | 8 | 5 | 3 | 2 | 1 | 1 |
| 33 | | | | | | | |
| 32 | | | | | | | |
| 31 | | | | | | | |
| 30 | | | | | | | |
| 29 | | | | | | | |
| 28 | | | | | | | |
| 27 | | | | | | | |
| 26 | | | | | | | |
| 25 | | | | | | | |
| 24 | | | | | | | |
| 23 | | | | | | | |
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| 21 | | | | | | | |
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| 19 | | | | | | | |
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| 17 | | | | | | | |
| 16 | | | | | | | |
| 15 | | | | | | | |
| 14 | | | | | | | |
| 13 | | | | | | | |
| 12 | | | | | | | |
| 11 | | | | | | | |
| 10 | | | | | | | |
| 9 | | | | | | | |
| 8 | | | | | | | |
| 7 | | | | | | | |
| 6 | | | | | | | |
| 5 | | | | | | | |
| 4 | | | | | | | |
| 3 | | | | | | | |
| 2 | | | | | | | |
| 1 | | | | | | | |
| 0 | | | | | | | |
| -1 | | | | | | | |
| -2 | | | | | | | |

Level



$q(1)$

$q(2)$

$q(3)$

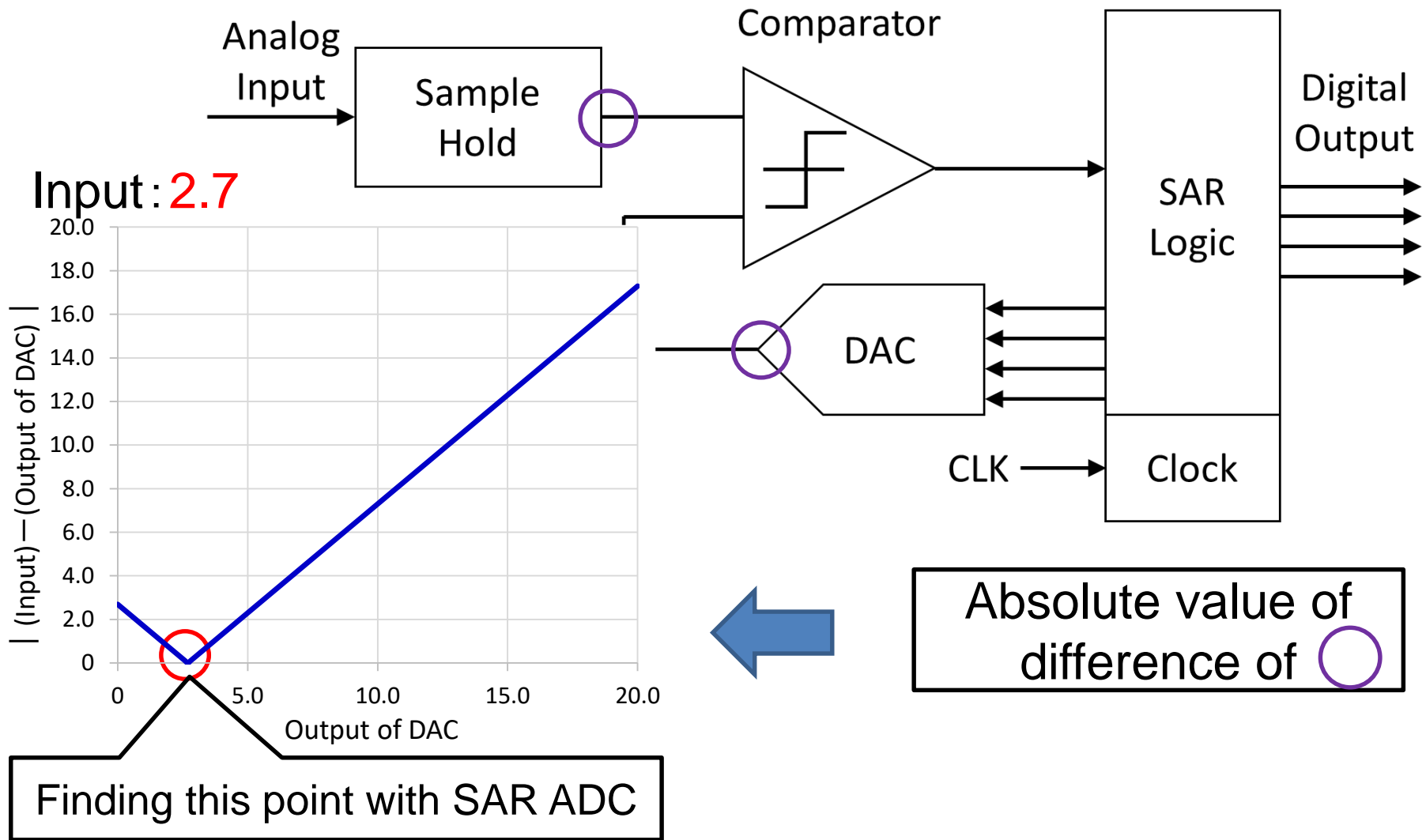
$q(4)$

$q(5)$

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SAR ADC Based on Fibonacci Search

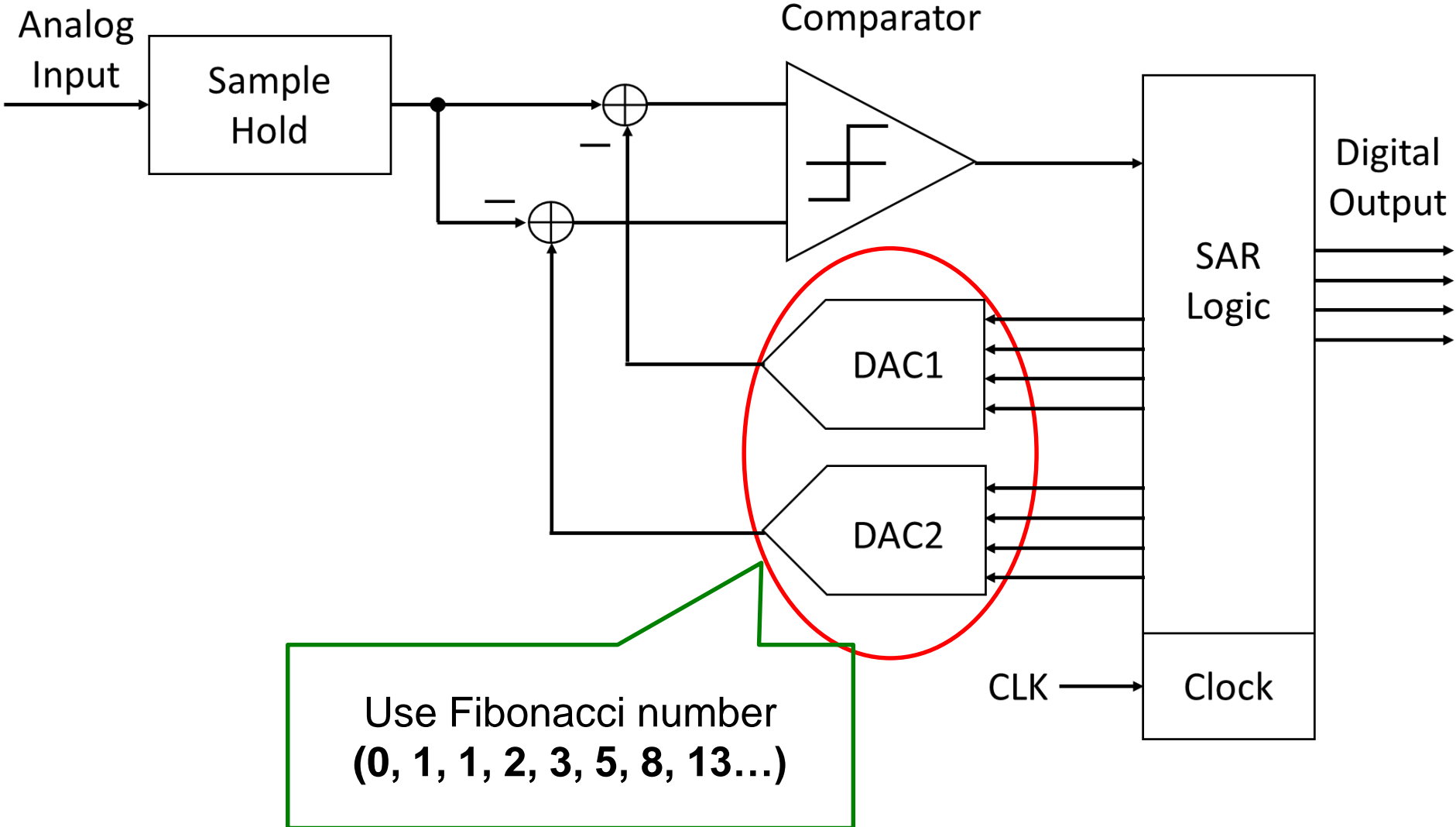


Absolute value of difference of 

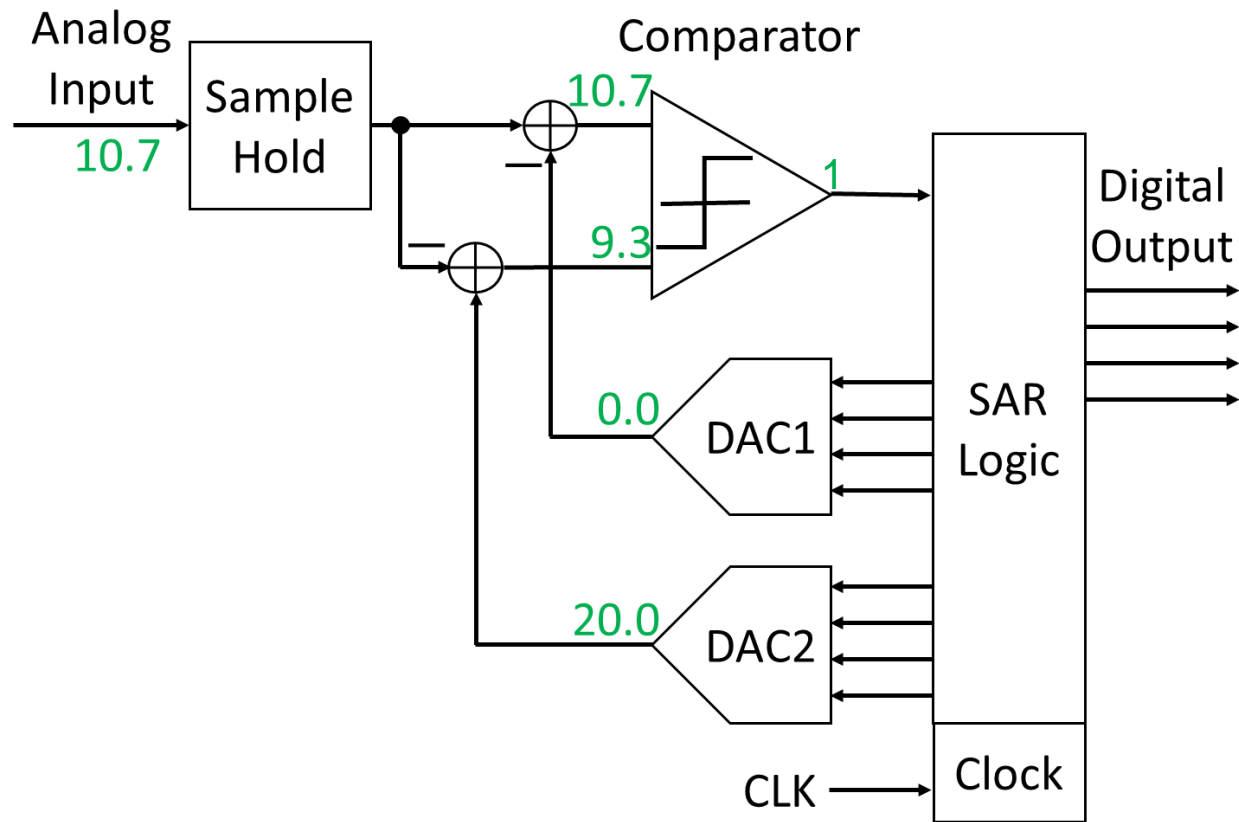
Unimodal function with local minimum 

Use **Fibonacci search**

Block Diagram of SAR ADC Based on Fibonacci Search



Operation of SAR ADC Based on Fibonacci Search



| step | 1st | 2nd | 3rd | 4th | 5th | output |
|------|------|-----|-----|-----|-----|--------|
| 20 | | | | | | 20 |
| 19 | | | | | | 19 |
| 18 | | | | | | 18 |
| 17 | | | | | | 17 |
| 16 | 9.3 | | | | | 16 |
| 15 | | | | | | 15 |
| 14 | | | | | | 14 |
| 13 | | | | | | 13 |
| 12 | | | | | | 12 |
| 11 | | | | | | 11 |
| 10 | | | | | | 10 |
| 9 | | | | | | 9 |
| 8 | | | | | | 8 |
| 7 | | | | | | 7 |
| 6 | | | | | | 6 |
| 5 | | | | | | 5 |
| 4 | 10.7 | | | | | 4 |
| 3 | | | | | | 3 |
| 2 | | | | | | 2 |
| 1 | 1 | | | | | 1 |
| 0 | | | | | | 0 |
| -1 | | | | | | -1 |

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Revised SAR ADC Based on Fibonacci Search

Comparison method before change

$$V_{in} - DAC1 (\geq \text{ or } \leq) DAC2 - V_{in}$$



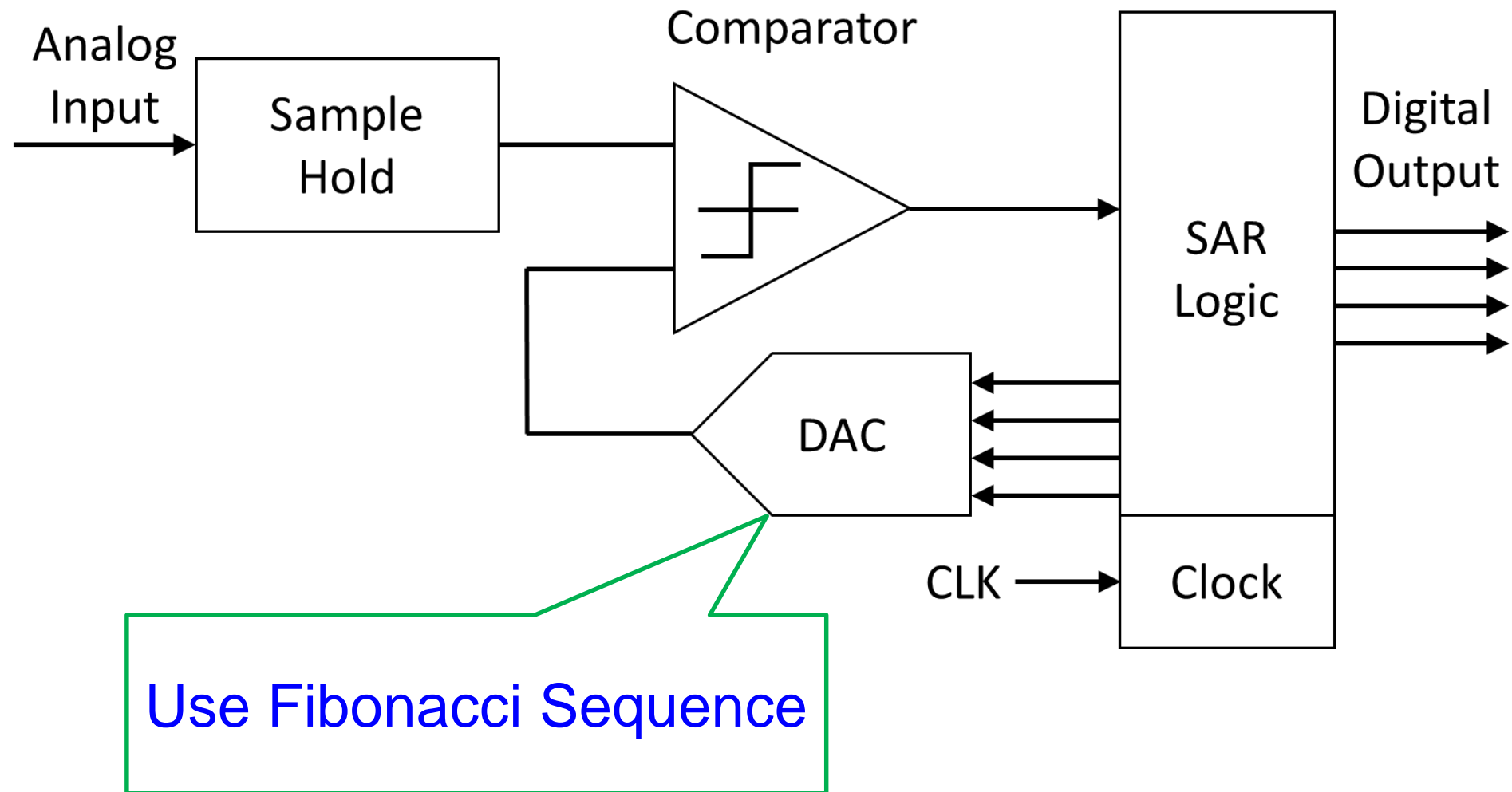
$$2V_{in} (\geq \text{ or } \leq) DAC1 + DAC2$$



$$V_{in} (\geq \text{ or } \leq) \frac{1}{2} (DAC1 + DAC2)$$

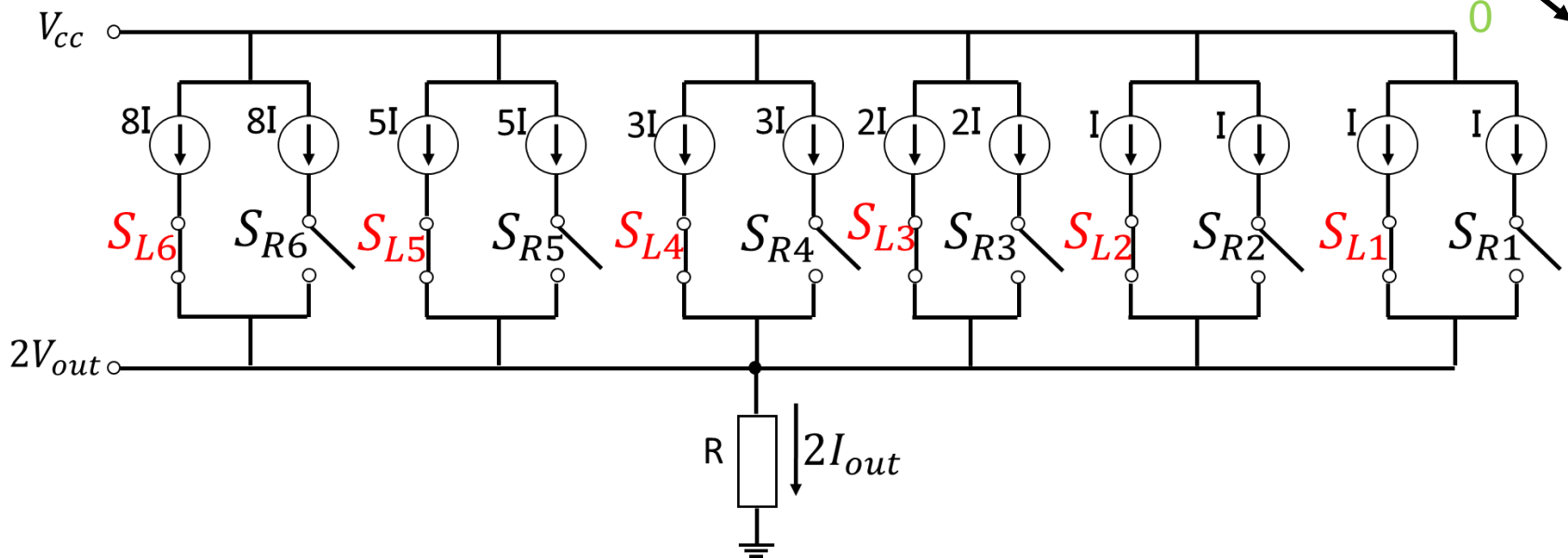
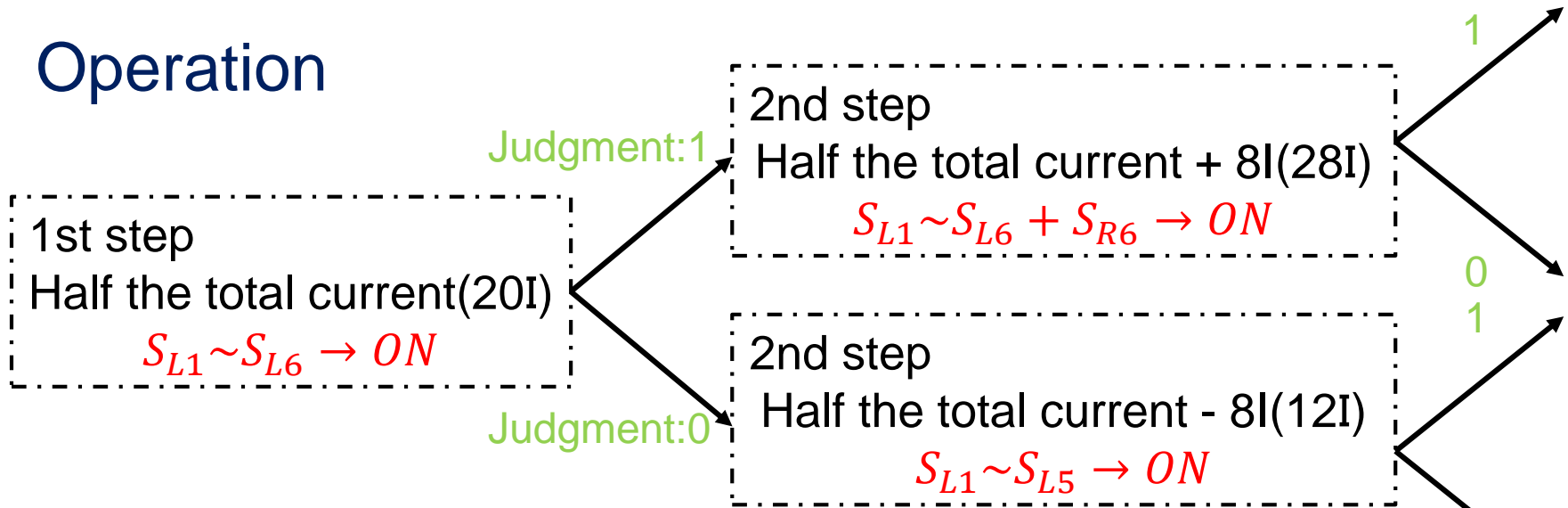
Equivalent comparison method

Block Diagram of Revised SAR ADC Based on Fibonacci Search



Operation & DAC Revised SAR ADC Based on Fibonacci Search

Operation



Revised SAR ADC Based on Fibonacci Search

Revised SAR ADC Based on Golden Section Search

Input 10.7

Output 10

| | step | 1st | 2nd | 3rd | 4th | 5th | output |
|--|------|-----|-----|-----|-----|-----|--------|
| | 20 | | | | | | 20 |
| | 19 | | | | | | 19 |
| | 18 | | | | | | 18 |
| | 17 | | | | | | 17 |
| | 16 | | | | | | 16 |
| | 15 | | | | | | 15 |
| | 14 | | | | | | 14 |
| | 13 | | | | | | 13 |
| | 12 | | | | | | 12 |
| | 11 | | | | | | 11 |
| | 10 | | | | | | 10 |
| | 9 | | | | | | 9 |
| | 8 | | | | | | 8 |
| | 7 | | | | | | 7 |
| | 6 | | | | | | 6 |
| | 5 | | | | | | 5 |
| | 4 | | | | | | 4 |
| | 3 | | | | | | 3 |
| | 2 | | | | | | 2 |
| | 1 | | | | | | 1 |
| | 0 | | | | | | 0 |
| | -1 | | | | | | -1 |

Level

---: Input

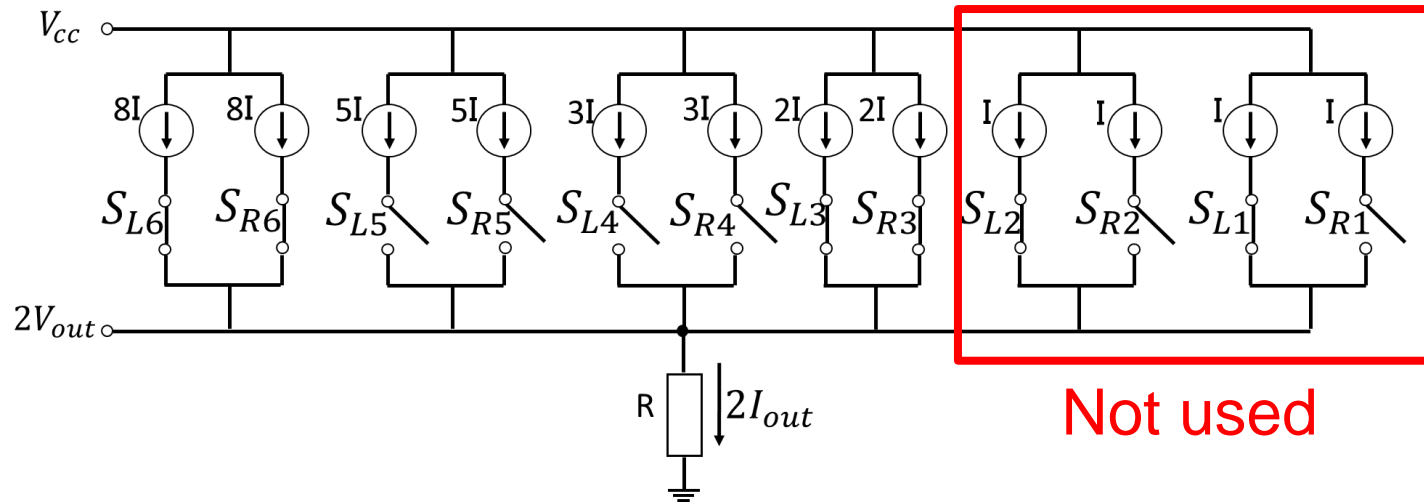
—: Comparison point

■: Solution existence range

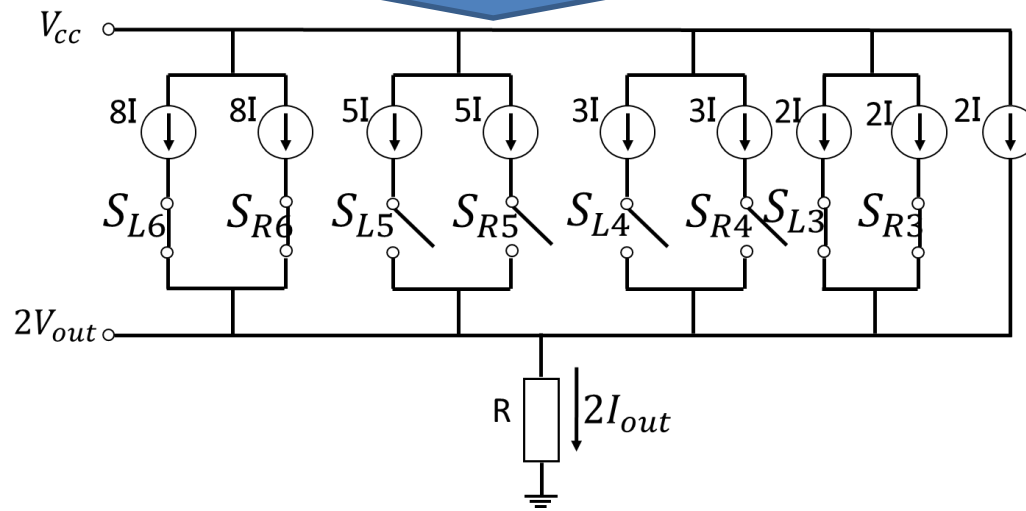
Figure of DAC
at this time

Final Step of Revised SAR ADC Based on Fibonacci Search

DAC of final step



Further revised



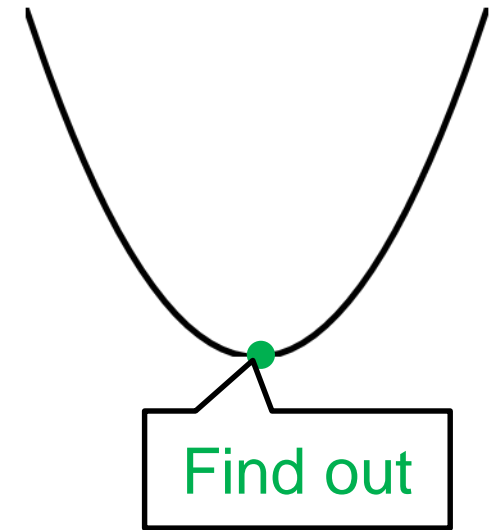
OUT LINE

- Introduction
- SAR ADC & Redundancy Design
- Golden Section Search & Fibonacci Search
- Fibonacci Sequence Weighted SAR ADC
- SAR ADC Based on Fibonacci Search
- **Proof & Simulation**
- Conclusion

Proof Contents

SAR ADC based on
golden section search
using unimodal function

 **equivalent**



Fibonacci sequence weighted SAR ADC

Prove above

Proof by Mathematical Expression

Fibonacci sequence

$$F_0 = 0$$

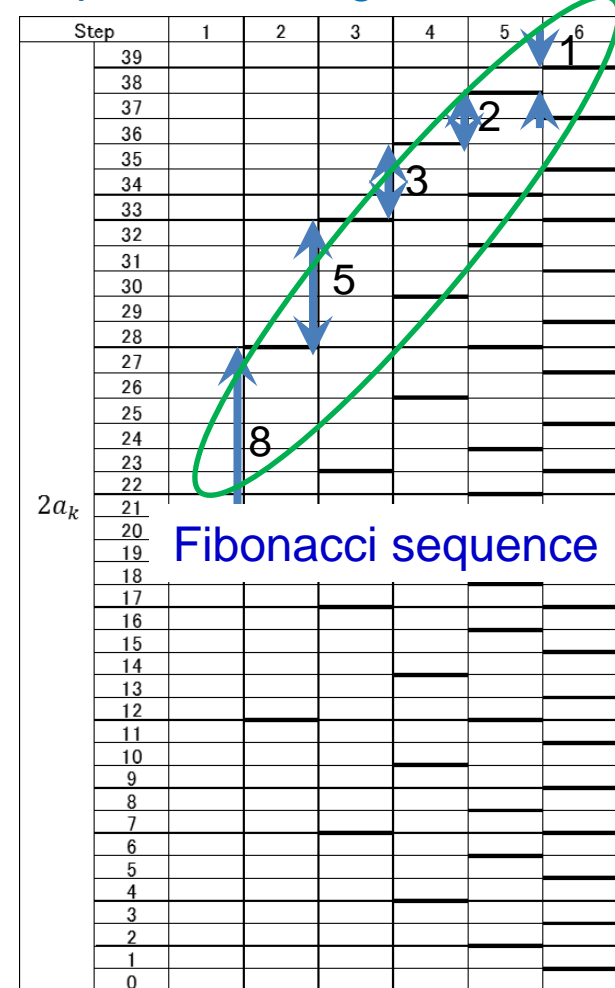
$$F_1 = 1$$

$$F_{n+2} = F_n + F_{n+1}$$

Comparison voltage

$$2a_k = (F_n + F_{n-1} + \dots + F_1) + (\pm F_n \pm F_{n-1} \pm \dots \pm F_1)$$

Comparison voltage when n=6



Difference of comparison voltages is
Fibonacci sequence



Matches **Fibonacci sequence**
weighted SAR ADC

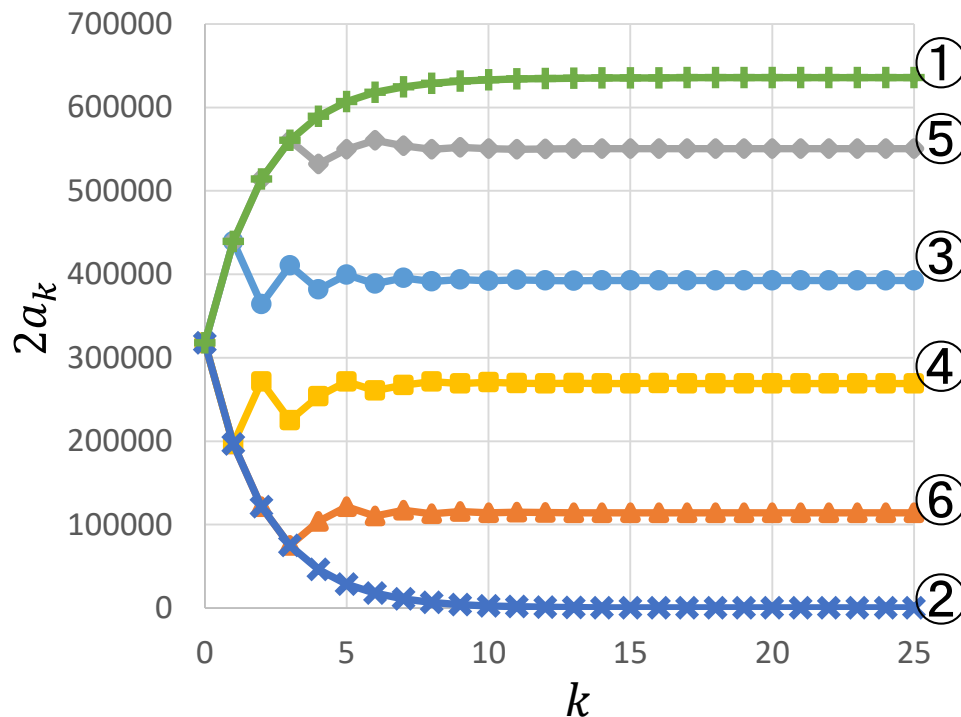
Simulation

Simulation condition

- ① $V_{in} = 0$, ② $V_{in} = 317810$, ③ $V_{in} = 196231.78$,
 ④ $V_{in} = 57096.156$, ⑤ $V_{in} = 275302.91$, ⑥ $V_{in} = 134576.64$

Convergence prediction

- ① 0, ② 635620, ③ 392462, ④ 114192, ⑤ 550604, ⑥ 269152



All converged to
intended value

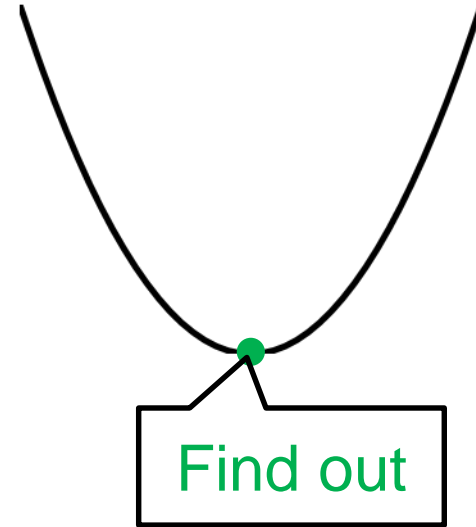
※ $n = 26$

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- Introduction
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Conclusion

New Theorem

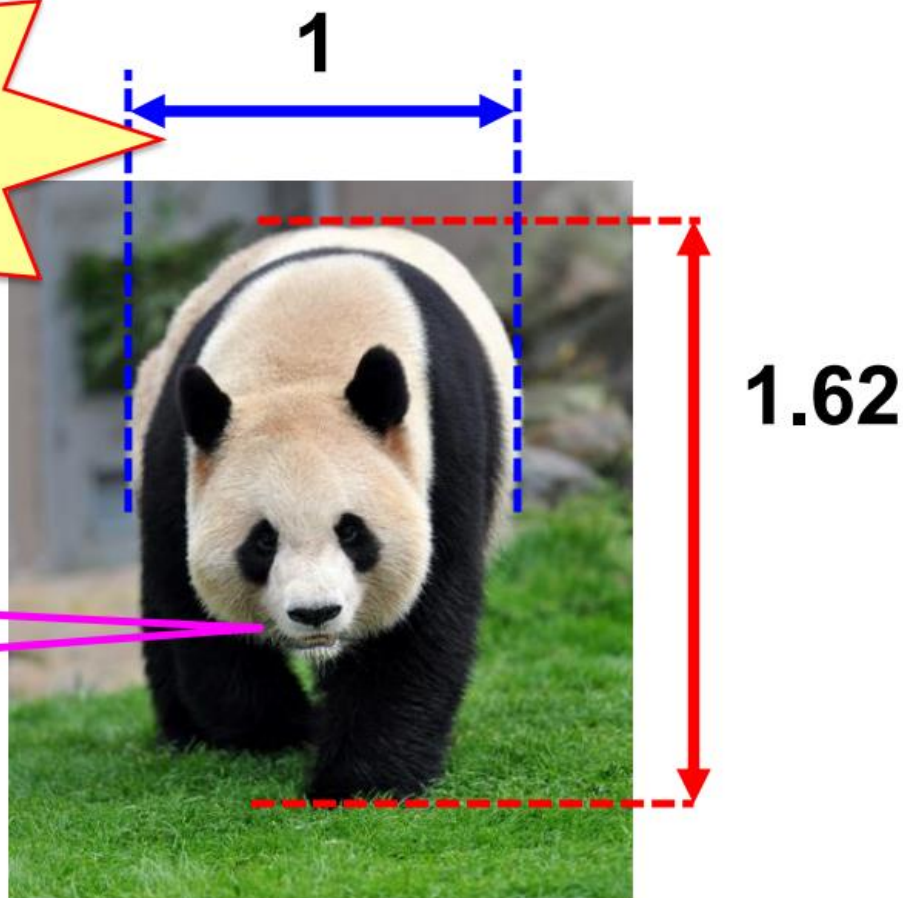


Equivalency

- SAR ADC using golden section search
- Fibonacci sequence weighted SAR ADC

Thank you for listening

Golden Ratio

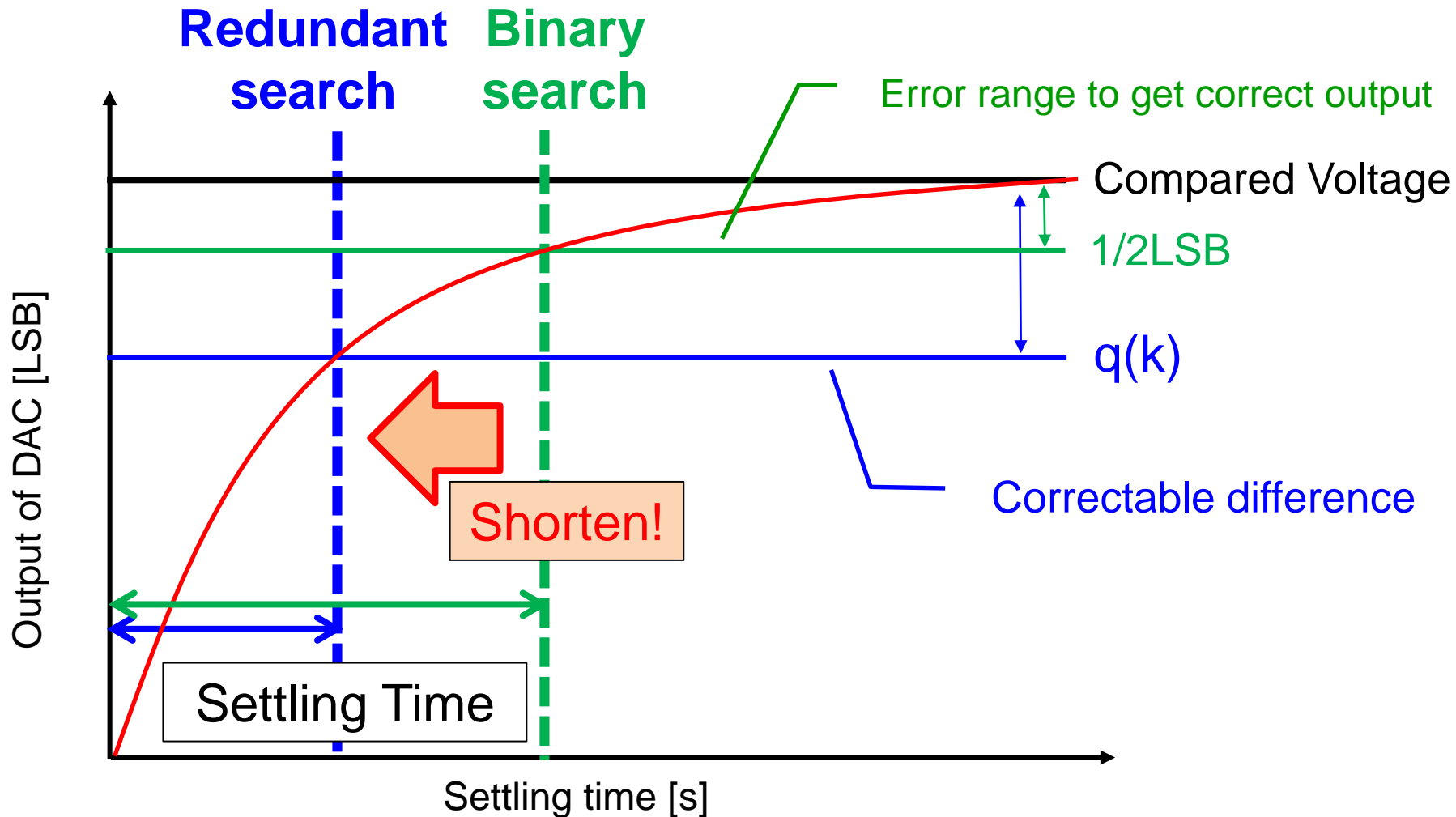


謝謝

appendix

DAC Settling Time at Every Step

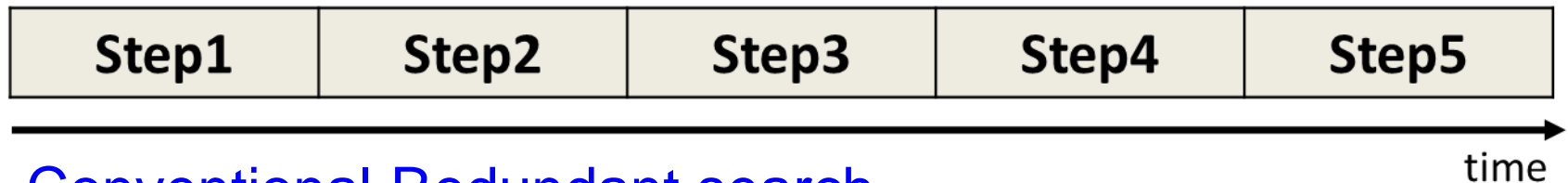
Shorten Conversion time



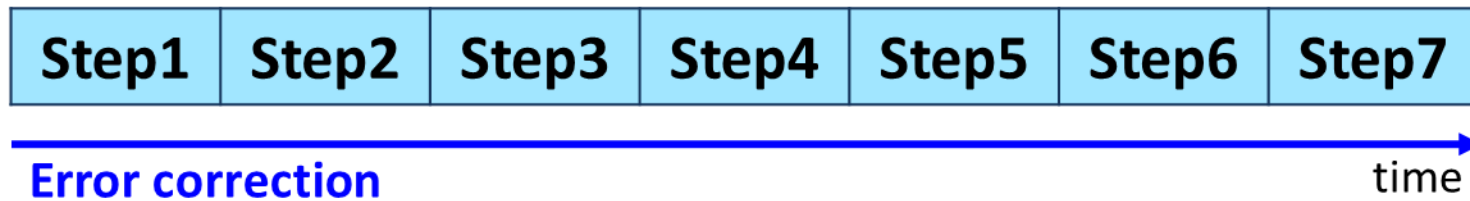
Reduction of Settling Time

5bit SAR ADC

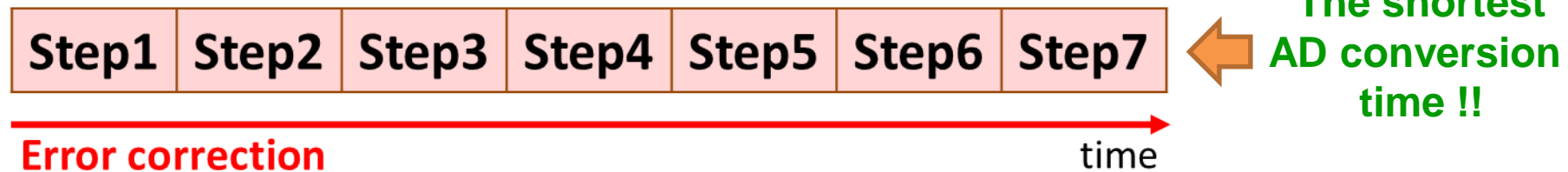
Binary search



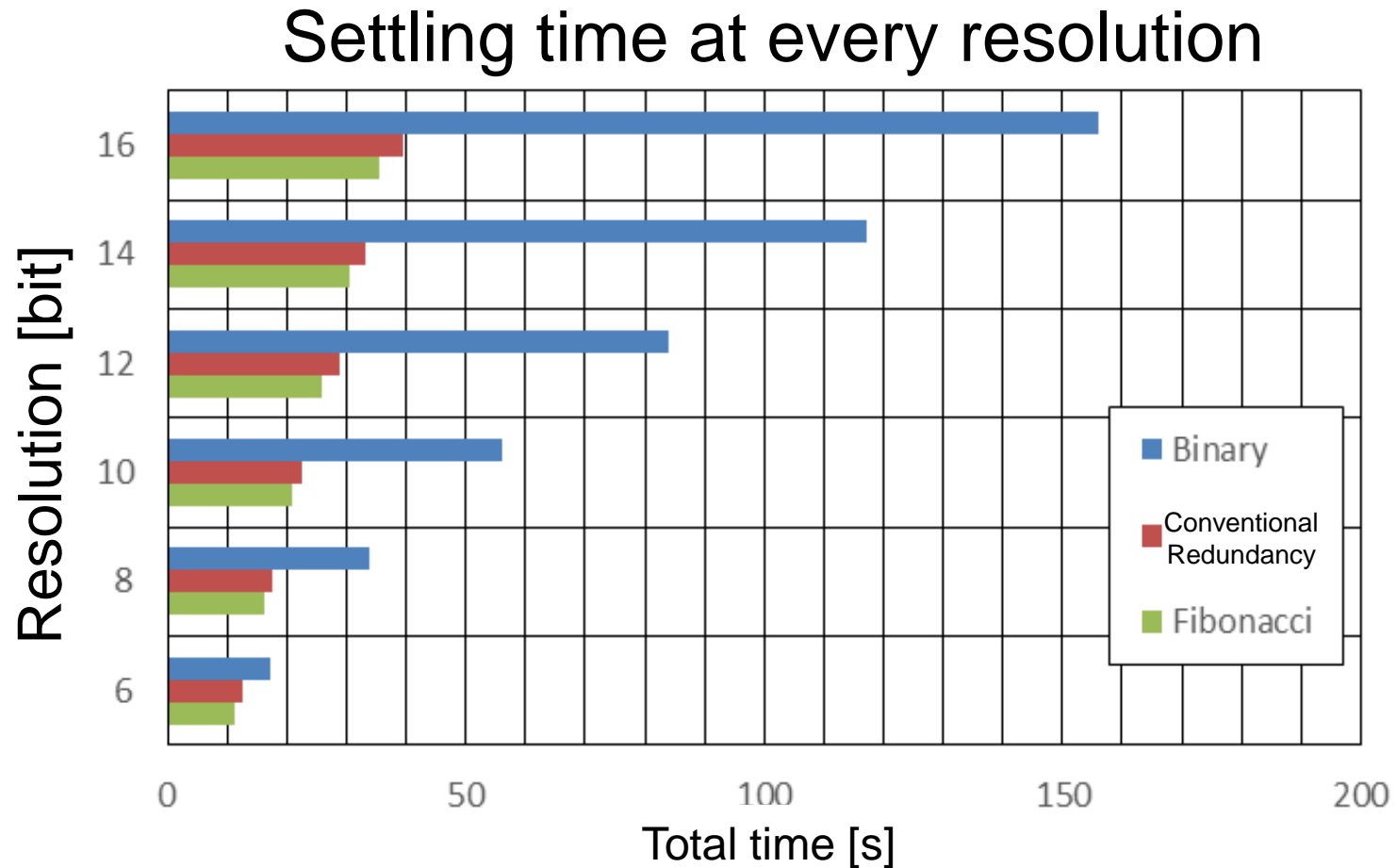
Conventional Redundant search



Fibonacci search



Comparison of Incomplete Settling Time



At fixed clock,

Fibonacci → the shortest AD conversion time !!

Conventional and Proposal DAC

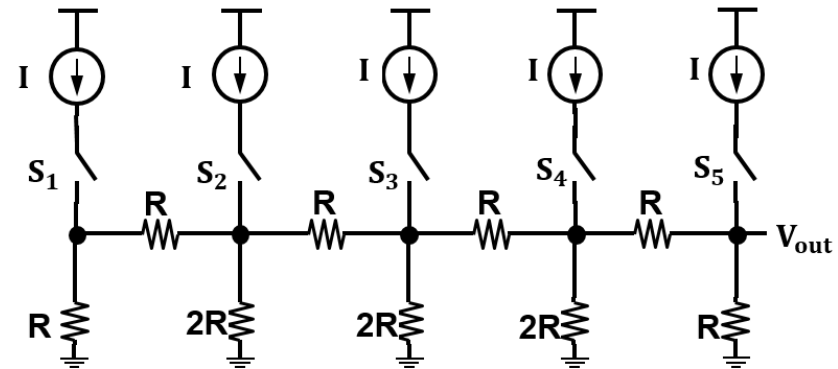
Conventional

R-2R resistor ladder

⇒ Generate binary voltage



Change all resistors to R



R-2R resistor ladder

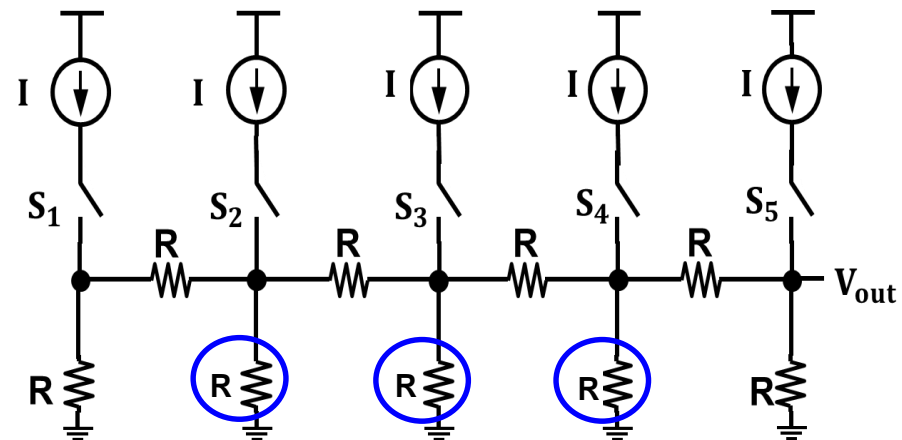


Proposal

R-R resistor ladder

⇒ Generate Fibonacci voltage

Realize Fibonacci DAC
by using simple circuit !

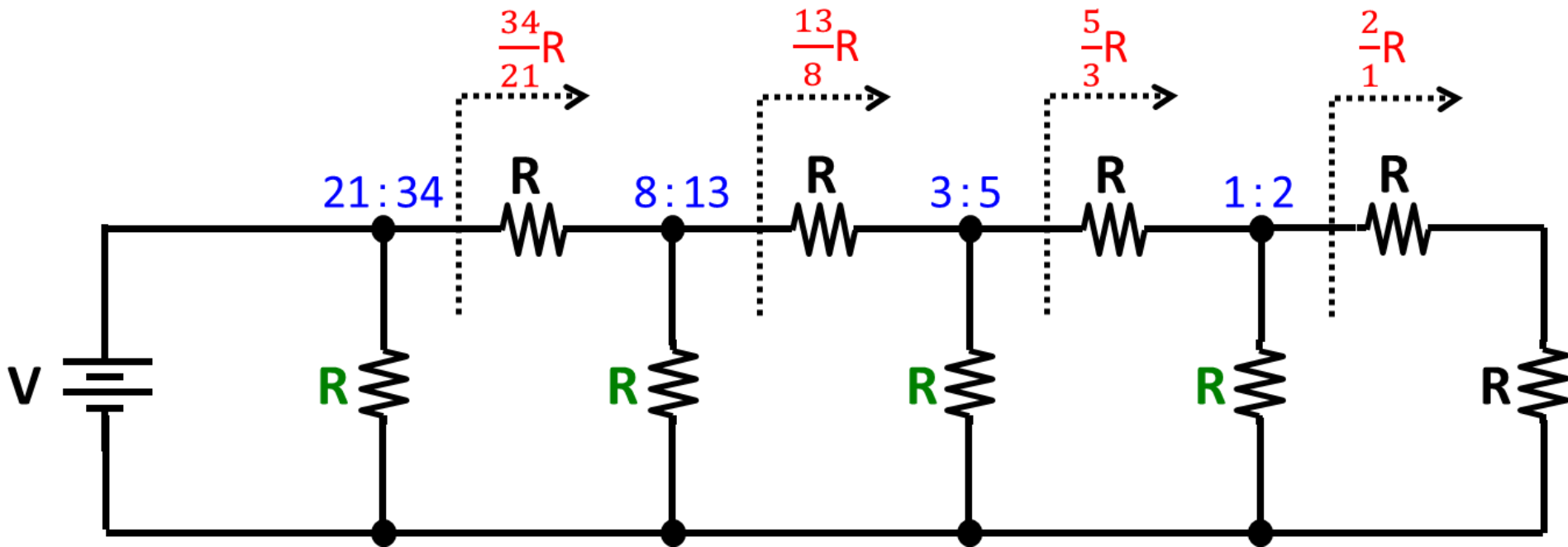


R-R resistor ladder

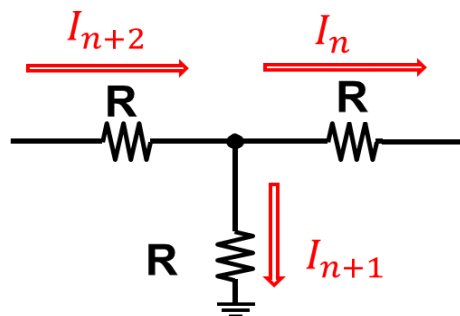
Principle of Fibonacci Voltage

New property

Divides current into **Fibonacci ratio** in each node



Principle



$$I_{n+2} = I_{n+1} + I_n$$

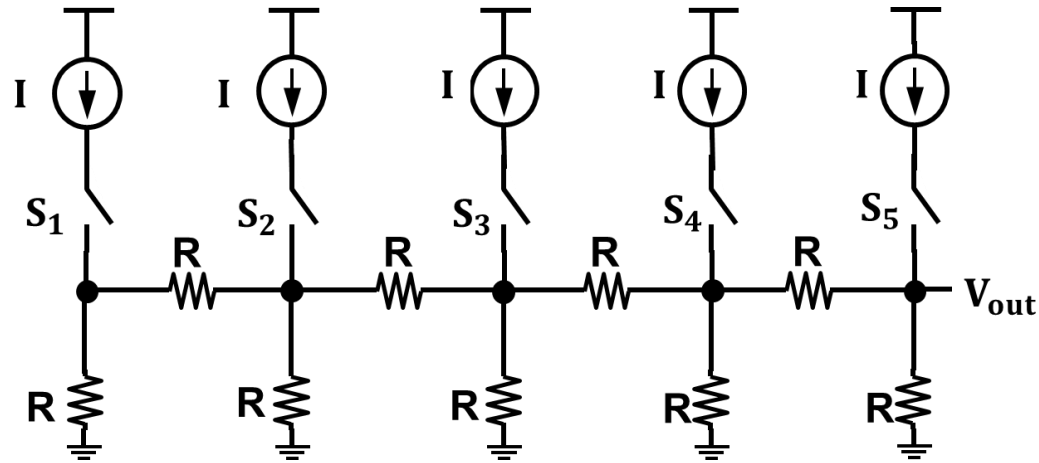


$$F_{n+2} = F_{n+1} + F_n$$

Proposal of R//R Fibonacci DAC

R-R resistor ladder

Generate
Fibonacci voltage
of **odd** term

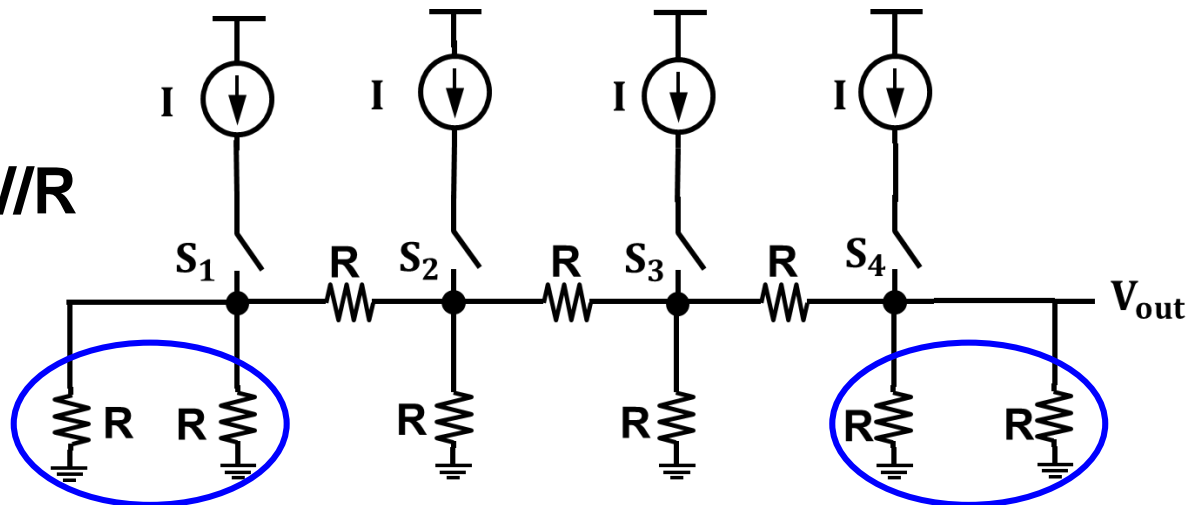


Change terminal resistors to
parallel resistors

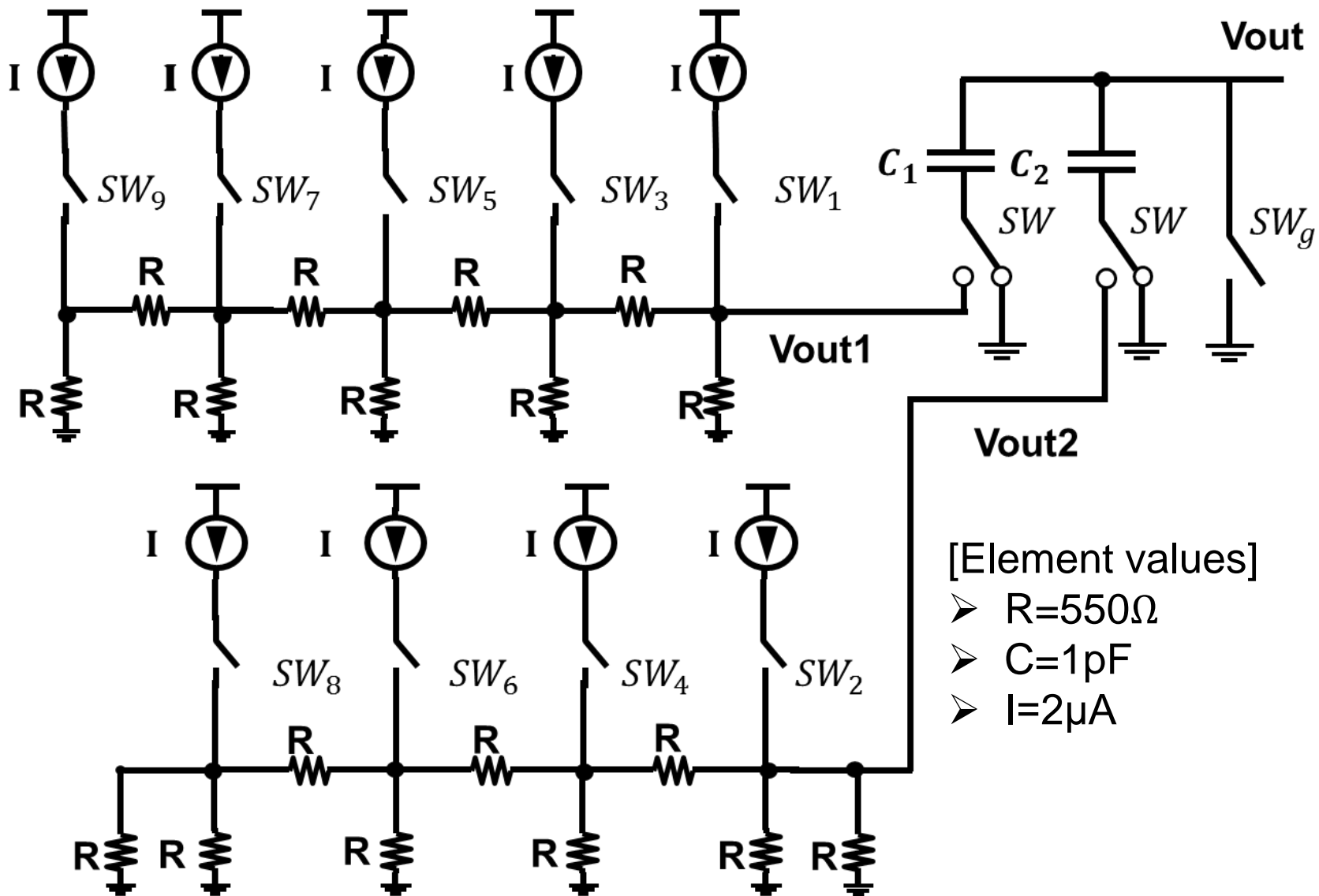
Proposal

R-R resistor ladder with terminations of R//R

Generate
Fibonacci voltage
of **even** term



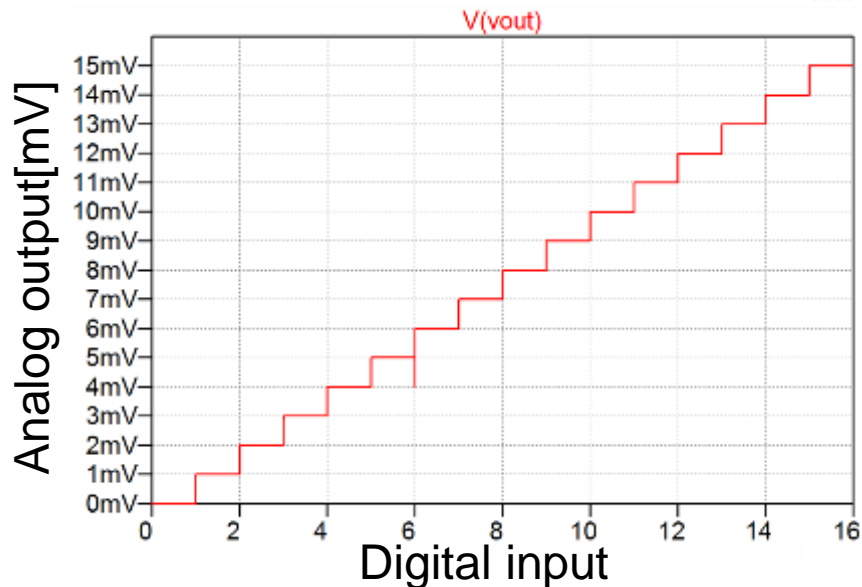
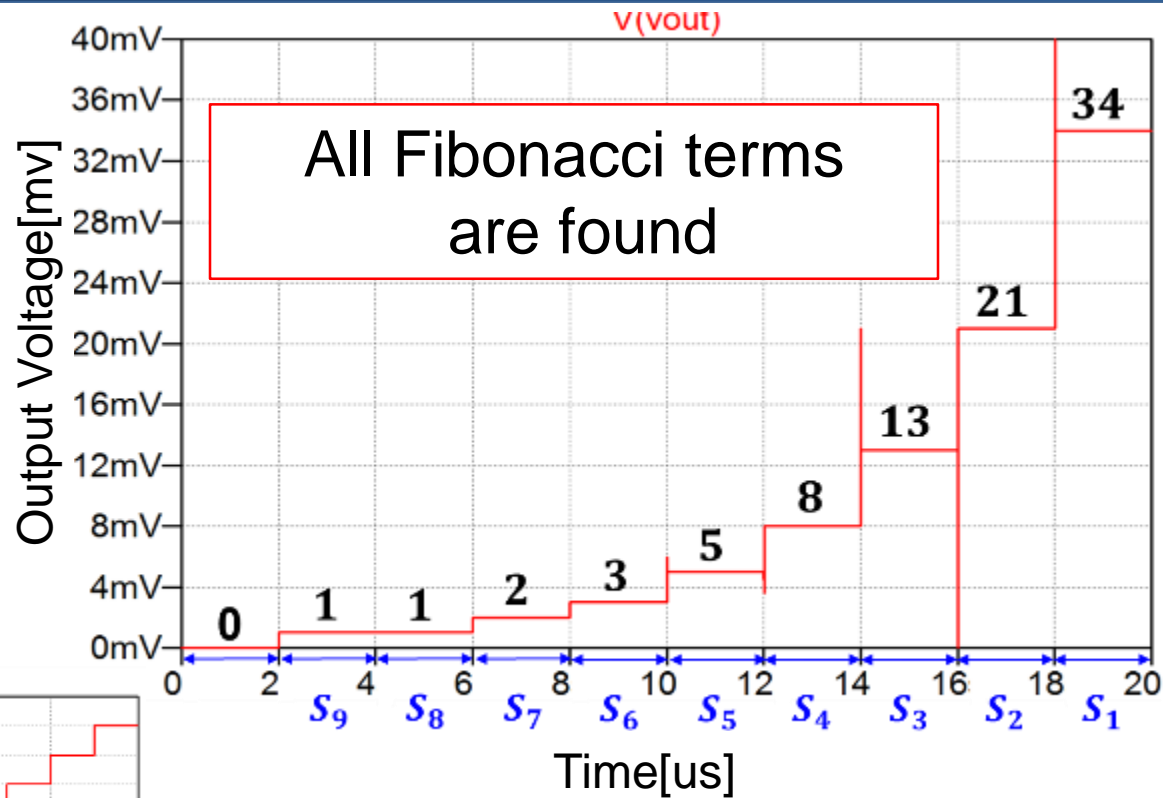
Fibonacci DAC simulation



Simulation Result

Operation simulation

Each switch corresponds to a Fibonacci term



A-D conversion simulation

Combination of current sources realizes DAC function

Fibonacci DAC is realized

