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Architecture of High Performance Successive Approximation Time Digitizer

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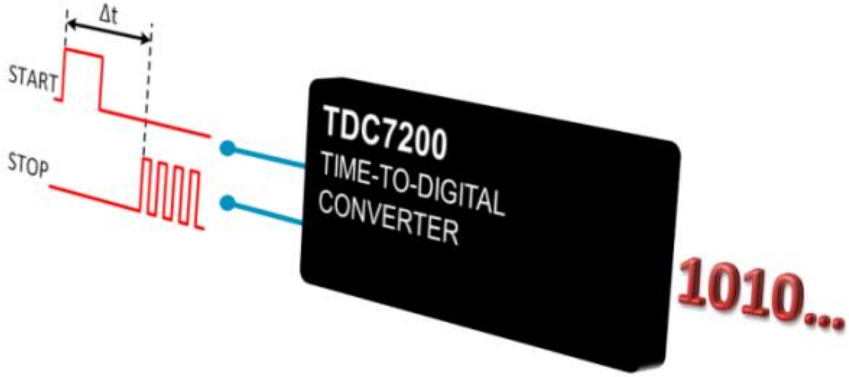
OUTLINE

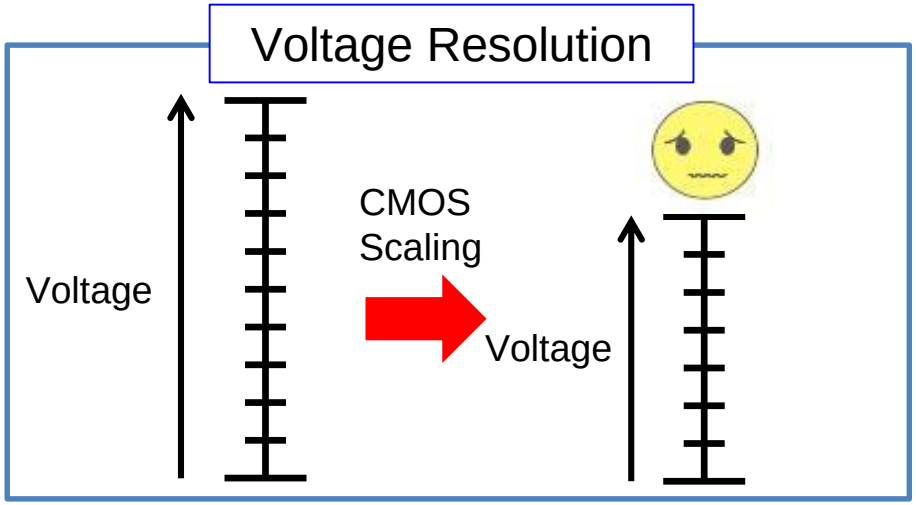
- Research background
- What is TDC ?
- Configuration of SAR TDC
- Fine Time Resolution with 2-step
- Self-calibration for absolute delay variation
- One-shot timing measurement using trigger circuit
- Conclusion

Research Objective

Development of
highly - linear, fine time-resolution TDC
for high-speed digital I/O interface timing measurement

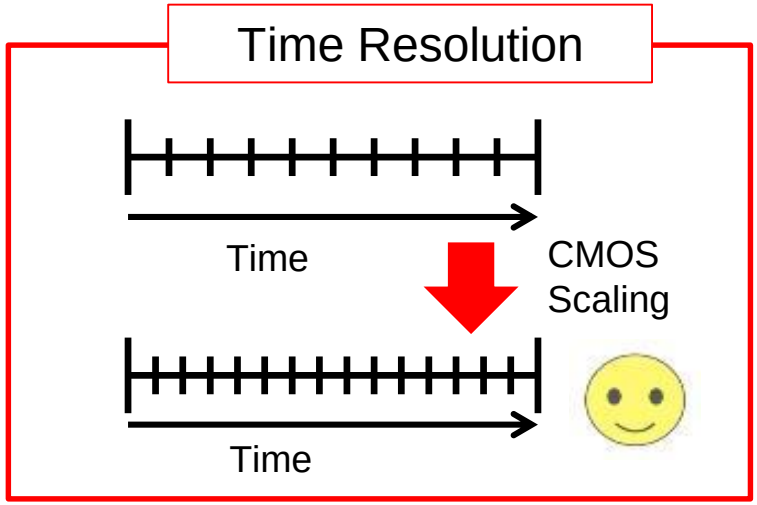


Background

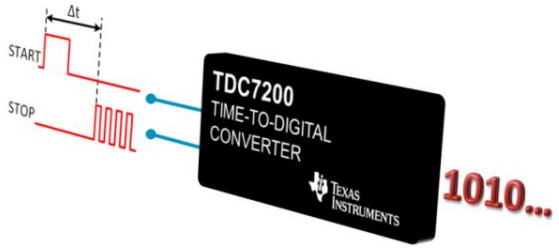


facing difficulties
due to reduced supply voltage

Analog circuit design difficultly

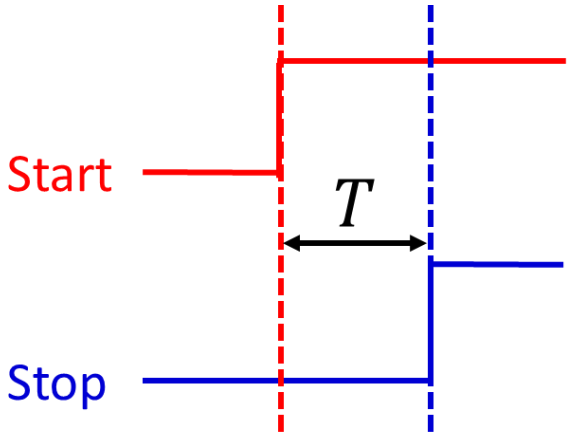


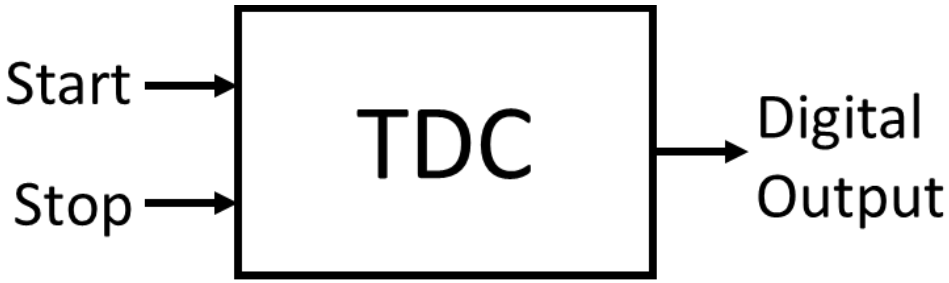
becoming superior



Role of Time-to-Digital Converter

Time difference → Measurement → Digital output





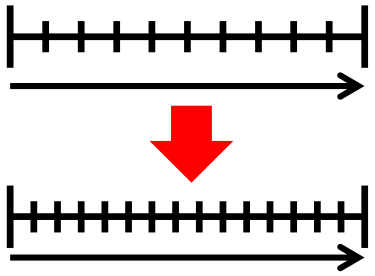
Time-to-Digital Converter : TDC

measure two time differences, outputs digitally

Innovation

[1] Two – Step SAR TDC

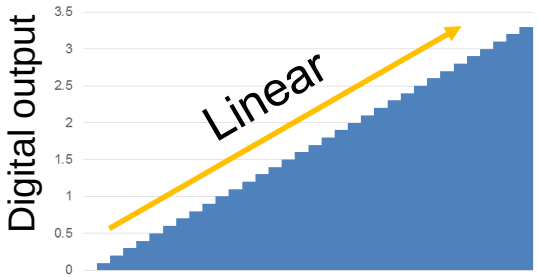
⇒ Fine time resolution



time resolution

[2] Self – Calibration

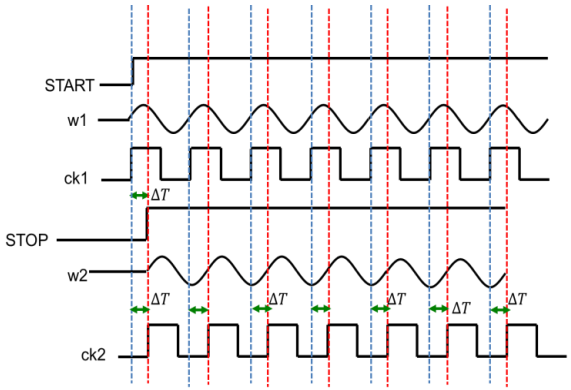
⇒ Linear TDC



time resolution

[3] Trigger Circuit

⇒ One – shot timing measurement

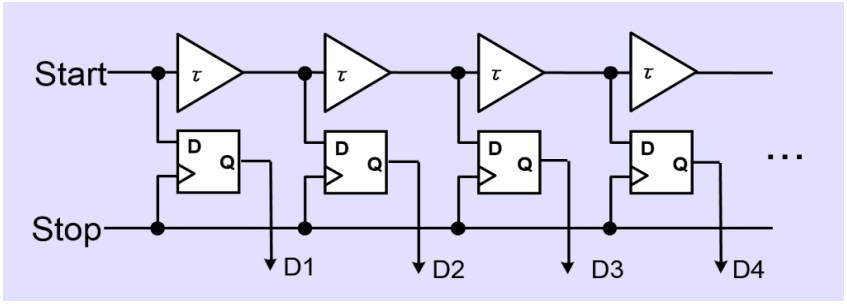


Holds the signal time difference once input

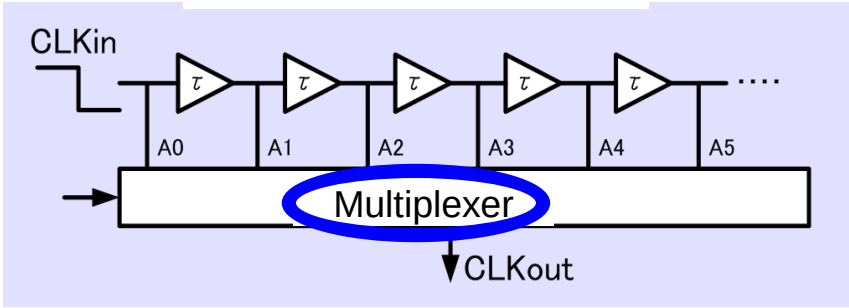
Configuration of SAR TDC

Use multiplexer

Dramatically reduced number of DFFs

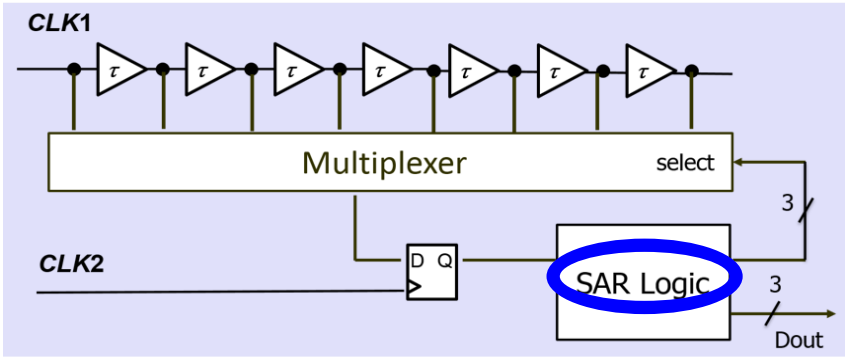


Flash type TDC



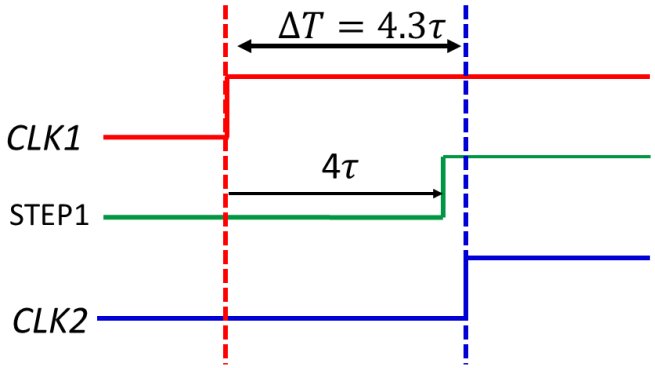
Use SAR Logic

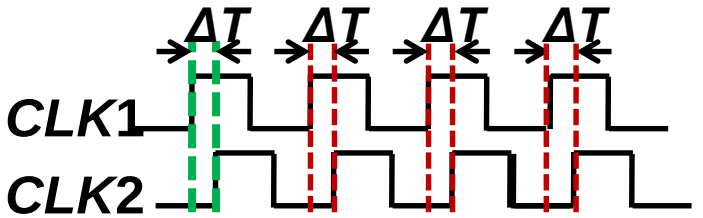
Operation loop of circuit



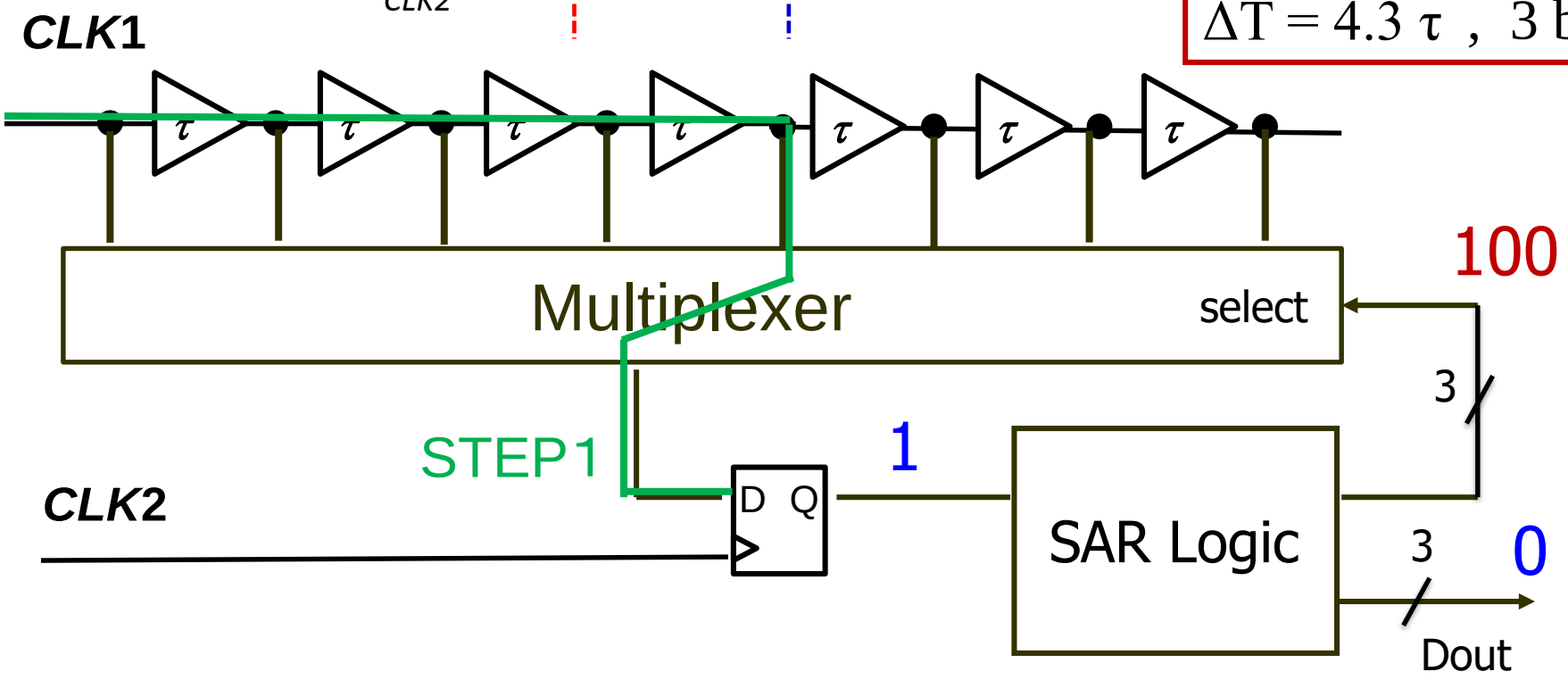
SAR TDC

Operation of SAR TDC (STEP 1)

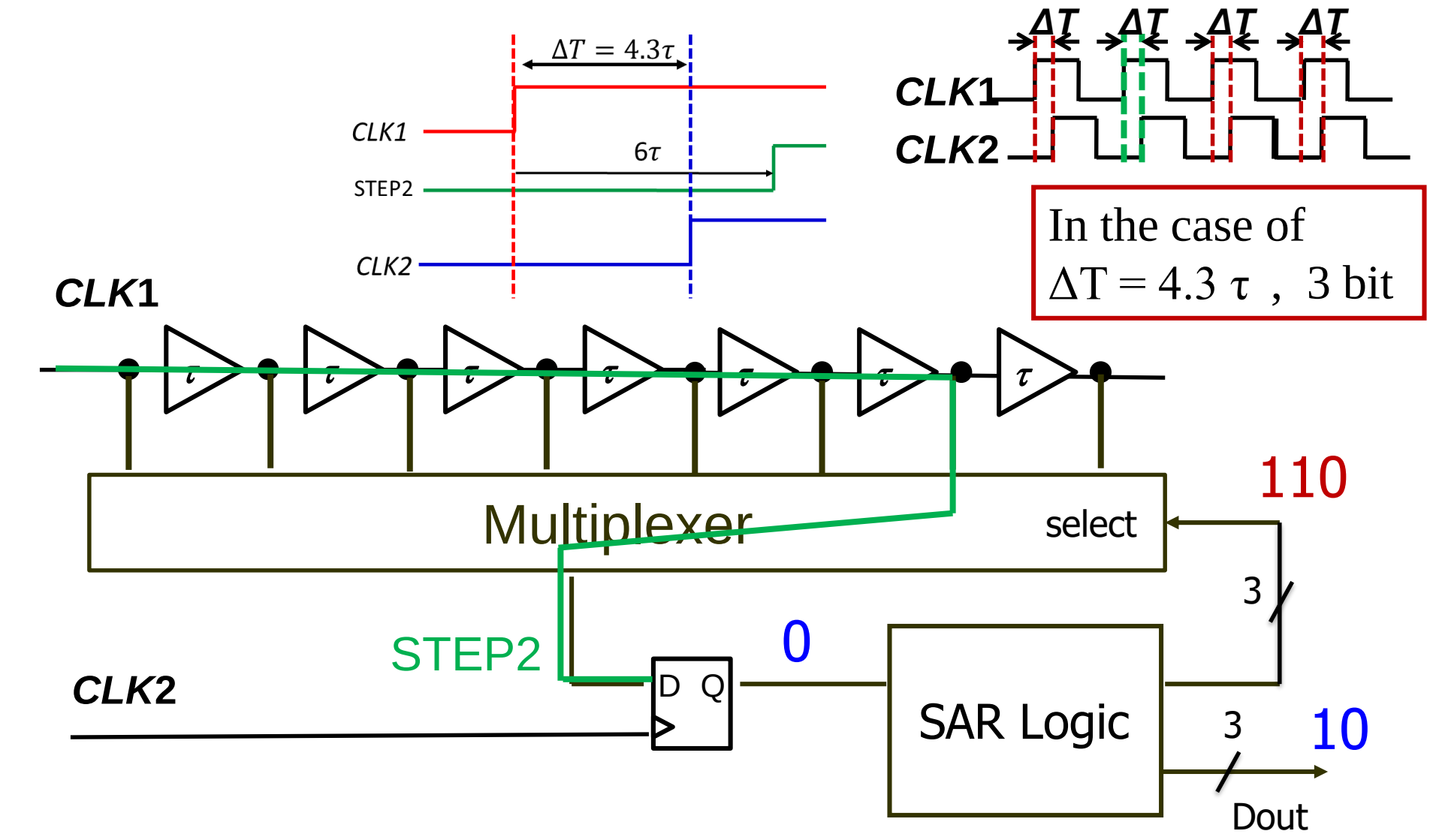




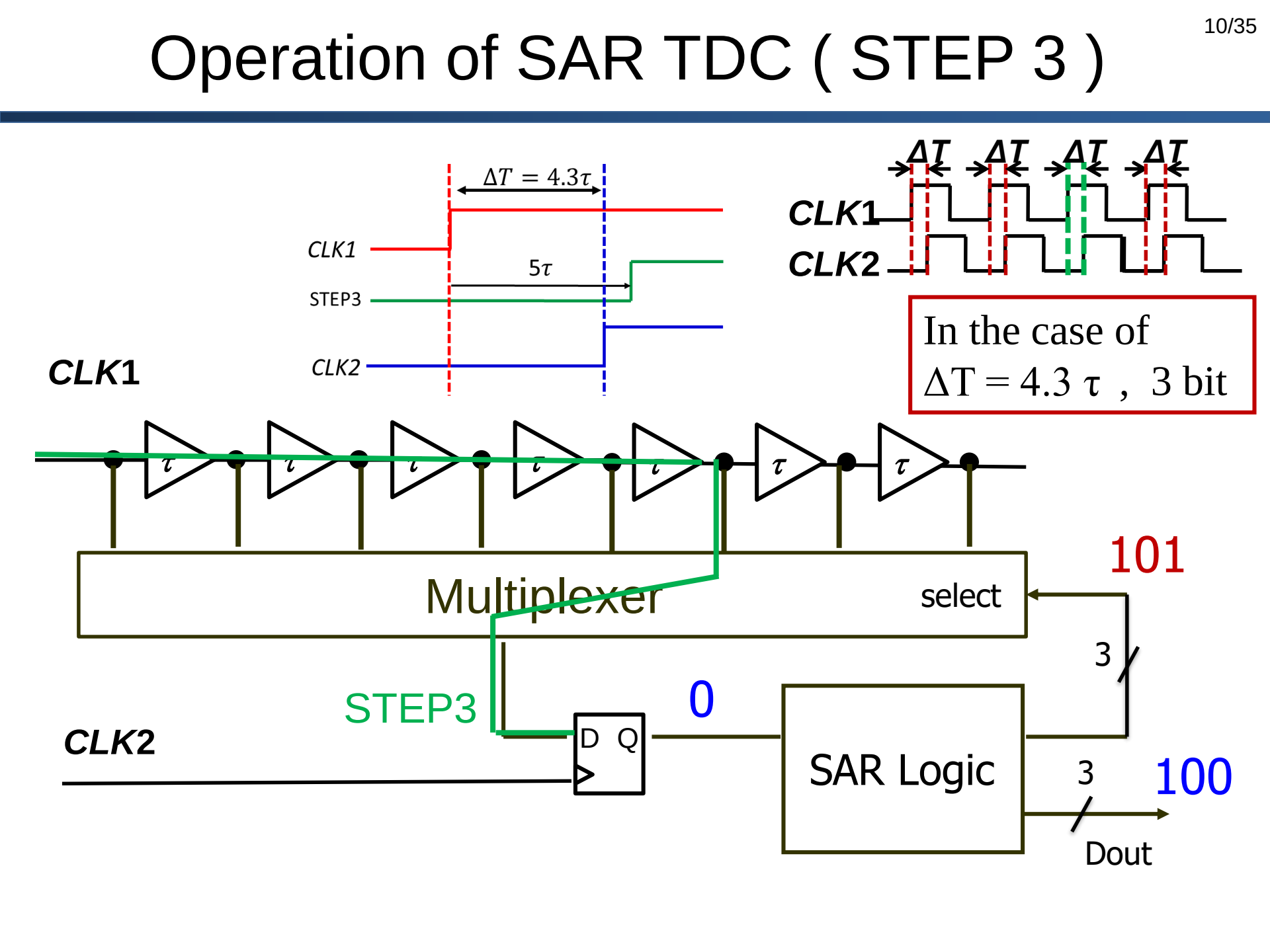
In the case of
$\Delta T = 4.3\ \tau$, 3 bit



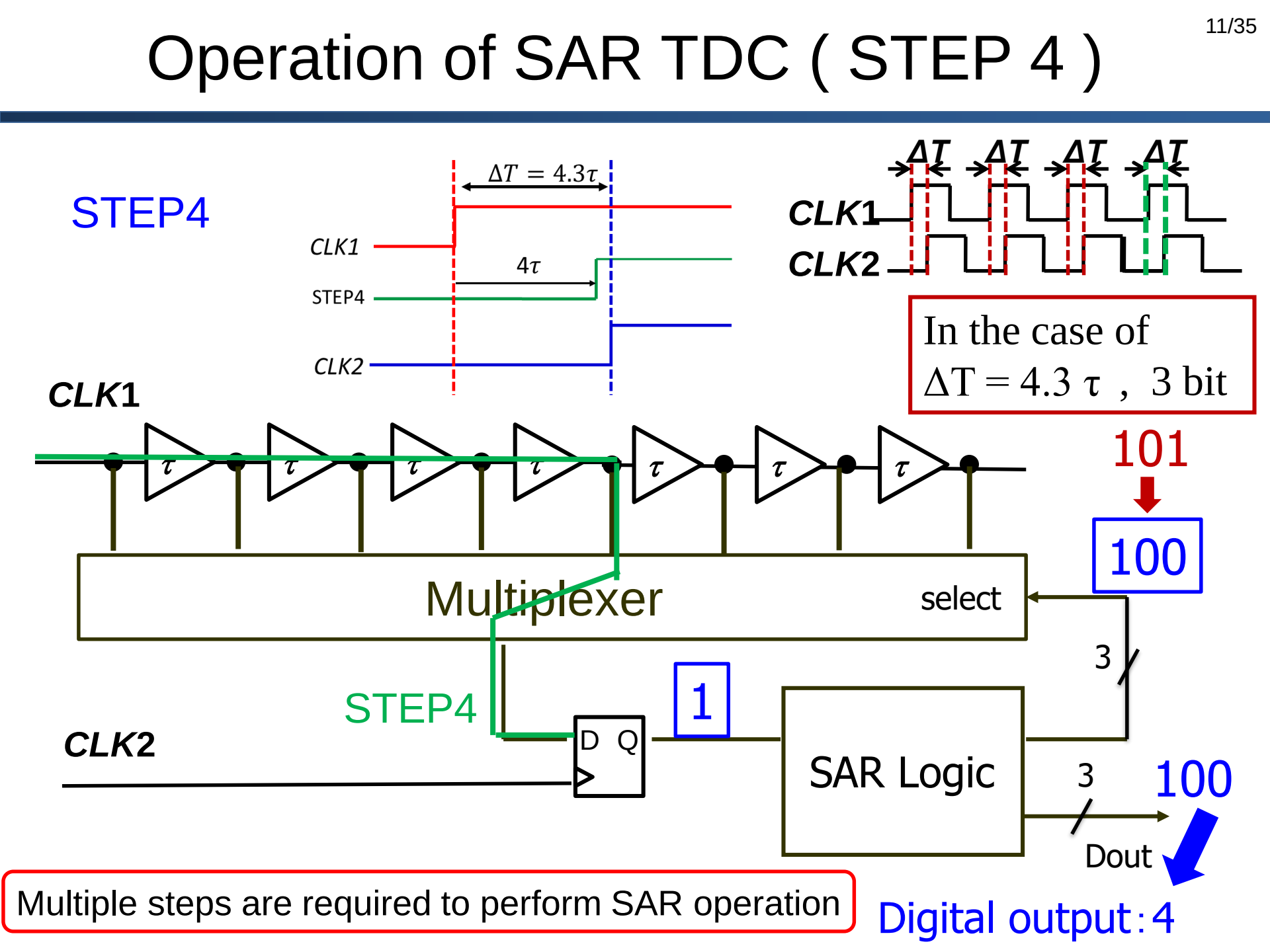
Operation of SAR TDC (STEP 2)



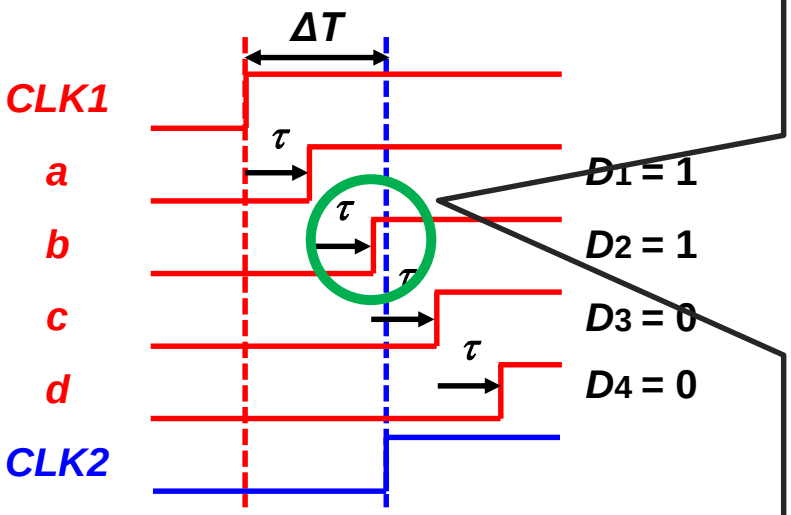
Operation of SAR TDC (STEP 3)



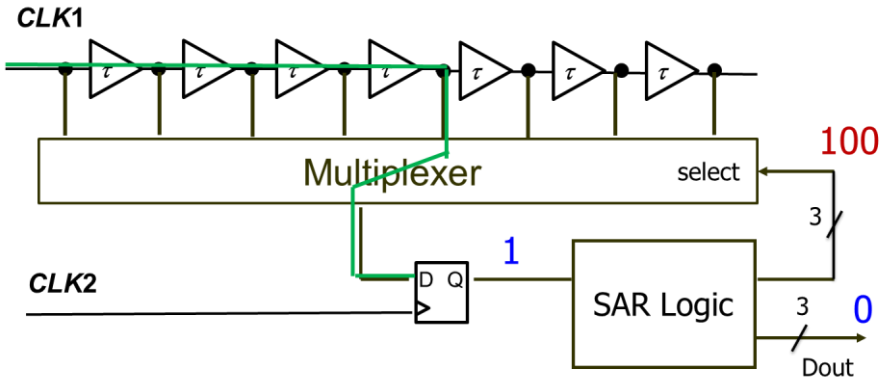
Operation of SAR TDC (STEP 4)

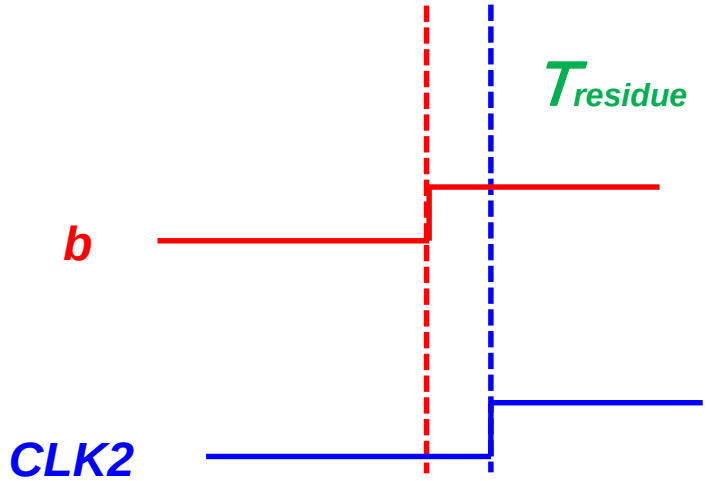


Residual Time



Measurement result of SAR TDC



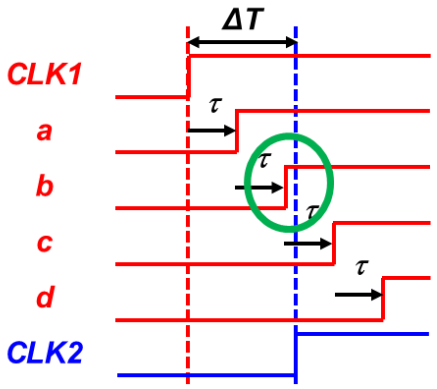


Measurement with residual time at sub TDC

more accurate values

Fine Time Resolution with 2 Step Method

Fine time resolution with 2 step method
SAR＋Vernier-Type TDC

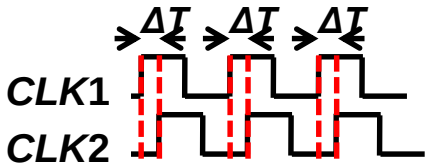


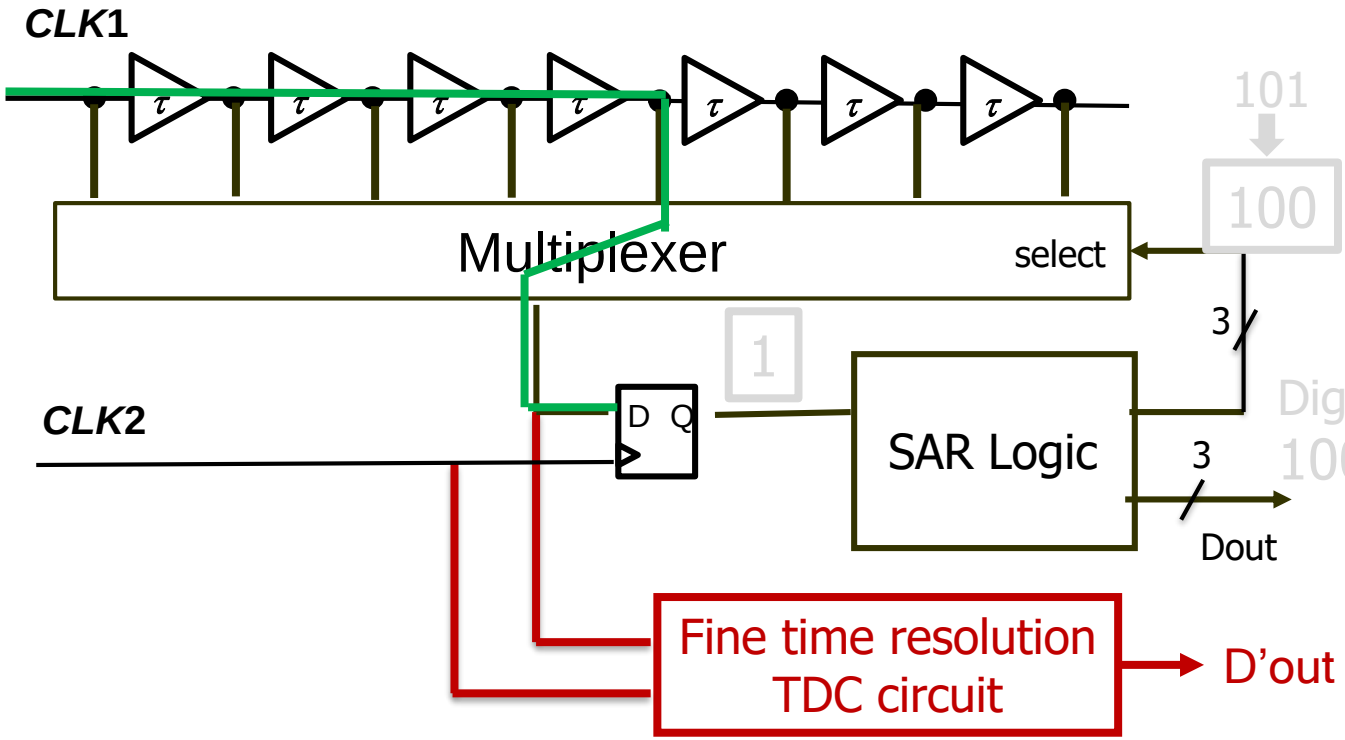
step1：SAR TDC → Integer time | Residual time

step2：SAR +Vernier−type TDC → Measurement of residual time

Fine Time Resolution TDC

In the case of
$\Delta T = 4.3\ \tau$

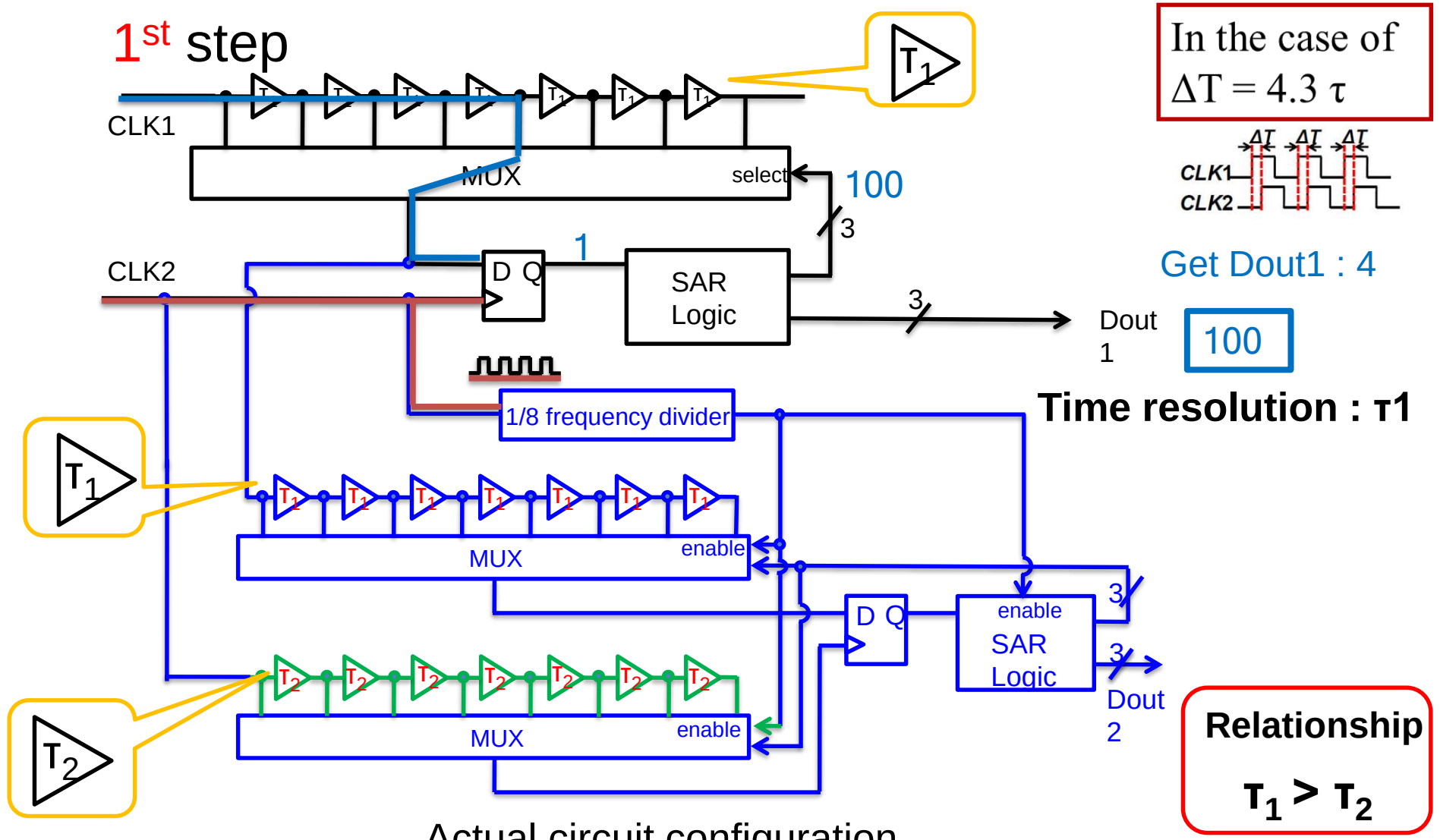




Attach sub TDC to conventional SAR TDC

SAR＋Vernier-Type TDC (1st step)

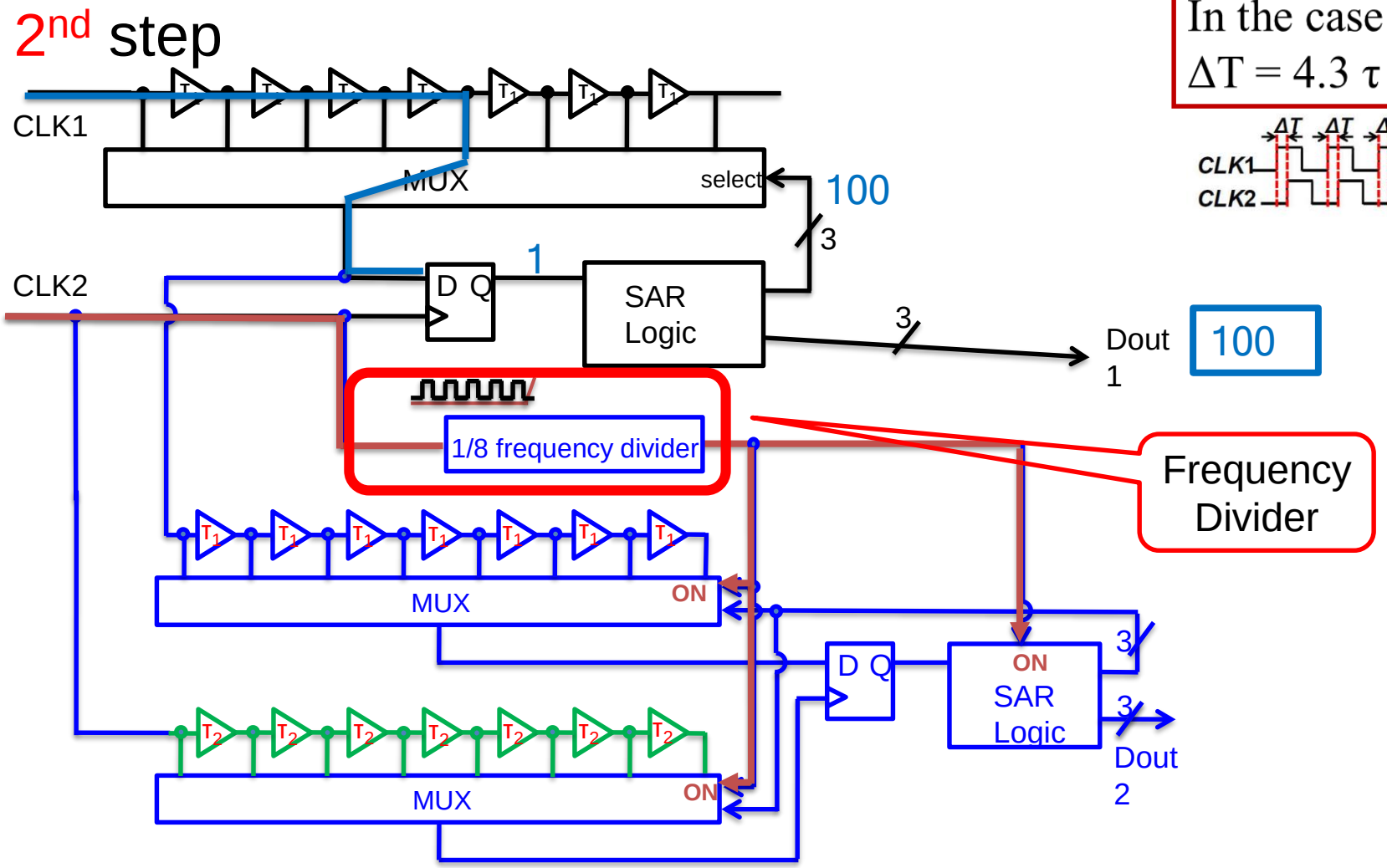
Operation of 3bit SAR＋3bit SAR-Vernier TDC



Actual circuit configuration

SAR＋Vernier-Type TDC (2nd step)

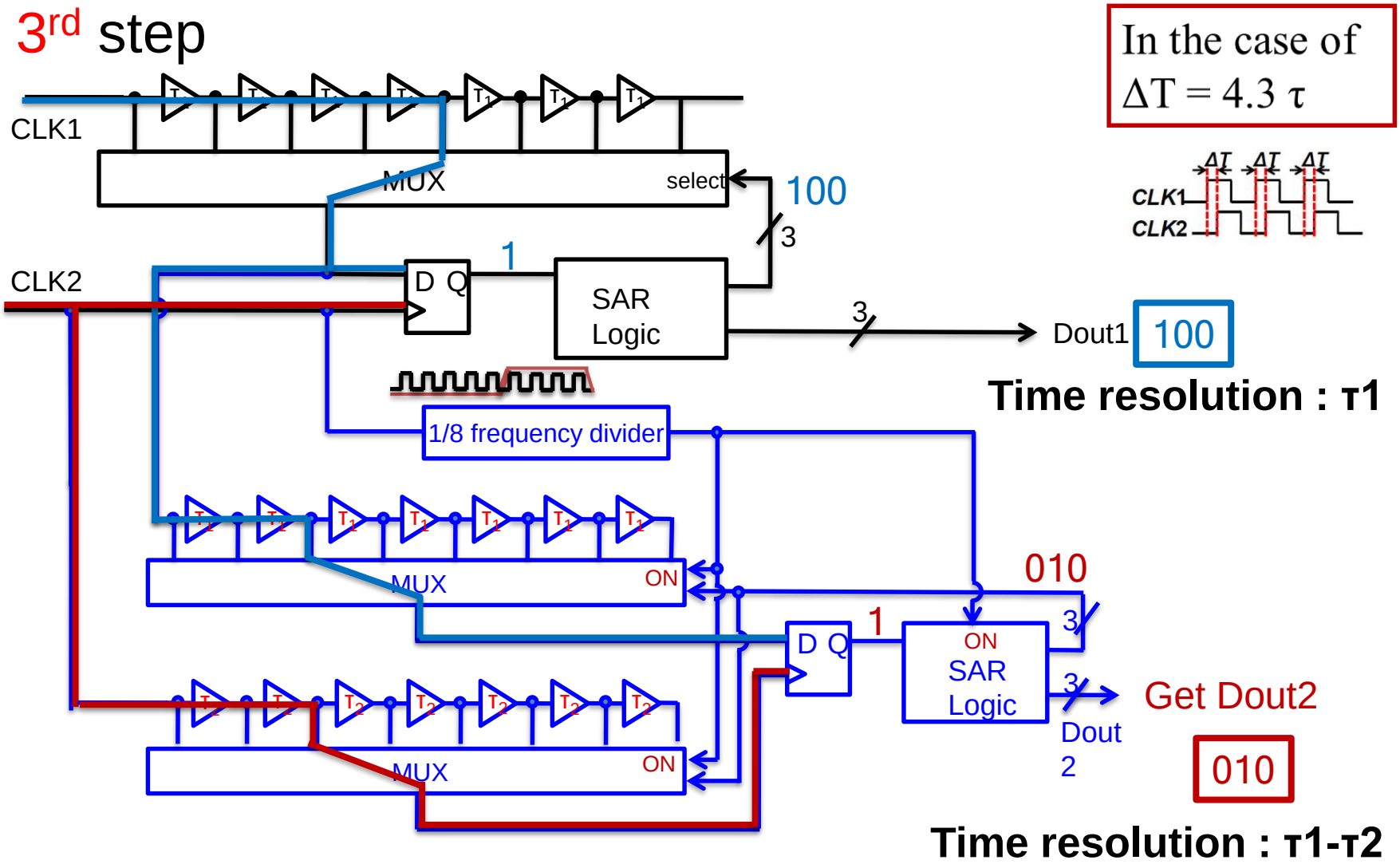
Operation of 3bit SAR＋3bit SAR-Vernier TDC



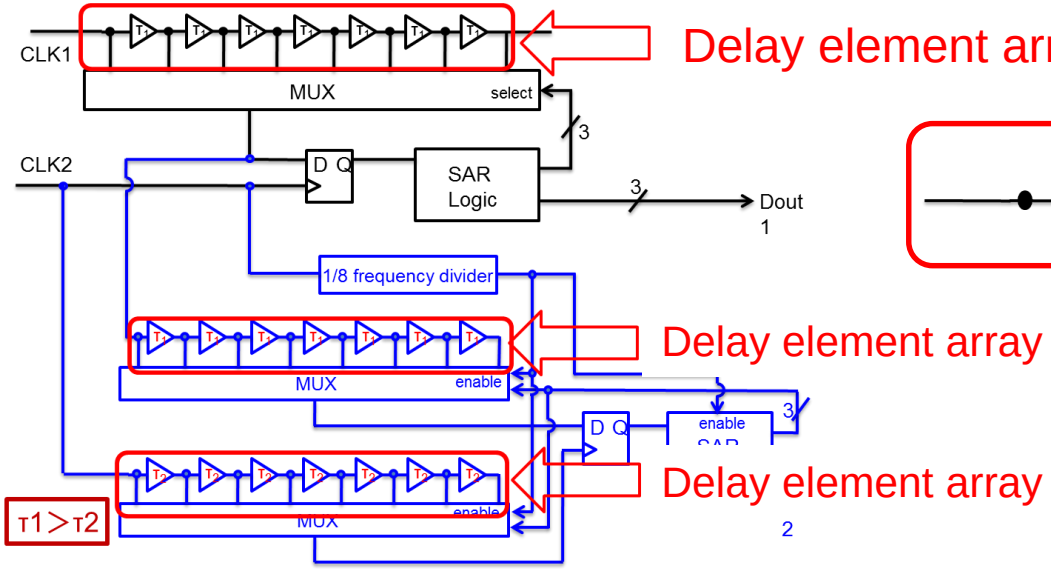
SAR＋Vernier-Type TDC (3rd step)

Operation of 3bit SAR＋3bit SAR-Vernier TDC

3rd step

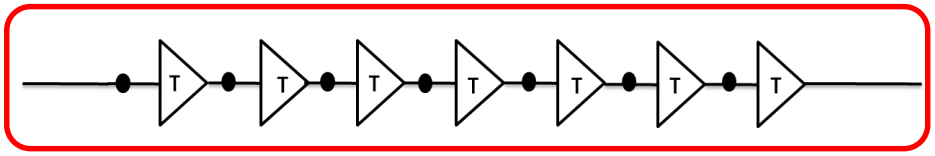


Purpose of Self Calibration



Delay element array

Delay element array



Delay element array

The average delay value of the delay array varies

- Process
- Supply voltage
- Temperature

→ Relative variation

Focus

- Overall delay element delay

→ Absolute variation

Generation of Reference Clock

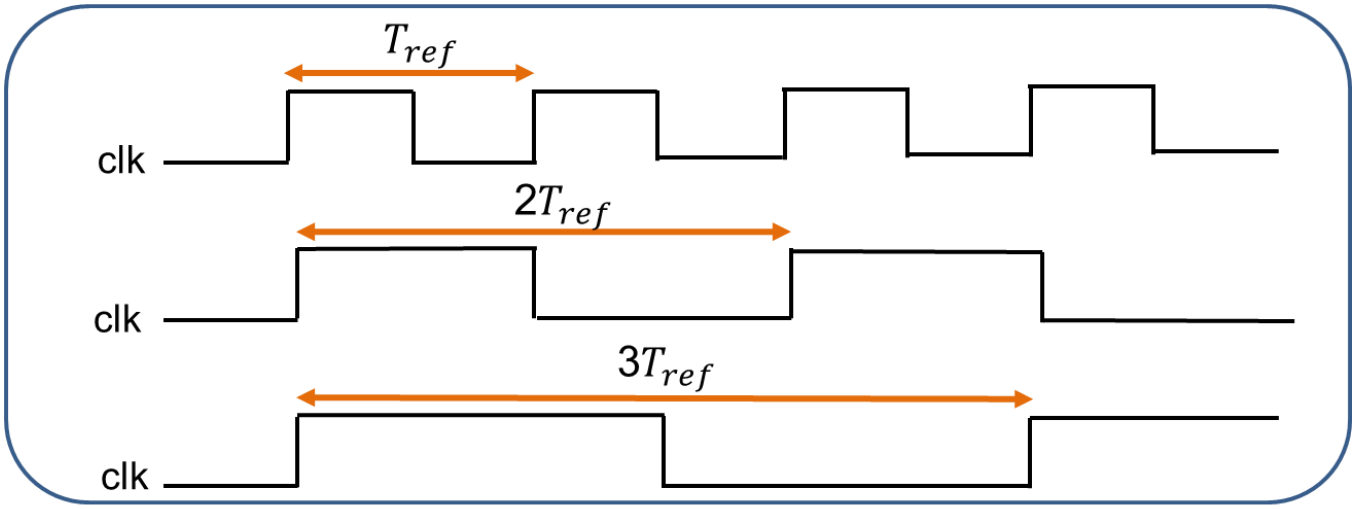
self calibration

↓

Reference clock required

↓

Reference clock can be generated



Time (Tref) can be easily and accurately generated

Calibration Algorithm in 2 step SAR TDC

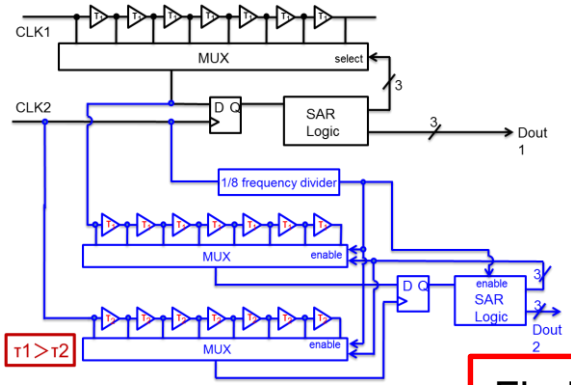
Example of "Number of samples: 3"

$n_{\blacksquare}$, $m_{\blacksquare}$:outout data
$T_{\blacksquare}$:Known input data

$$\begin{cases} n_A\tau_1 + m_A\tau_3 \cong T_1 \\ n_B\tau_1 + m_B\tau_3 \cong T_2 \\ n_C\tau_1 + m_C\tau_3 \cong T_3 \end{cases}$$

※ $\tau_3=\tau_1-\tau_2$

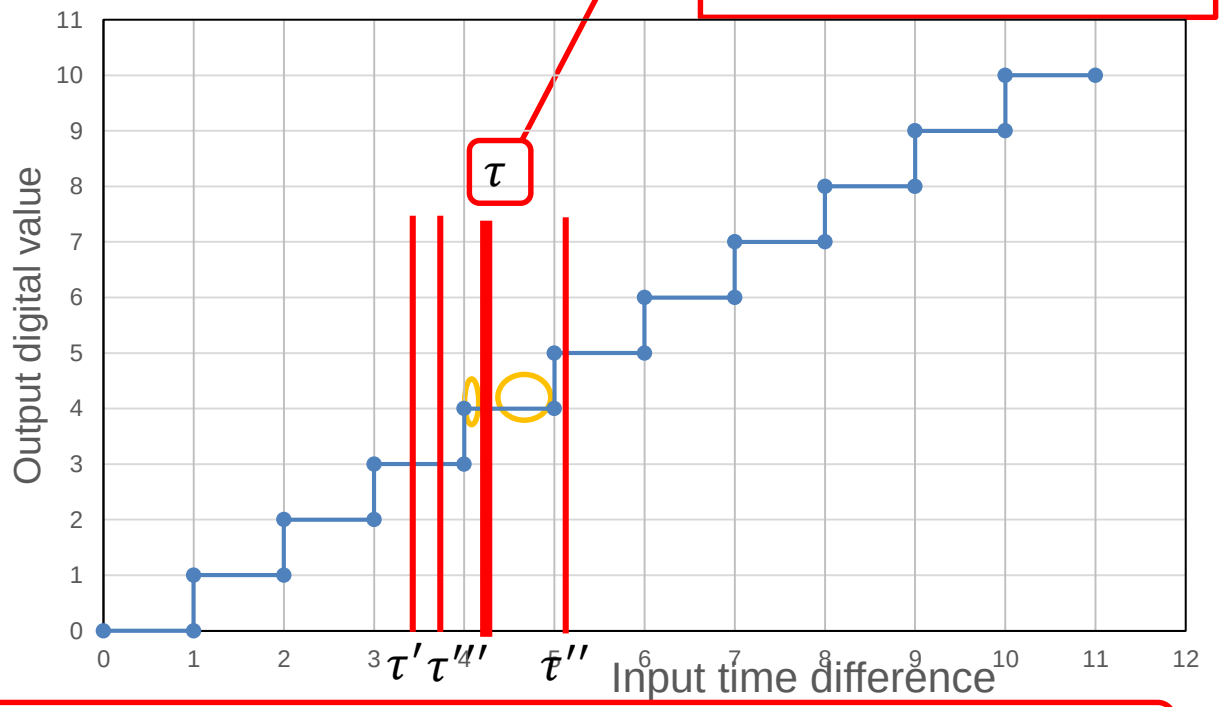
$$\begin{cases} \tau' = m_1\tau_1 + n_1\tau_3 \doteqdot T_1 \\ \tau'' = m_2\tau_1 + n_2\tau_3 \doteqdot T_2 \\ \tau''' = m_3\tau_1 + n_3\tau_3 \doteqdot T_3 \end{cases}$$



D_{OUT1} → $n_{\blacksquare}$

D_{OUT2} → $m_{\blacksquare}$

Find the exact value of τ



This time, $\tau_1(=1.0)$, $\tau_3(=0.1)$ is virtually set, comparison and evaluation

Measurement Error with Respect to Estimate

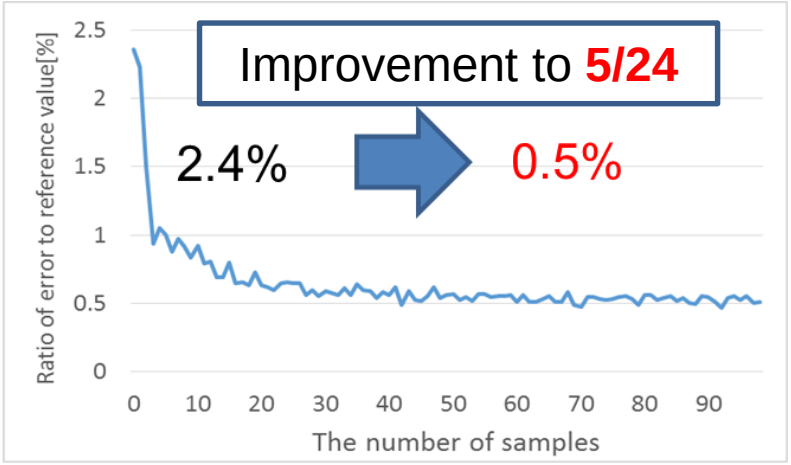
In case of τ_1

number of samples is "2"

About 2.4%

number of samples is“100“

About 0.5%



Measurement error with respect to the estimate of τ_1

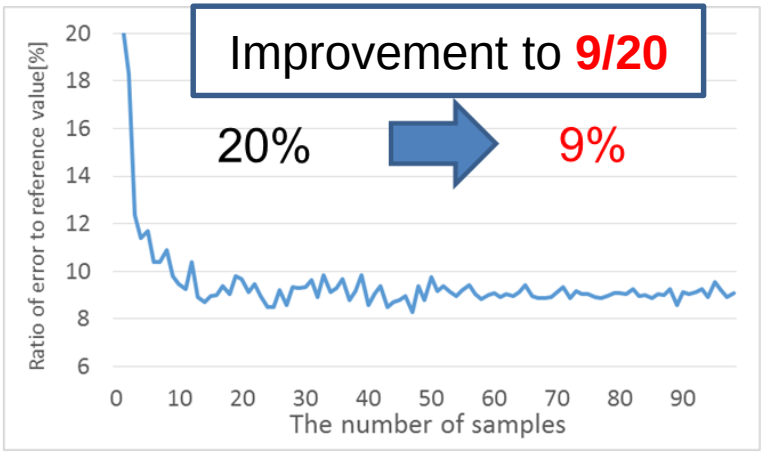
In case of τ_3

number of samples is "2“

About 20.0%

number of samples is“100“

About 9.0%



Measurement error with respect to the estimate of τ_3

$(\tau_3 = \tau_1 - \tau_2)$

Variation of Error with Respect to Estimated Value

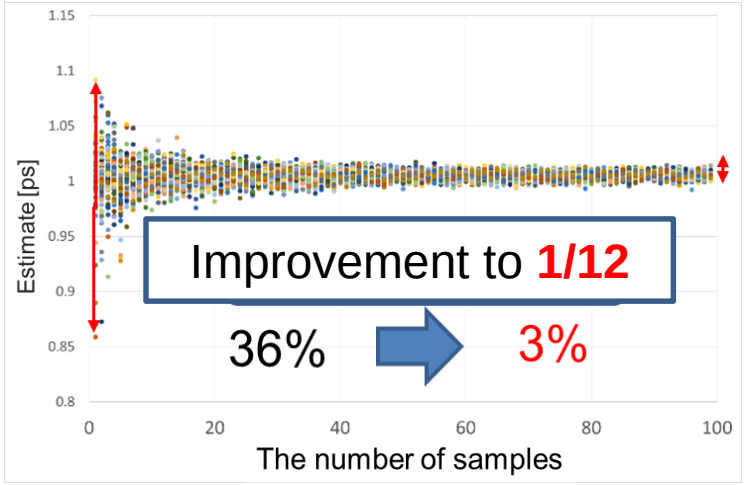
In case of $\tau_1 (= 1.0)$

the number of samples is " 2 "

0.86(-14%) ~ 1.08(+22%)

the number of samples is " 100 "

0.98(-2%) ~ 1.01(+1%)



Error variation with respect to τ_1

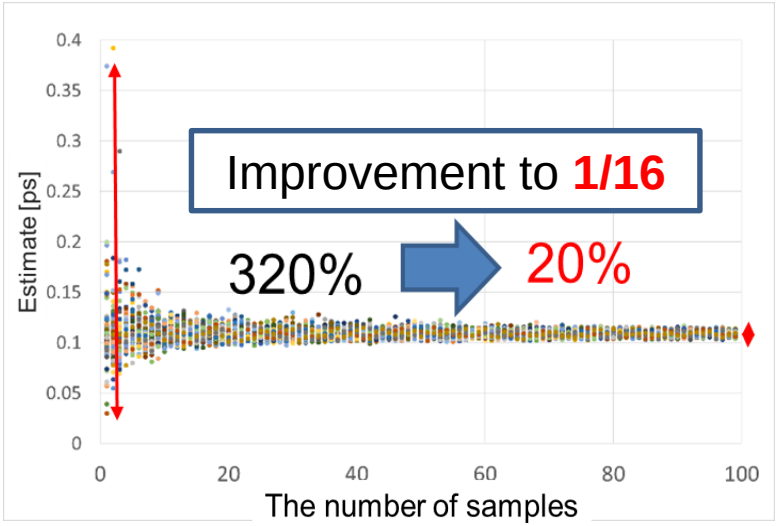
In case of $\tau_3 (= 0.1)$

the number of samples is " 2 "

0.03(-70%) ~ 0.35(+250%)

the number of samples is " 100 "

0.1(0%) ~ 0.12(20%)



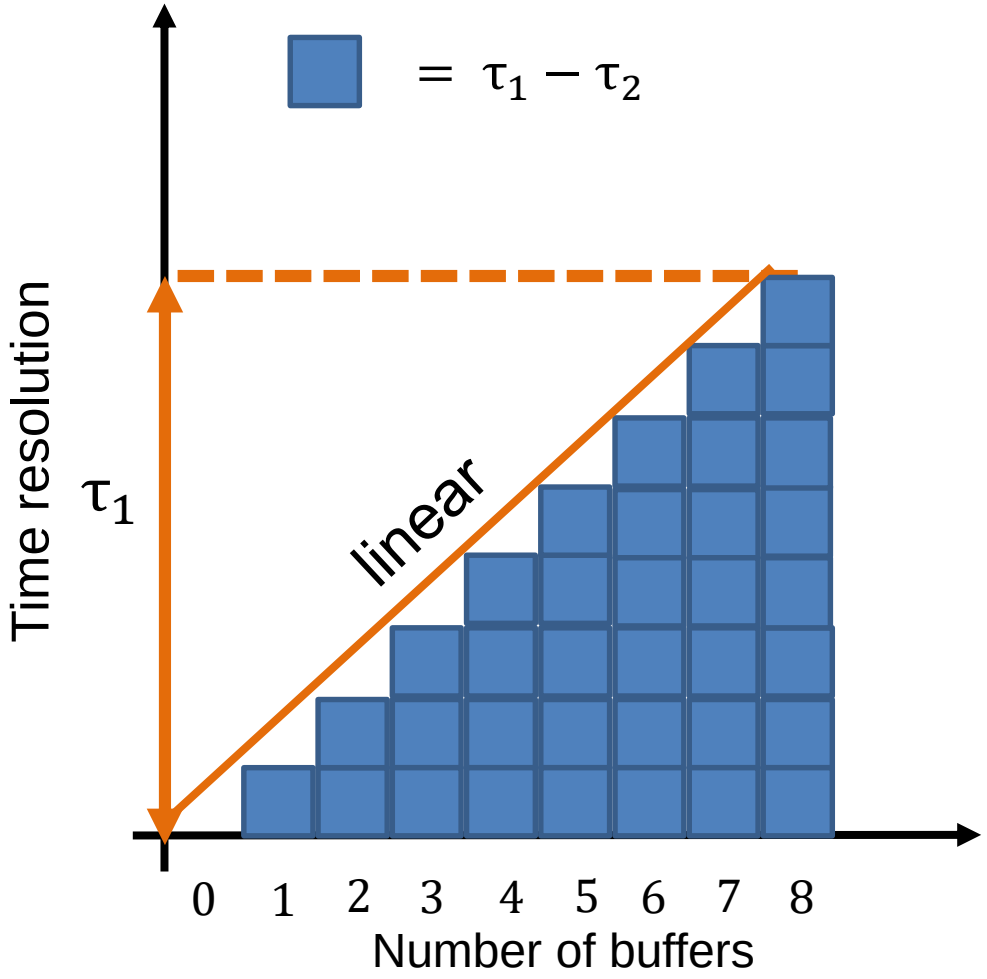
Error variation with respect to τ_3

The reliability improves as the number of samples increases

SAR + Vernier TDC Linearity Problem

Define as ideal

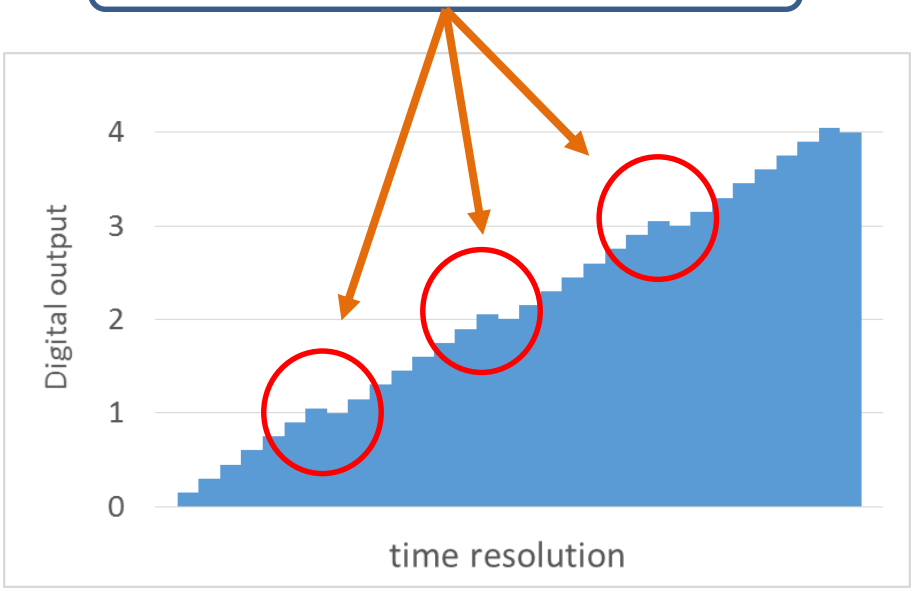
$$\frac{1}{8}\tau_1 = \tau_1 - \tau_2$$



Gap between Real and Ideal

$$\frac{1}{8}\tau_1 < \tau_1 - \tau_2$$

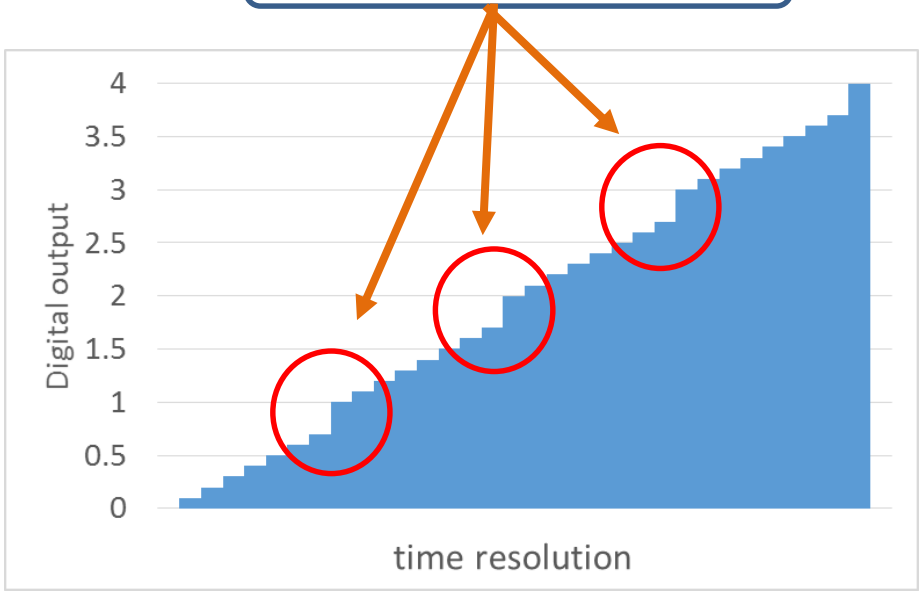
Reversal phenomenon occurs



$\tau_1 = 1.0$, $\tau_1 - \tau_2 = 0.12$

$$\frac{1}{8}\tau_1 > \tau_1 - \tau_2$$

The linearity collapses



$\tau_1 = 1.0$, $\tau_1 - \tau_2 = 0.08$

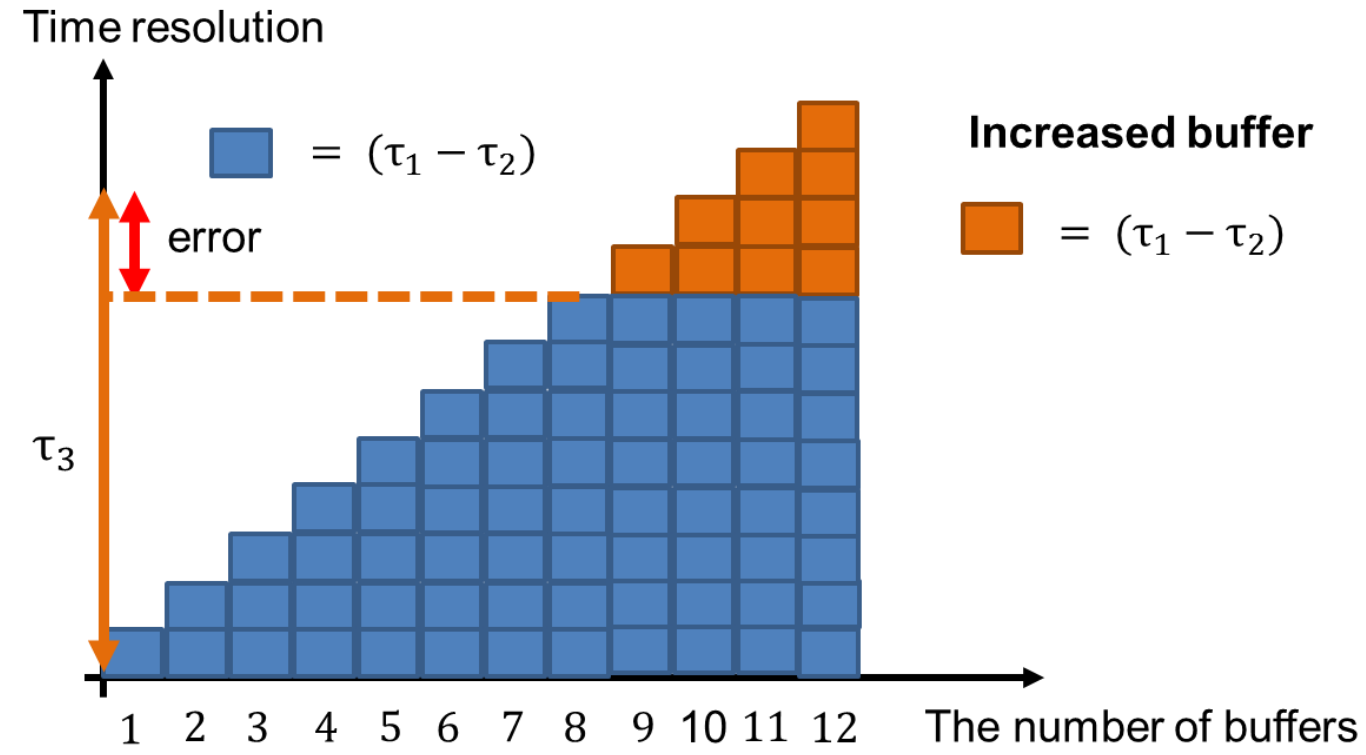
Occurs when the integer part switches

Extra Buffers

τ2 is deliberately set to
(1/8) τ1 > (τ1− τ2)

Extra buffers

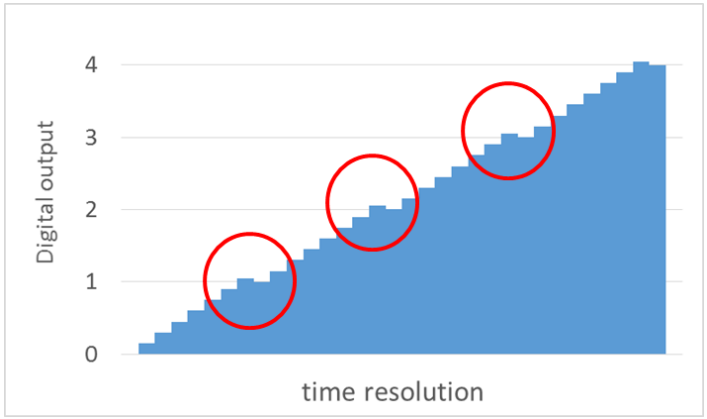
When $\tau_1 - \tau_2 < \tau_3$

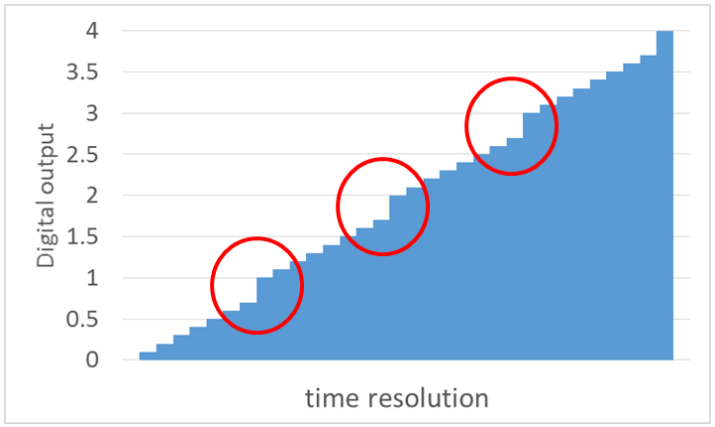


Make Redundancy

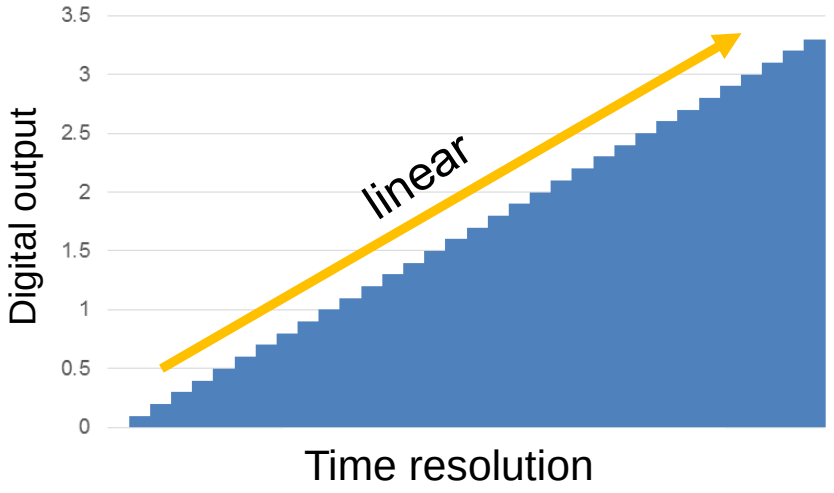
Self-calibration → Estimate time resolution → Selection of number of buffers

Increased buffer + τ_2 setting : $(\frac{1}{8}\tau_1 < \tau_1 - \tau_2)$

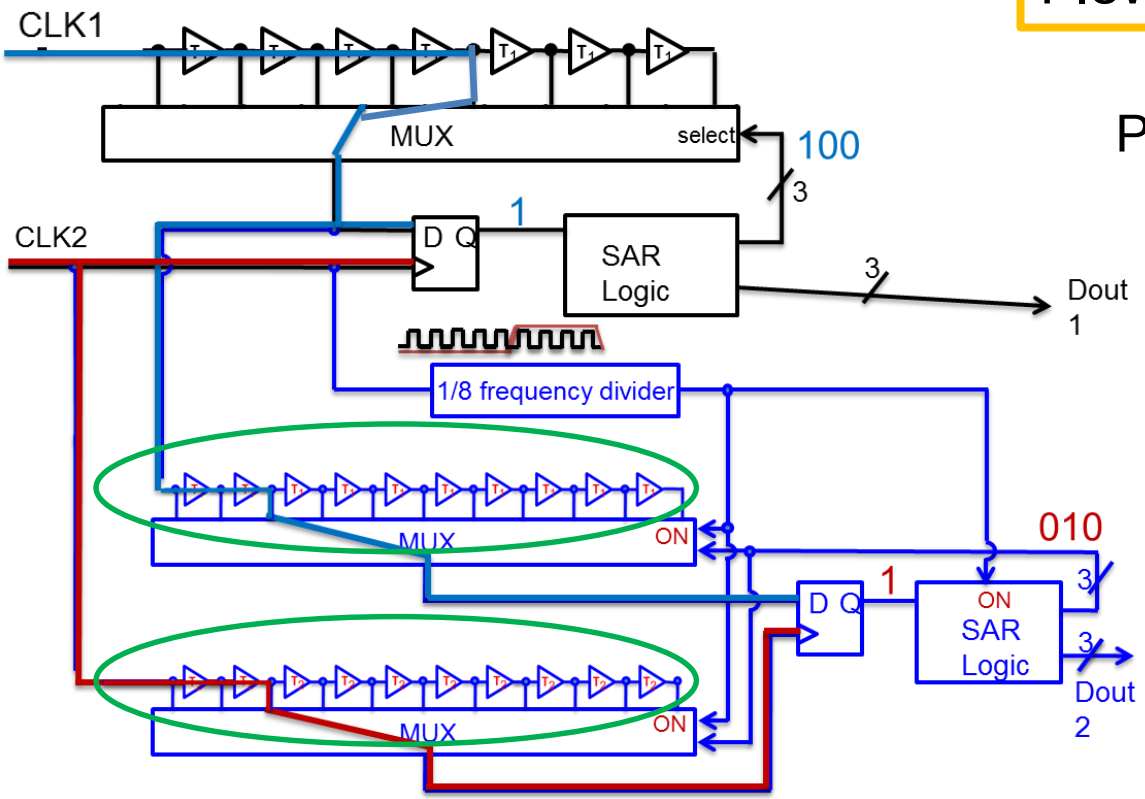




Possible to maintain linearity



Circuit configuration with redundancy



SAR + Vernier TDC

Flow of self calibration overall

Place extra delay elements

↓

self calibration

↓

Select number of buffers

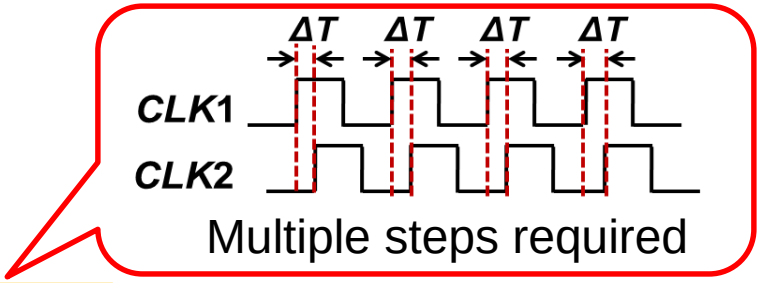
↓

Can maintain linearity

Problems in Operation of SAR

During measurement

The necessity to always input certain time difference



Input signal → **SAR TDC** → Output signal

Circuit approach to problem

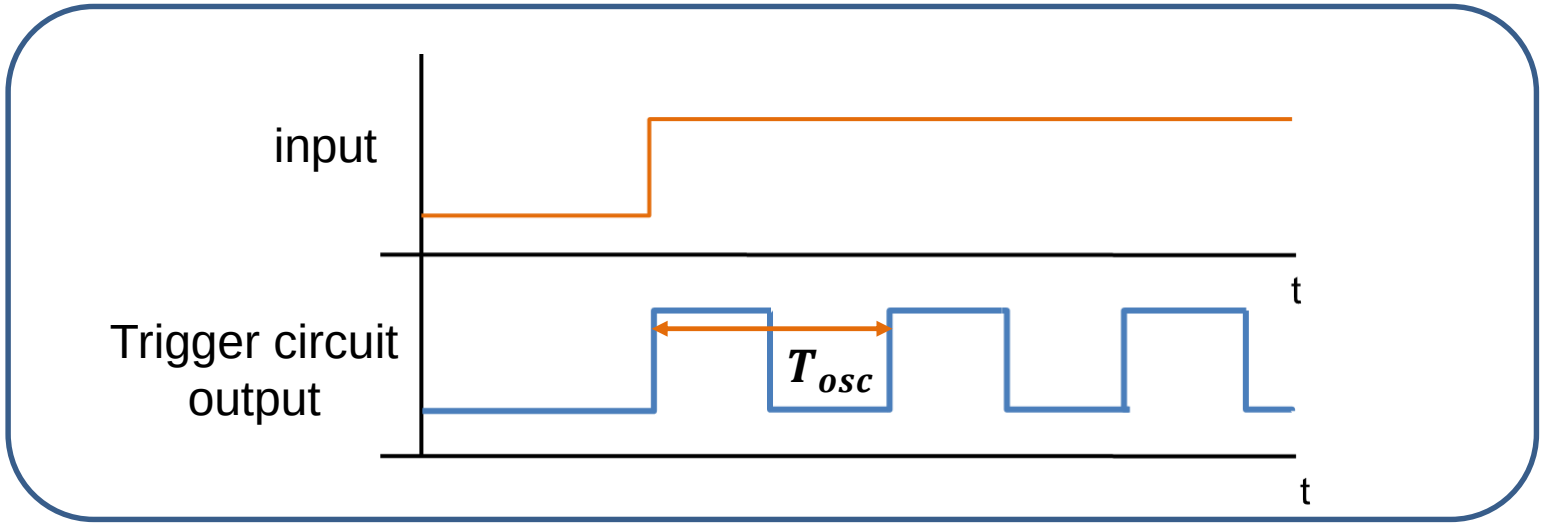
Accuracy is good

Digital ⇔ Analog

What is Trigger Circuit ?

Trigger circuit : Digital circuit with two thresholds

"Circuit that oscillates with constant phase
with zero phase at input timing signal "

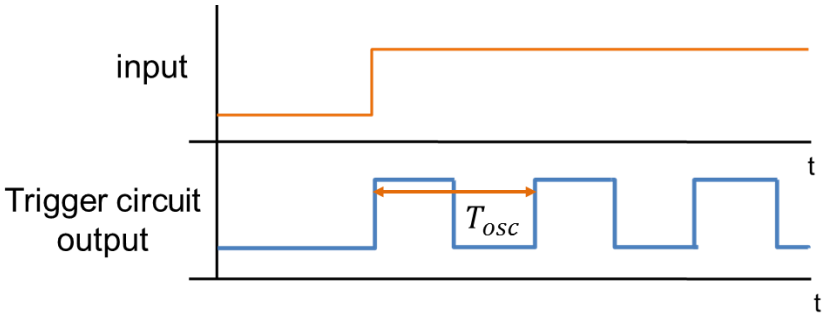


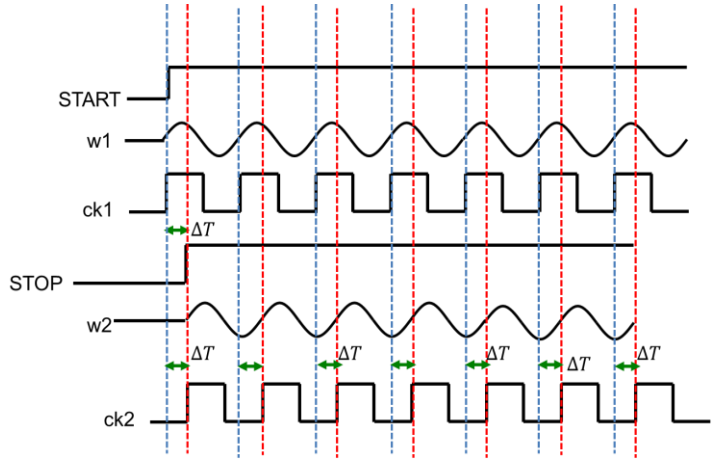
Voltage Signal & Time signal

Conventional

○ Voltage signals can be held

× Time signal difference can not be held





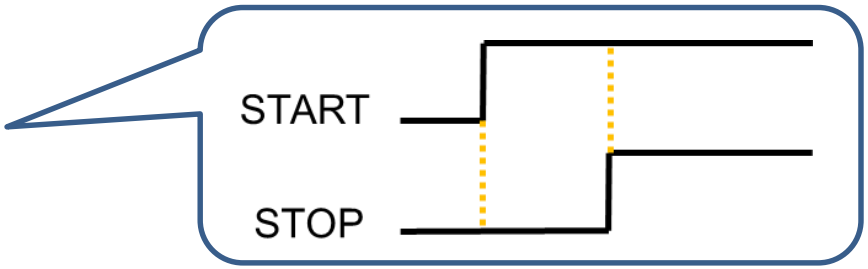
Proposal

○ Time signal difference can be held

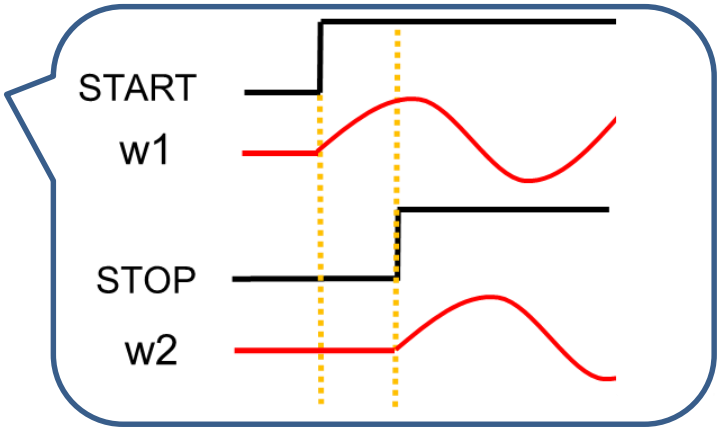
Single-shot Timing Measurement Using Trigger Circuit

Proposal

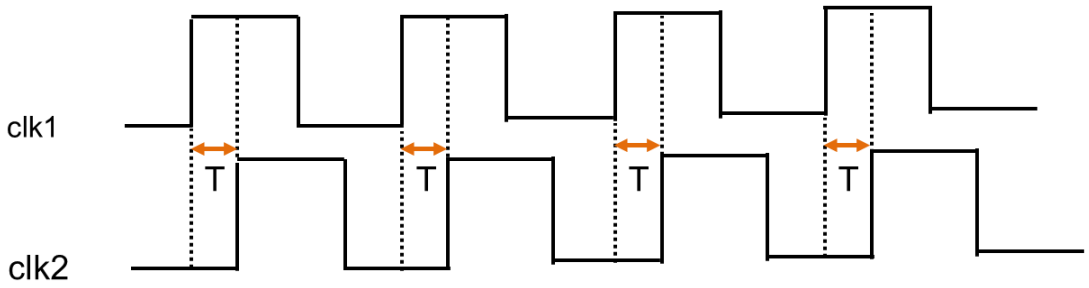
Enter START & STOP signals



Oscillation start at initial phase determined



Time signal difference can be held

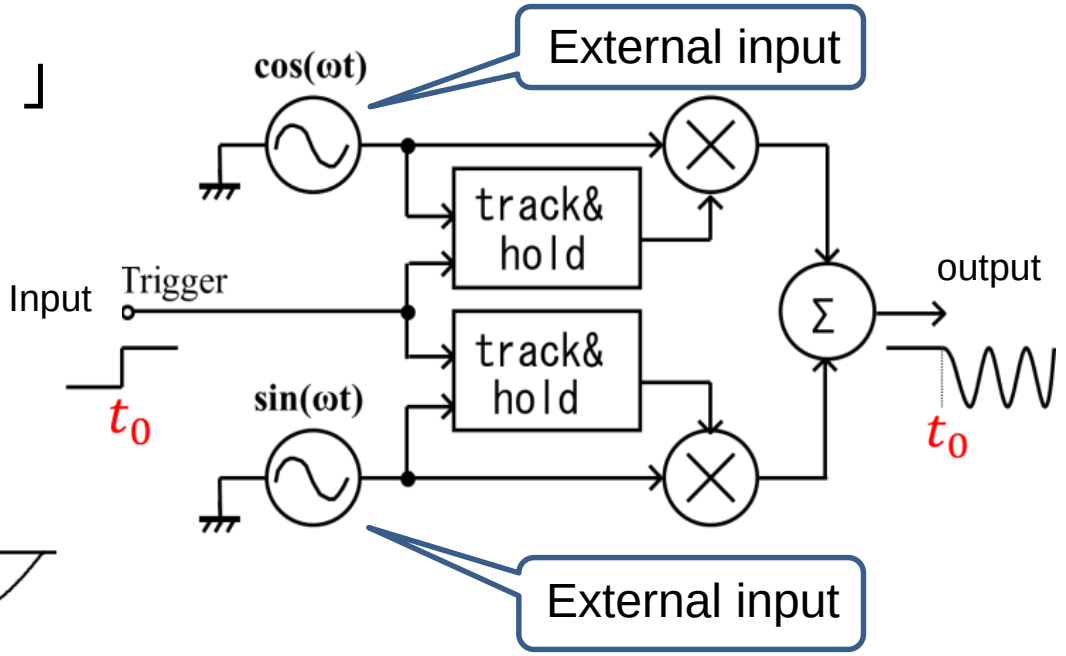


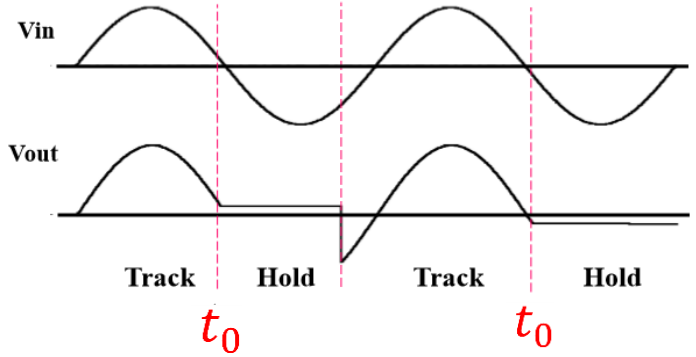
SAR TDC requires multiple steps

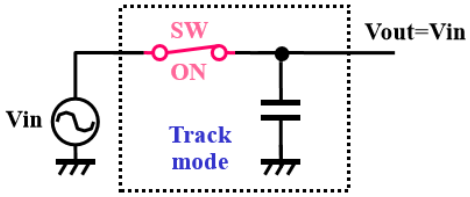
Can measure one-shot signal by using trigger circuit in front of SAR TDC

Trigger Circuit example

「 Trigger circuit example 」

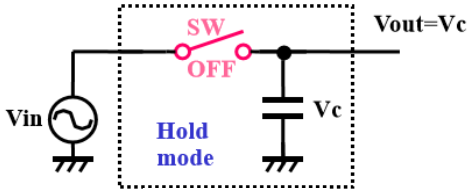






T/H circuit

Output the input signal



T/H circuit

C holds Vin and outputs

track and hold circuit

・**track mode**

$$Vout=\cos(\omega t)\cos(\omega t)+\cos(\omega t+\pi/2)\ \cos(\omega t+\pi/2)$$
$$=\cos^2(\omega t)+\sin^2(\omega t)$$
$$=1 \quad (\text{一定の値})$$

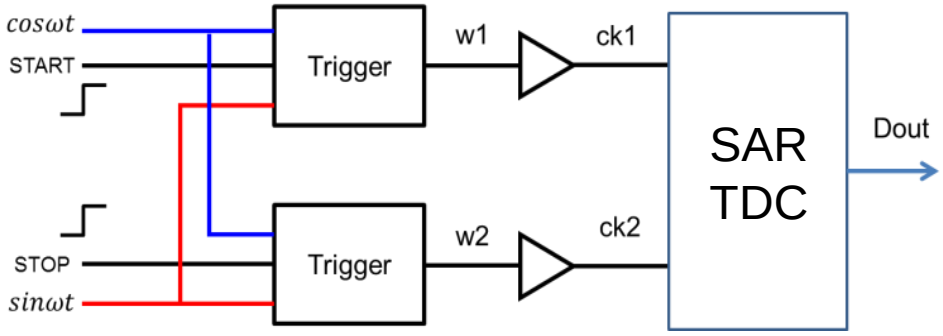
・**hold mode**

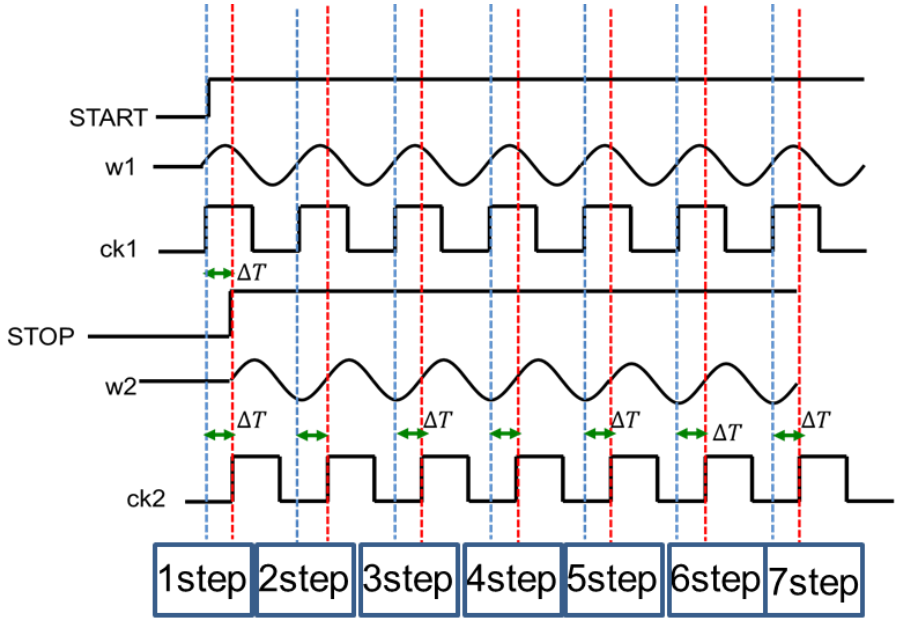
$$Vout=\cos(\omega t)\ \cos(\omega t_0)\ +\sin(\omega t)\sin(\omega t_0)$$
$$=\cos(\omega(t-t_0))$$

※ **trigger time:t_0**

Circuit configuration of One-Shot Measurement

SAR TDC using trigger circuit





Using trigger circuit and inverter

one shot (start & stop) signal

Time difference can be held

Can operate with SAR TDC with one time difference

Our Research Results

Research subject

- Fine time resolution and high linearity TDC circuit with small circuit / low power consumption
- Enable single-shot timing measurement with SAR TDC

Achievement

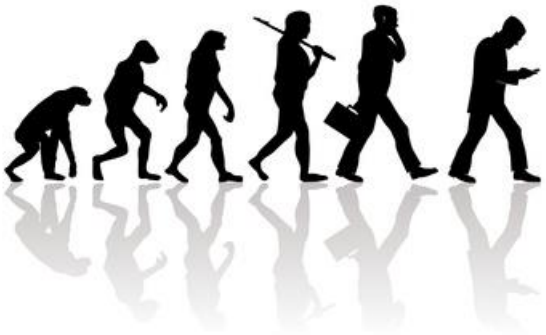
- Fine time resolution circuit configuration
- Self calibration in absolute error
- Improve circuit linearity with buffer redundancy for two-step SAR TDC
- One-shot timing measurement using trigger circuit

Thank You for Listening

「 此一时，彼一时 」

孟子（公孙丑下）

The times always change



However …

Time is always constant