Architecture of High Performance Successive Approximation Time Digitizer

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OUTLINE

• Research background
• What is TDC ?
• Configuration of SAR TDC
• Fine Time Resolution with 2-step
• Self-calibration for absolute delay variation
• One-shot timing measurement using trigger circuit
• Conclusion
Research Objective

Development of highly-linear, fine time-resolution TDC for high-speed digital I/O interface timing measurement
Background

- **Voltage Resolution**
  - CMOS Scaling
  - Voltage

- **Time Resolution**
  - Time
  - CMOS Scaling

Facing difficulties due to reduced supply voltage

Analog circuit design difficultly

Becoming superior
Role of Time-to-Digital Converter

Time-to-Digital Converter: TDC
measure two time differences, outputs digitally
Innovation

[1] Two – Step SAR TDC
⇒ Fine time resolution

[2] Self – Calibration
⇒ Linear TDC

[3] Trigger Circuit
⇒ One – shot timing measurement
Configuration of SAR TDC

Use multiplexer
Dramatically reduced number of DFFs

Use SAR Logic
Operation loop of circuit

Flash type TDC

SAR TDC
Operation of SAR TDC (STEP 1)

In the case of \( \Delta T = 4.3 \tau \), 3 bit
Operation of SAR TDC (STEP 2)

In the case of $\Delta T = 4.3 \tau$, 3 bit
Operation of SAR TDC (STEP 3)

In the case of $\Delta T = 4.3\,\tau$, 3 bit
Operation of SAR TDC (STEP 4)

In the case of $\Delta T = 4.3 \tau$, 3 bit multiple steps are required to perform SAR operation.

Digital output: 4
Residual Time

Measurement result of SAR TDC

Measurement with residual time at sub TDC

more accurate values
Fine time resolution with 2 step method
SAR + Vernier-Type TDC

step1: SAR TDC → Integer time

step2: SAR + Vernier-type TDC → Residual time

Measurement of residual time
In the case of $\Delta T = 4.3 \tau$

Attach sub TDC to conventional SAR TDC
SAR + Vernier-Type TDC (1st step)

Operation of 3bit SAR + 3bit SAR-Vernier TDC

1st step

CLK1

MUX

CLK2

SAR Logic

DQ

1/8 frequency divider

100

3

Get Dout1 : 4

Time resolution : τ1

In the case of
ΔT = 4.3 τ

Relationship

T1 > T2

Actual circuit configuration
In the case of $\Delta T = 4.3\, \tau$

2nd step

Operation of 3bit SAR + 3bit SAR-Vernier TDC

SAR + Vernier-Type TDC (2nd step)
SAR + Vernier-Type TDC (3rd step)

Operation of 3bit SAR + 3bit SAR-Vernier TDC

3rd step

CLK1

MUX

select

100

CLK2

D Q

SAR Logic

Dout1 100

1/8 frequency divider

MUX

ON

MUX

ON

Dout2 010

Time resolution : τ1

Time resolution : τ1-τ2

In the case of ΔT = 4.3 τ

Operation of 3bit SAR + 3bit SAR-Vernier TDC (3rd step)
Purpose of Self Calibration

- Process
- Supply voltage
- Temperature

The average delay value of the delay array varies:

- Relative variation
- Absolute variation

Focus:

- Overall delay element delay
Generation of Reference Clock

self calibration

Reference clock required

Reference clock can be generated

Time ($T_{ref}$) can be easily and accurately generated
Calibration Algorithm in 2 step SAR TDC

Example of "Number of samples: 3"

\[ n_A \tau_1 + m_A \tau_3 \cong T_1 \]
\[ n_B \tau_1 + m_B \tau_3 \cong T_2 \]
\[ n_C \tau_1 + m_C \tau_3 \cong T_3 \]

\[ \tau'_0 = m_1 \tau_1 + n_1 \tau_3 \div T_1 \]
\[ \tau''_0 = m_2 \tau_1 + n_2 \tau_3 \div T_2 \]
\[ \tau'''_0 = m_3 \tau_1 + n_3 \tau_3 \div T_3 \]

Find the exact value of \( \tau \)

This time, \( \tau_1 (= 1.0) \), \( \tau_3 (= 0.1) \) is virtually set, comparison and evaluation
Measurement Error with Respect to Estimate

**In case of $\tau_1$**
- Number of samples is "2"
  - About 2.4%
- Number of samples is "100"
  - About 0.5%

**In case of $\tau_3$**
- Number of samples is "2"
  - About 20.0%
- Number of samples is "100"
  - About 9.0%

**Improvement to $5/24$**
- 2.4% to 0.5%

**Improvement to $9/20$**
- 20% to 9%
Variation of Error with Respect to Estimated Value

In case of $\tau_1(=1.0)$

- The number of samples is "2"
  - $0.86(-14\%) \sim 1.08(+22\%)

- The number of samples is "100"
  - $0.98(-2\%) \sim 1.01(+1\%)

In case of $\tau_3(=0.1)$

- The number of samples is "2"
  - $0.03(-70\%) \sim 0.35(+250\%)

- The number of samples is "100"
  - $0.1(0\%) \sim 0.12(20\%)

Error variation with respect to $\tau_1$
- Improvement to $\frac{1}{12}$
  - 36\% → 3\%

Error variation with respect to $\tau_3$
- Improvement to $\frac{1}{16}$
  - 320\% → 20\%

The reliability improves as the number of samples increases.
Define as ideal

\[
\frac{1}{8} \tau_1 = \tau_1 - \tau_2
\]
Gap between Real and Ideal

\[ \frac{1}{8} \tau_1 < \tau_1 - \tau_2 \]

Reversal phenomenon occurs

\[ \frac{1}{8} \tau_1 > \tau_1 - \tau_2 \]

The linearity collapses

\[ \tau_1 = 1.0, \tau_1 - \tau_2 = 0.12 \]

\[ \tau_1 = 1.0, \tau_1 - \tau_2 = 0.08 \]

Occurs when the integer part switches
Extra Buffers

τ₂ is deliberately set to

\( (1/8) \tau_1 > (\tau_1 - \tau_2) \)

Extra buffers

When \( \tau_1 - \tau_2 < \tau_3 \)

Time resolution

\[ \text{error} = (\tau_1 - \tau_2) \]

Increased buffer

\[ \text{Increased buffer} = (\tau_1 - \tau_2) \]

The number of buffers
Make Redundancy

Self-calibration → Estimate time resolution → Selection of number of buffers

Increased buffer + $\tau_2$ setting : \( \left( \frac{1}{8} \tau_1 < \tau_1 - \tau_2 \right) \)

Possible to maintain linearity
Circuit configuration with redundancy

Flow of self calibration overall

Place extra delay elements

self calibration

Select number of buffers

Can maintain linearity

SAR + Vernier TDC
Problems in Operation of SAR

During measurement

The necessity to **always input certain time difference**

Input signal \(\rightarrow\) SAR TDC \(\rightarrow\) Output signal

Circuit approach to problem

Digital \(\leftrightarrow\) Analog

Accuracy is good

Multiple steps required
What is Trigger Circuit?

**Trigger circuit**: Digital circuit with two thresholds

"Circuit that oscillates with constant phase with zero phase at input timing signal “
Voltage Signal & Time signal

**Conventional**

Voltage signals *can* be held

Time signal difference *cannot* be held

**Proposal**

Time signal difference *can* be held
Single-shot Timing Measurement Using Trigger Circuit

Proposal

Enter START & STOP signals

Oscillation start at initial phase determined

Time signal difference can be held

SAR TDC requires multiple steps

Can measure one-shot signal by using trigger circuit in front of SAR TDC
Trigger Circuit example

「 Trigger circuit example 」

**Track and hold circuit**

- **Track mode**
  
  \[ V_{out} = \cos(\omega t) \cos(\omega t) + \cos(\omega t + \pi/2) \cos(\omega t) \]

  \[ = \cos^2(\omega t) + \sin^2(\omega t) \]

  \[ = 1 \quad \text{(一定的値)} \]

- **Hold mode**

  \[ V_{out} = \cos(\omega t) \cos(\omega t_0) + \sin(\omega t) \sin(\omega t_0) \]

  \[ = \cos(\omega (t-t_0)) \]

  ※ trigger time: \( t_0 \)

- Output the input signal
- C holds \( V_{in} \) and outputs

Vin

\[ \begin{array}{c}
\text{Vin} \\
\text{Vout} \\
\end{array} \]

\[ \begin{array}{c}
\text{Track} \\
\text{Hold} \\
\text{Track} \\
\text{Hold} \\
\end{array} \]

Input

Trigger

\( t_0 \)

External input

\[ \begin{array}{c}
\text{cos}(\omega t) \\
\text{sin}(\omega t) \\
\end{array} \]

\[ \begin{array}{c}
\text{track} \& \text{hold} \\
\text{track} \& \text{hold} \\
\end{array} \]

\( \Sigma \)

Output

\( t_0 \)

External input
Circuit configuration of One-Shot Measurement

SAR TDC using trigger circuit

Using trigger circuit and inverter

one shot ( start & stop ) signal

Time difference can be held

Can operate with SAR TDC with one time difference
Our Research Results

Research subject

- Fine time resolution and high linearity TDC circuit with small circuit / low power consumption
- Enable single-shot timing measurement with SAR TDC

Achievement

- Fine time resolution circuit configuration
- Self calibration in absolute error
- Improve circuit linearity with buffer redundancy for two-step SAR TDC
- One-shot timing measurement using trigger circuit
The times always change

However …

Time is always constant

孟子（公孫丑下）

「此一时，彼一时」

Thank You for Listening