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Nov. 8 WP-L2 14:30-15:50

SAR TDC Architecture for One-Shot Timing Measurement with Full Digital Implementation

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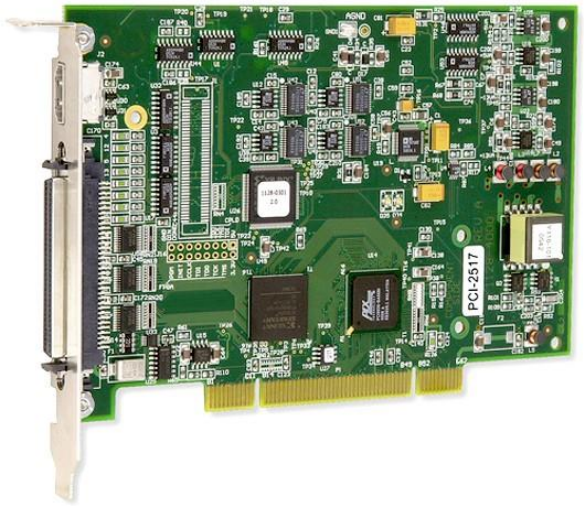
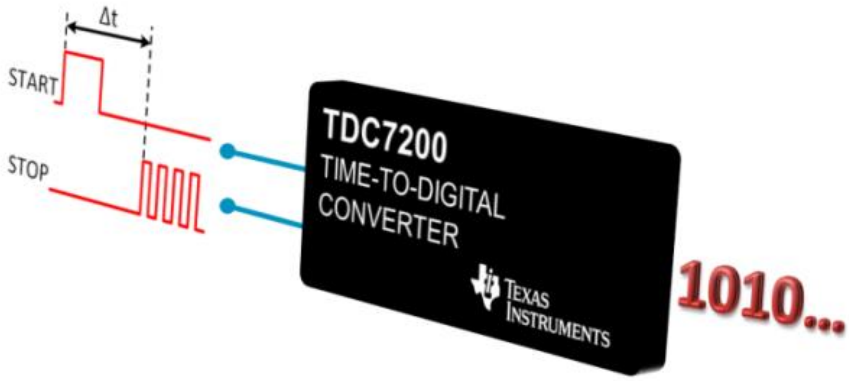
Objective

Development of
highly-linear, fine time-resolution TDC
for high-speed digital I/O interface timing measurement

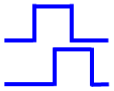




Innovation

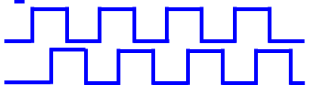
- ✓ **Trigger Circuit**

  One-shot timing measurement

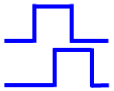
  &

  Good for low frequency repetitive timing

- ✓ **Ring Oscillator**

  One-shot timing measurement

  &

  Good for high & low frequency repetitive timing

Approach

SAR TDC

SAR TDC + Trigger Circuit

- Measure one-shot timing
- Include analog circuit

SAR TDC + Ring Oscillator

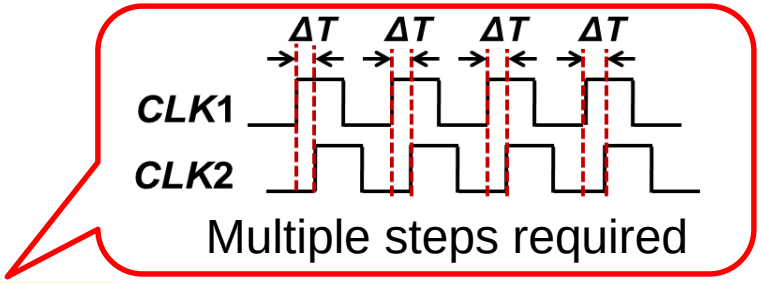
- Measure one-shot timing
- Without analog circuit

Full digital FPGA implementation

Problems in Operation of SAR

During measurement

The necessity to always input certain time difference



Input signal → **SAR TDC** → Output signal

Circuit approach to problem

Digital ⟺ Analog

Outline

- Research Objective
- Conventional TDC Architecture
  - Flash TDC
- SAR TDC Architecture & Operation
- Proposed SAR TDC – Analog Centric
- Proposed SAR TDC – Digital Centric
  - Architecture & Operation
  - High Frequency
  - Low Frequency
  - Simulation
- Conclusion

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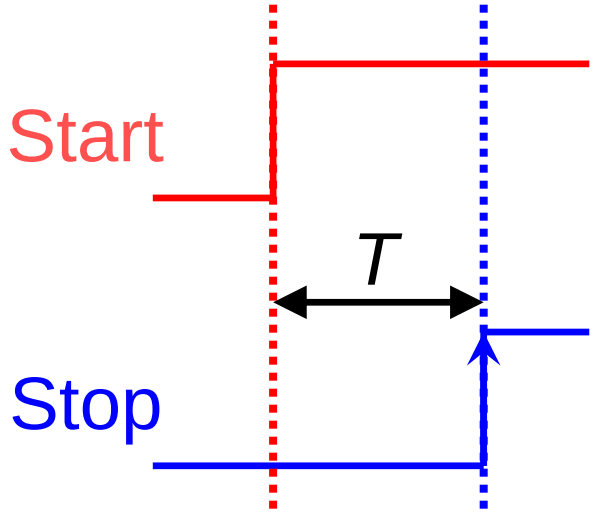
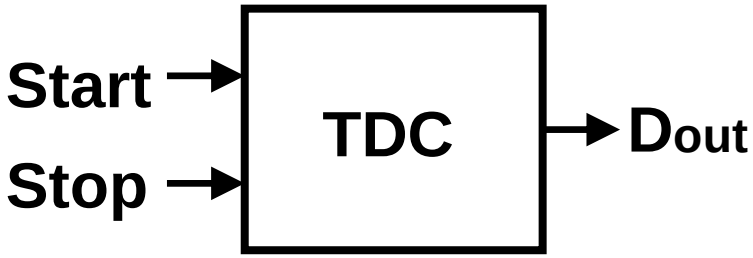
Time to Digital Converter（TDC）

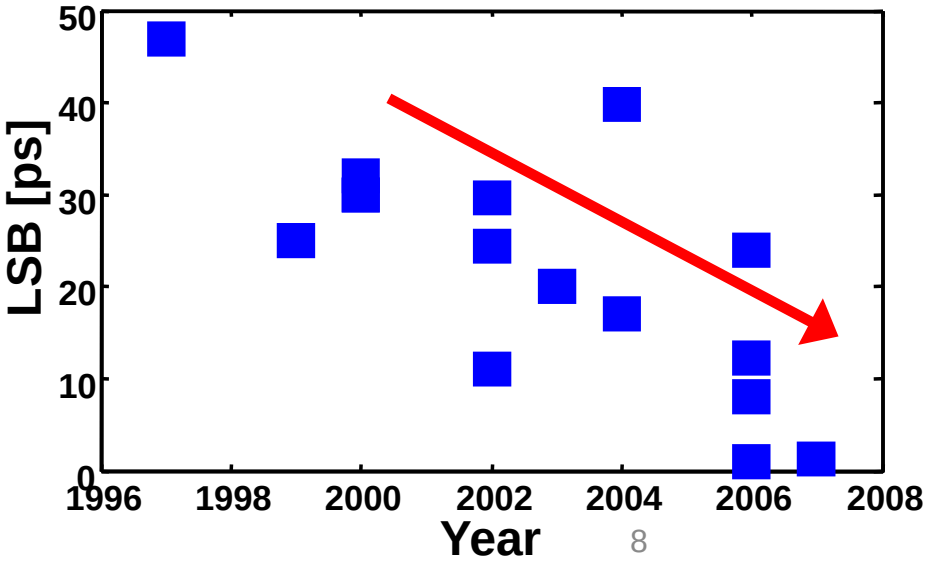
- Time interval → Measurement → Digital value





- Key component of Time-domain analog circuit
- Higher resolution can be obtained with scaled CMOS

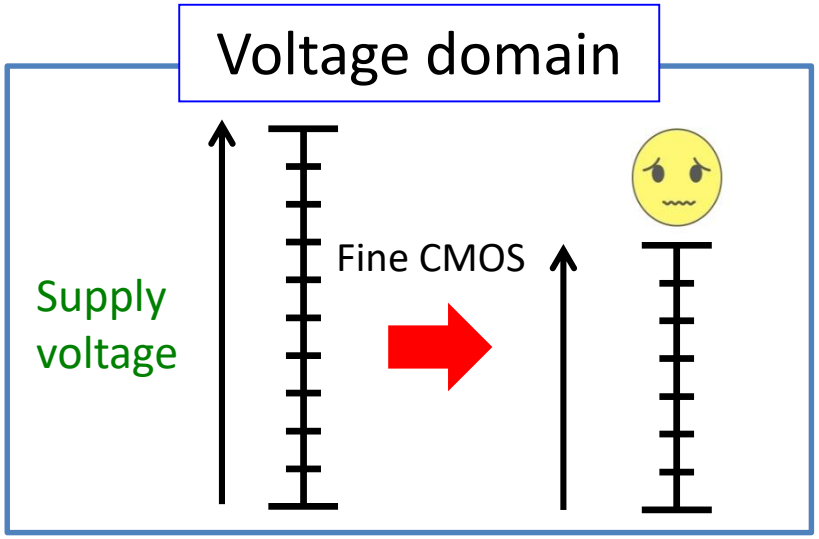
Higher resolution with CMOS scaling

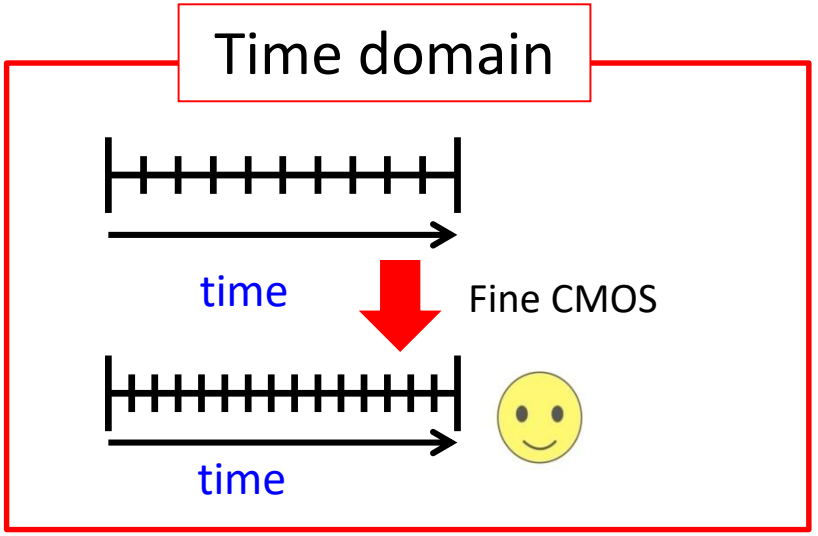


Background

Advanced CMOS VLSI

- Low power-supply voltages
- Fast switching speeds





A Time-to-Digital Converter (TDC) provides a digital output proportional to time between two clock transitions.

The TDC is a key component in time-domain analog circuits,

（e.g. I/O interface, Sensor Interfaces, All-Digital PLLs, ADCs, .. ）

Time Domain Analog Circuit Features

- Voltage domain:

  Signal range : Up to power supply voltage

  Time domain:

  Signal range : Time continues indefinitely

  ⇒ Large dynamic range

- Time domain analog circuit：

  Binary amplitude（Vss, Vdd)

  ⇒ Can consist of digital circuit

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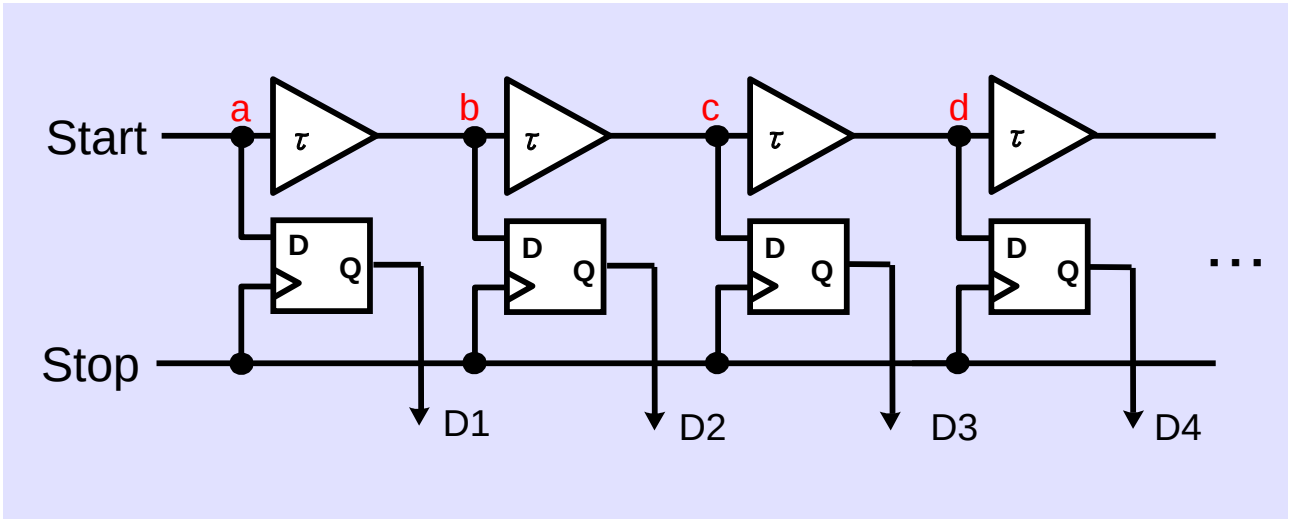
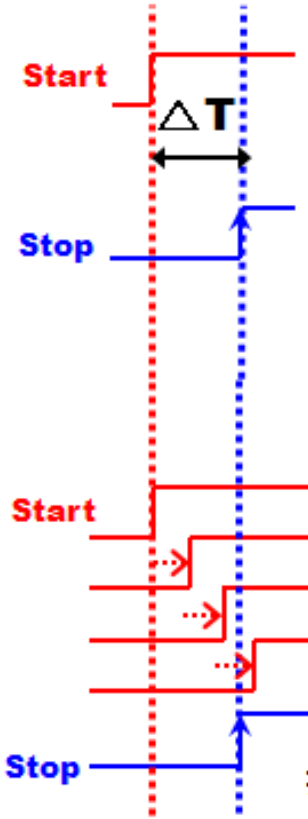
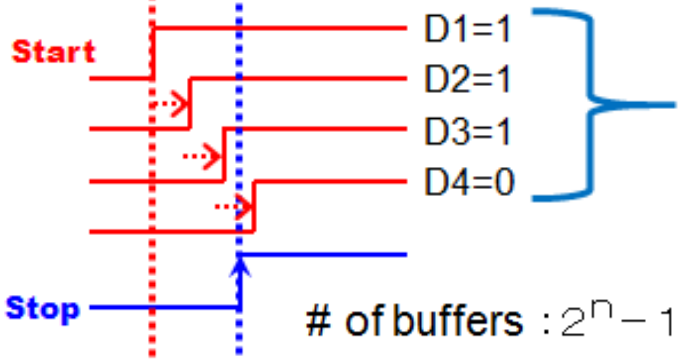
Flash-type TDC







D1=1
D2=1
D3=1
D4=0

thermal code

Digital output: 0111

Time resolution: τ

$\Delta T = 3\tau$

# of buffers : $2^n - 1$ (10bit→1023)

# of DFFs: $2^n - 1$ (10bit→1023) → Large circuit → Large power

Time resolution: buffer gate delay τ → Too coarse

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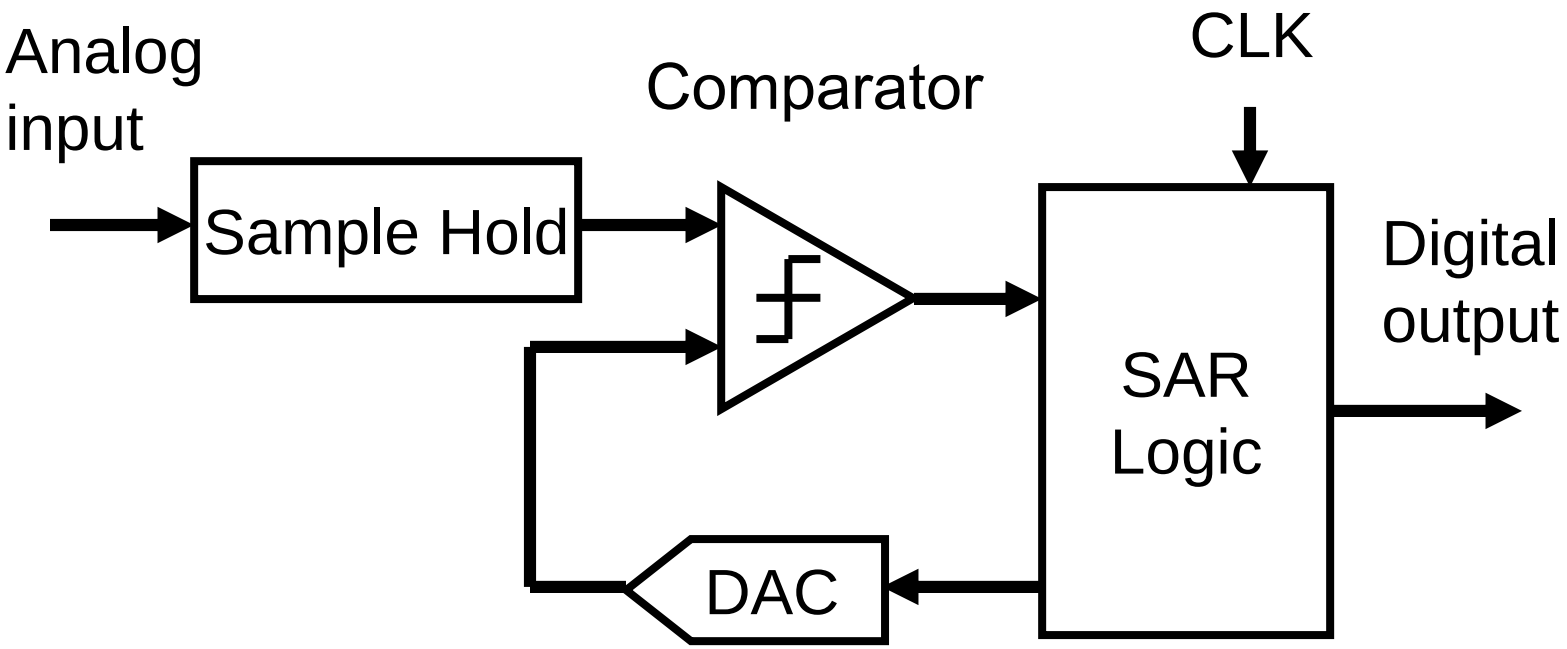
SAR ADC Block



SAR ADC is digital centric.

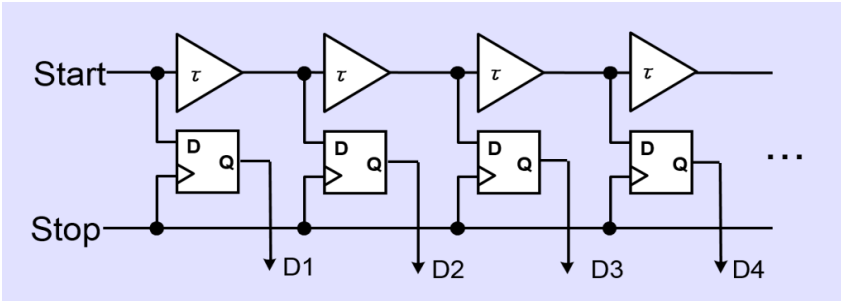
→ Suitable for fine CMOS implementation.

SAR TDC Architecture

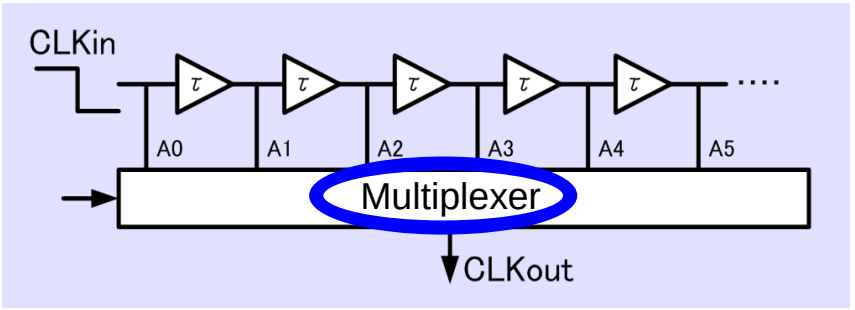
D-FF can be greatly reduced by using MUX

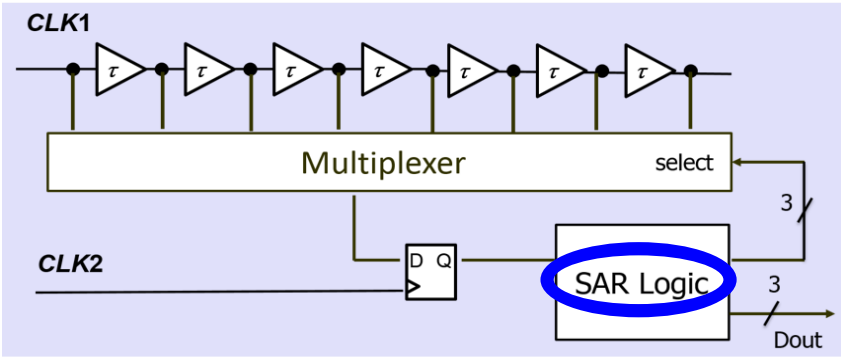
Circuit operation loop can be made with Successive Approximation

SAR : Successive Approximation Register



Flash type TDC



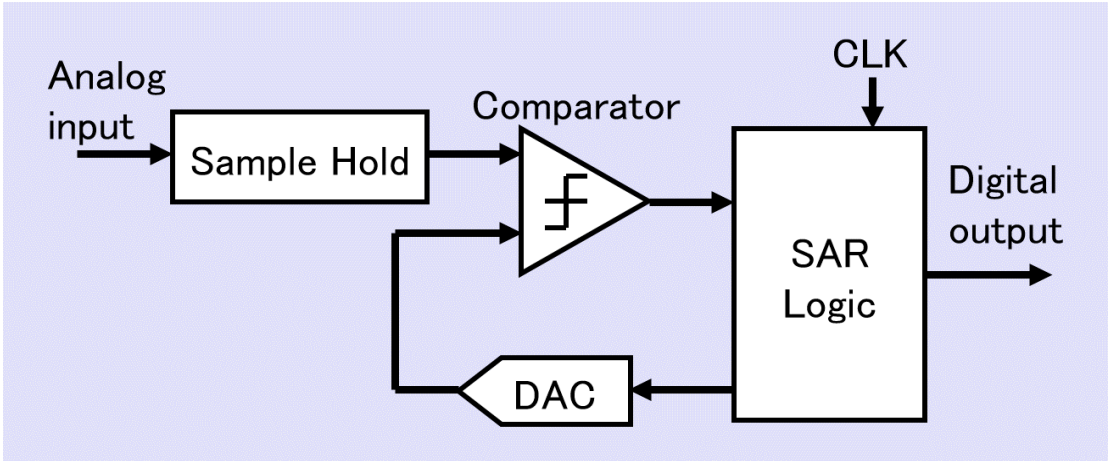


SAR TDC

SAR-ADC VS SAR-TDC

SAR ADC :

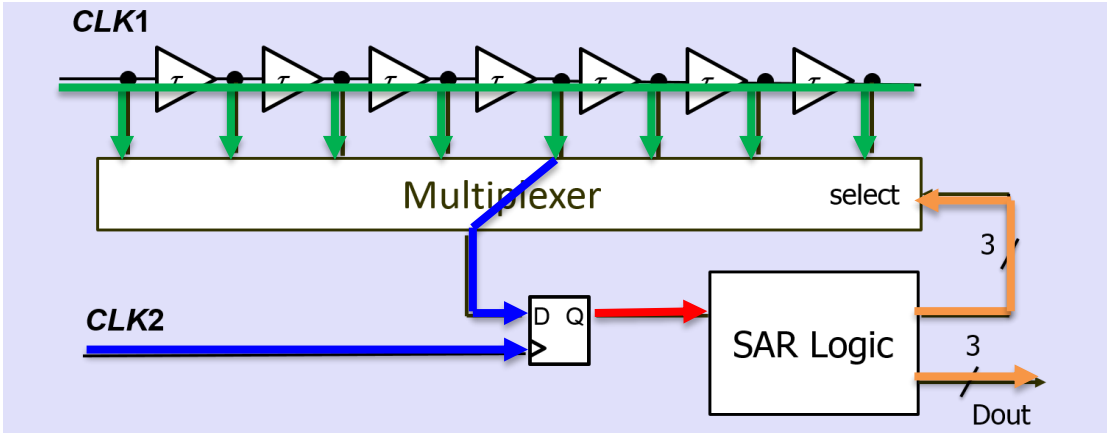
- Comparator
- DAC



SAR−ADC

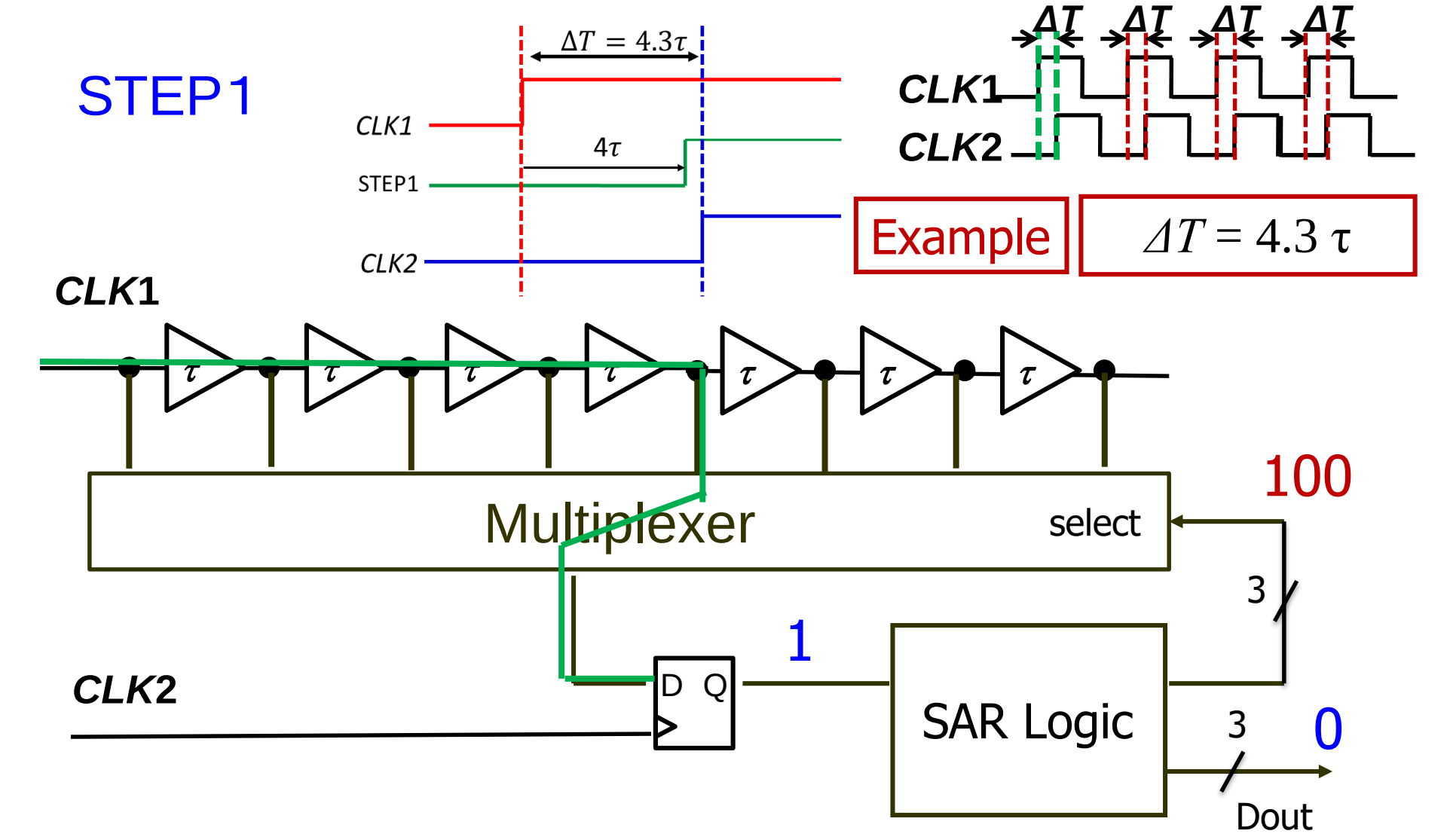
SAR TDC :

- D-FF
- Delay Line

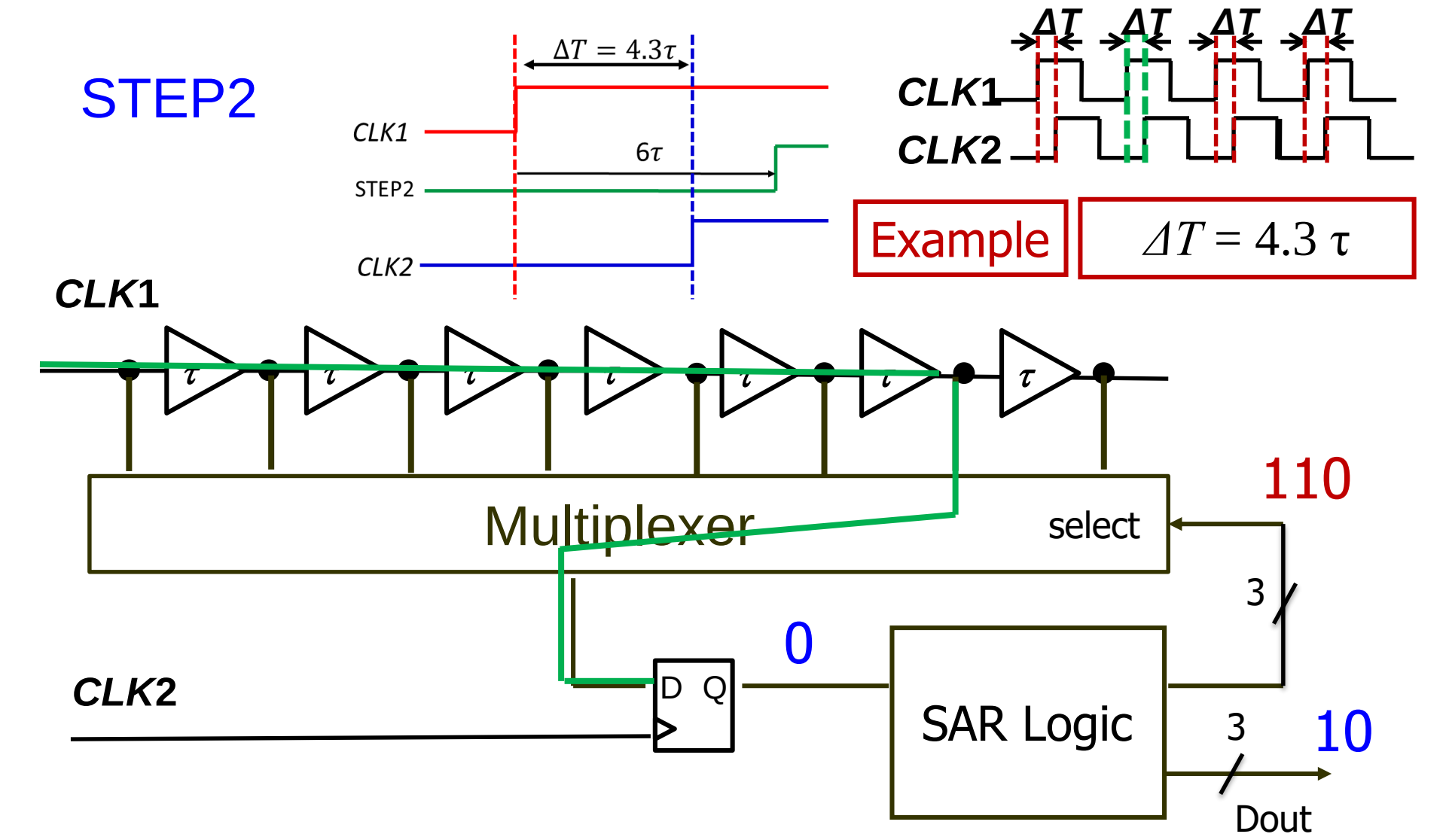


SAR-TDC

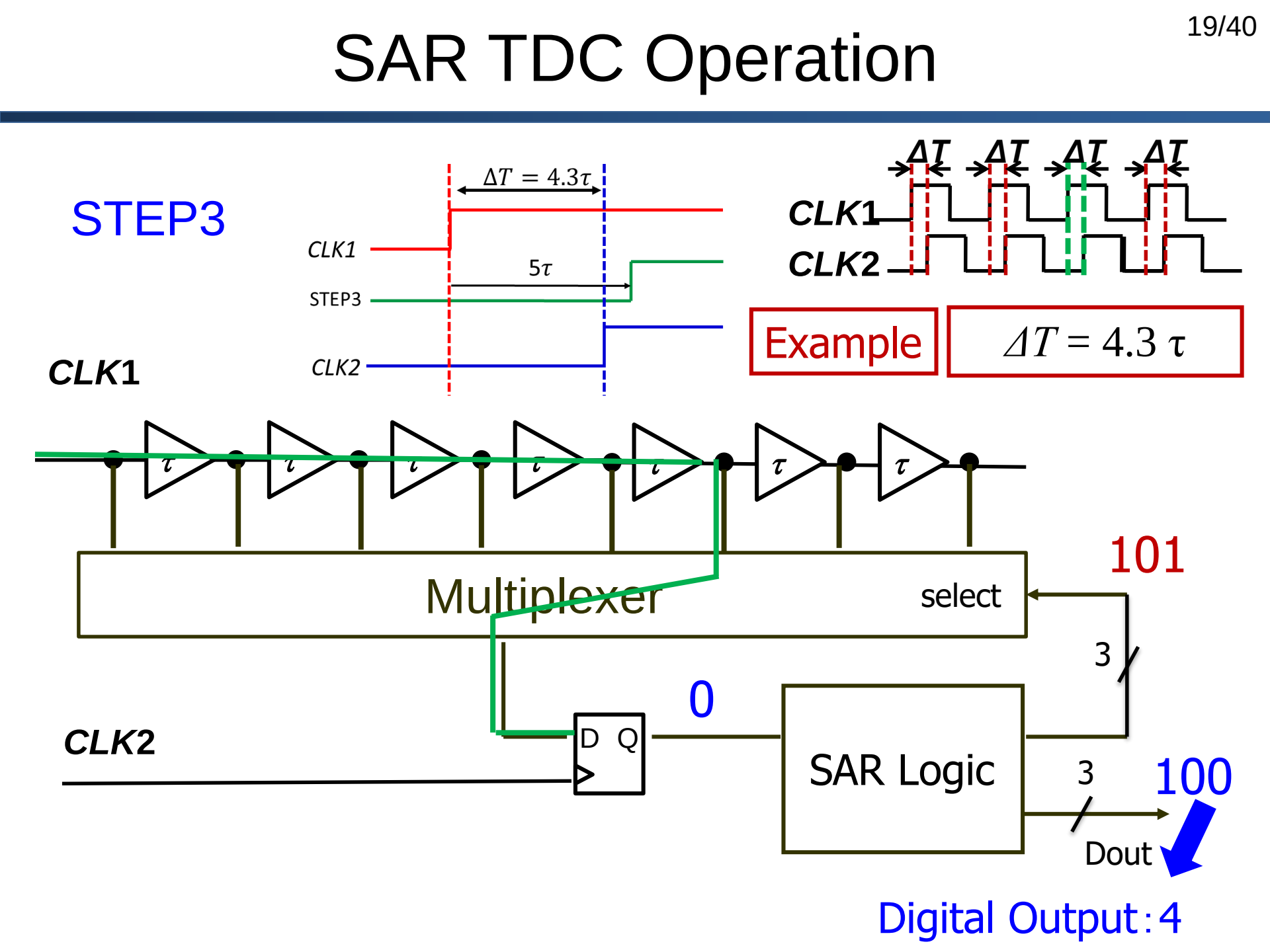
SAR TDC Operation



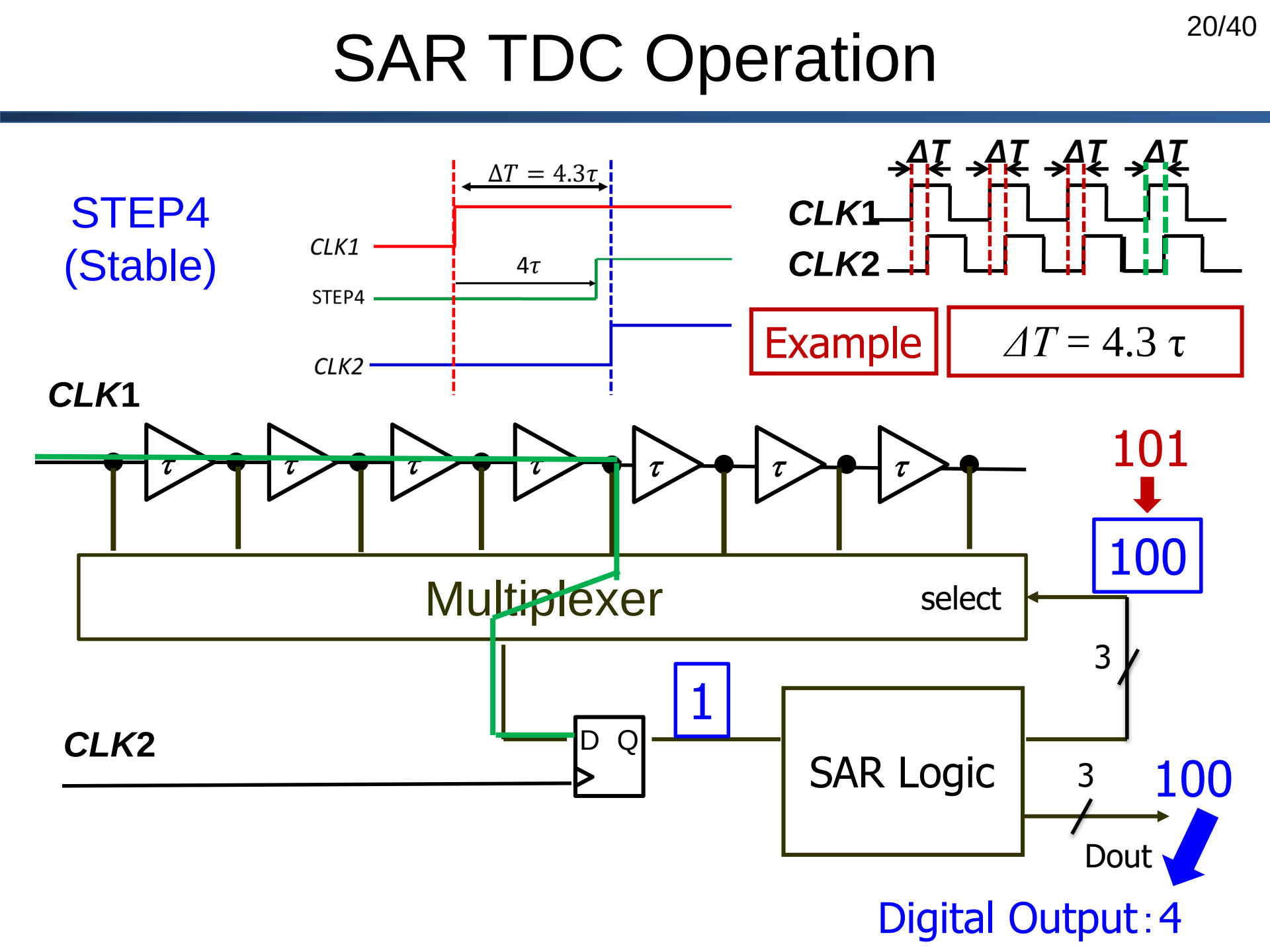
SAR TDC Operation



SAR TDC Operation



SAR TDC Operation



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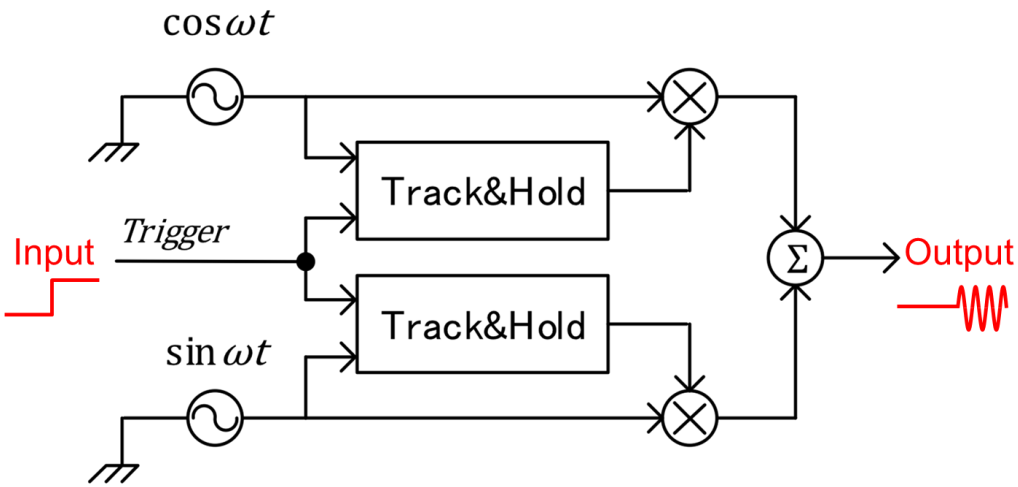
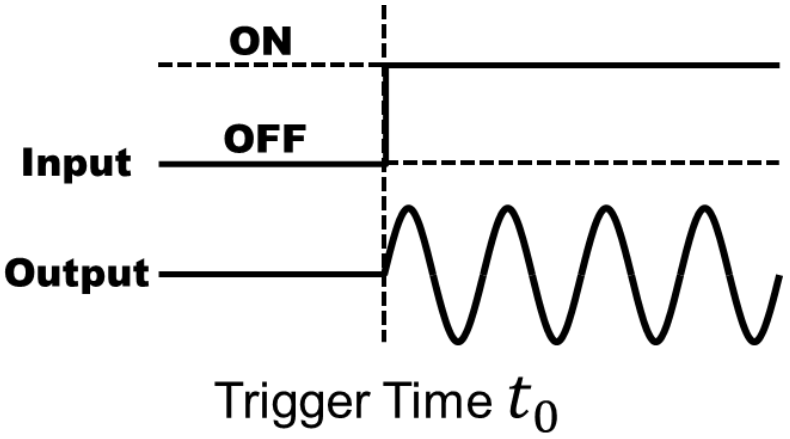
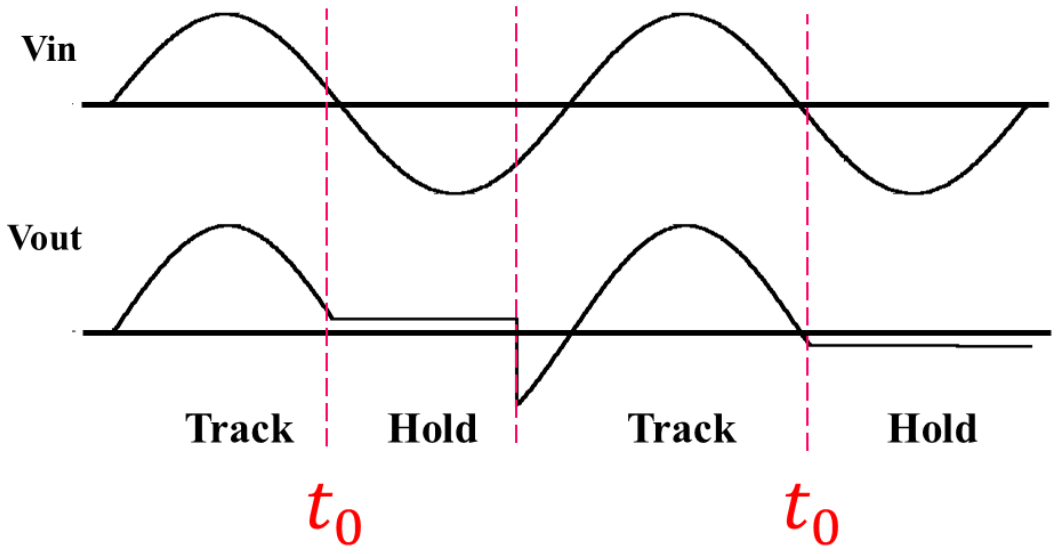
Trigger Circuit

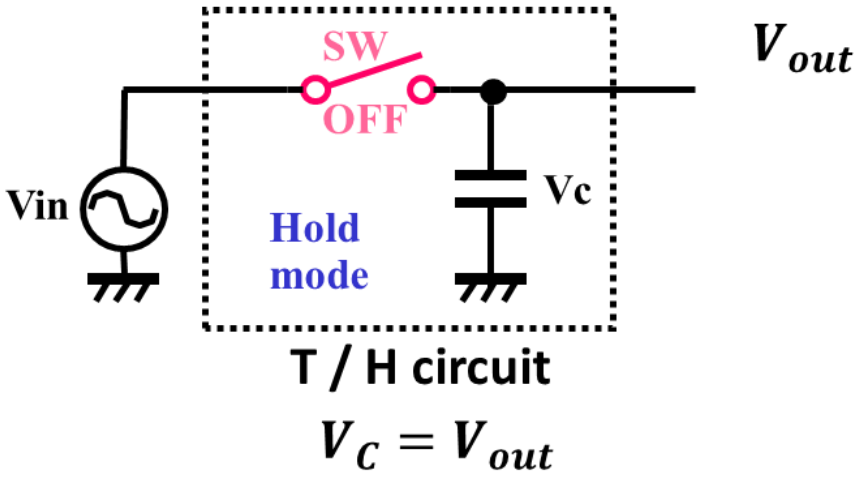


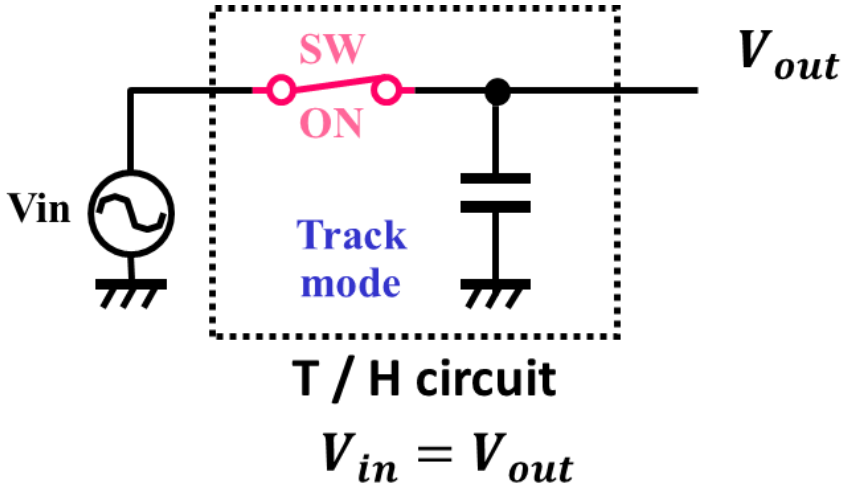


- Output starts to oscillate
  at rising timing edge of input
- Output waveform with no transient change

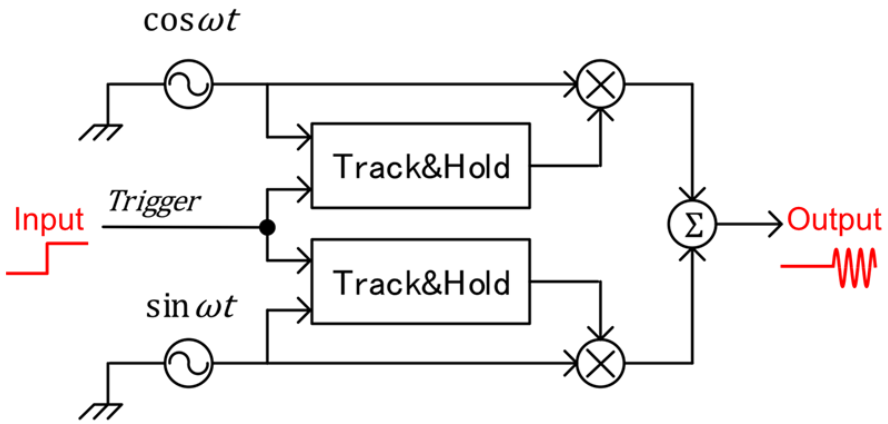
T/H Circuit

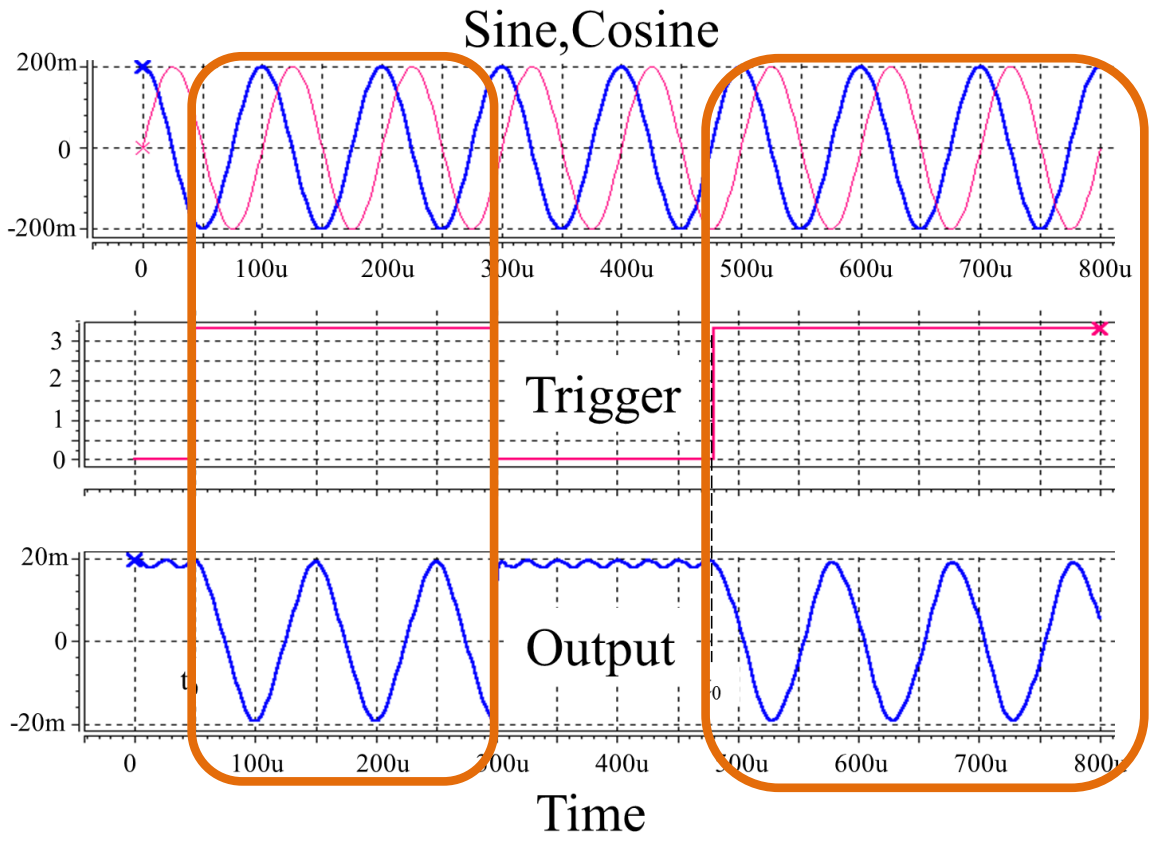

Vin
Vout
Track
Hold
Track
Hold
t_0
t_0


SW
OFF
Vin
Vc
Hold
mode
V_{out}
T / H circuit
$V_C = V_{out}$


SW
ON
Vin
Track
mode
V_{out}
T / H circuit
$V_{in} = V_{out}$

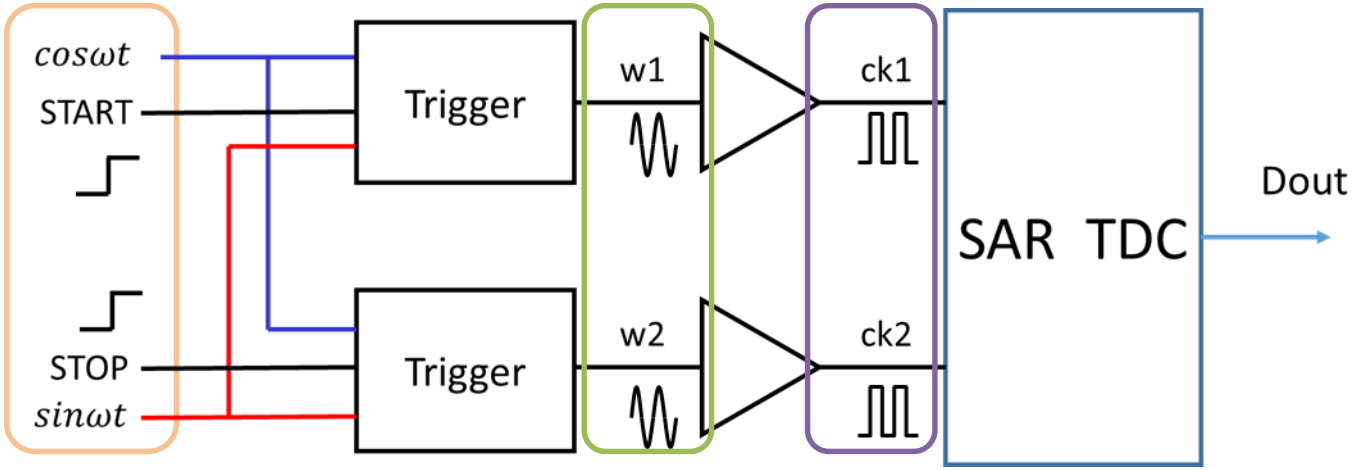
Trigger Circuit Waves

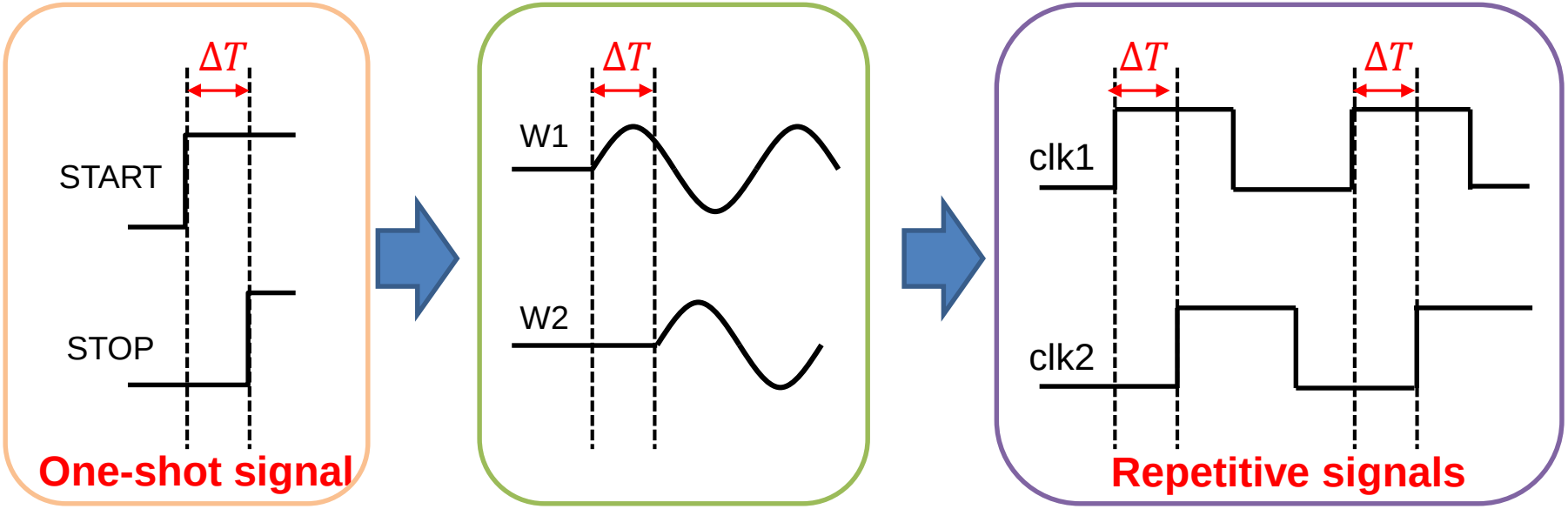




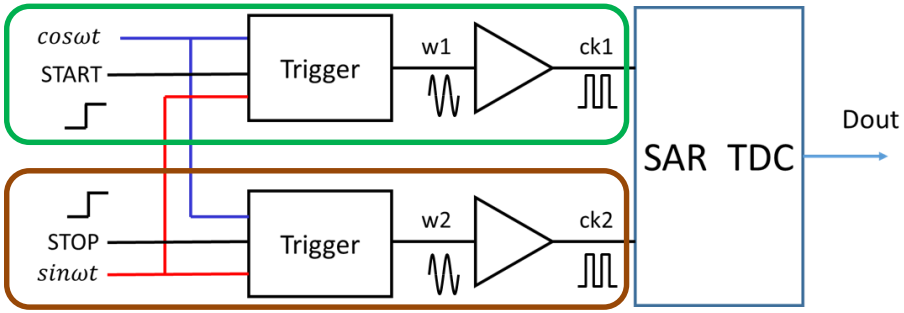
Combination of Trigger Circuit & SAR TDC

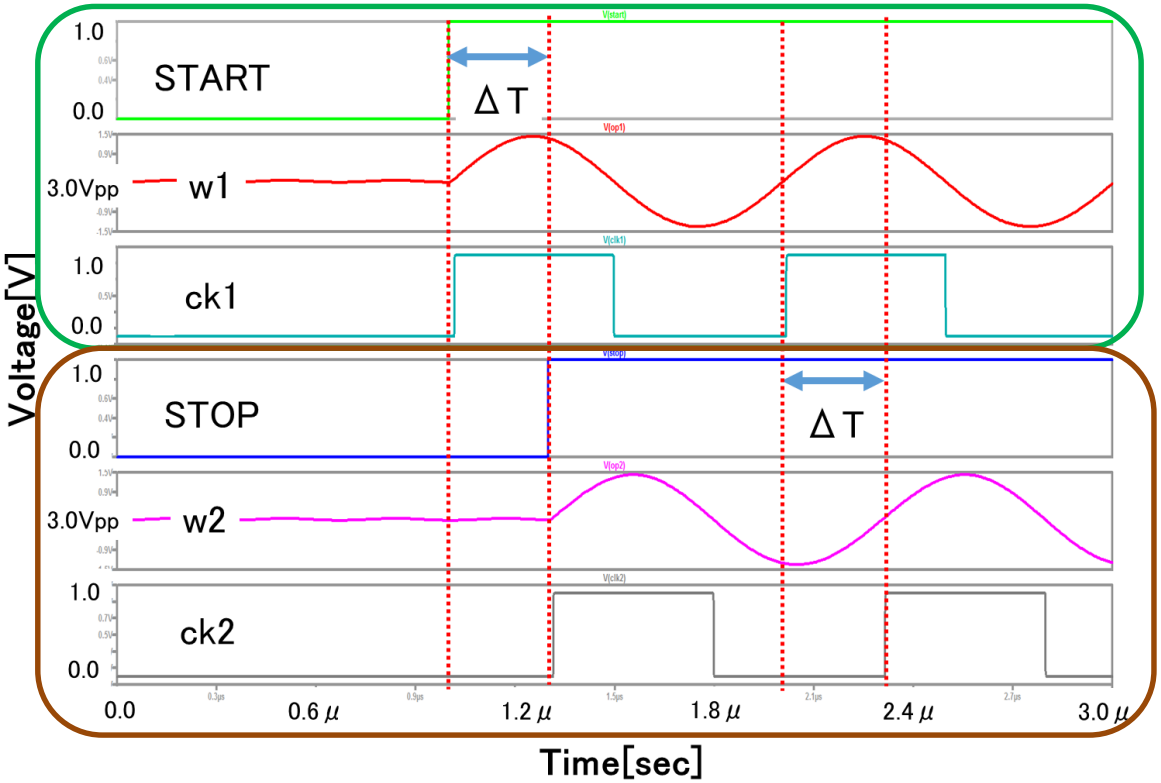
Proposed Circuit





Simulation Results





2 trigger circuits can generate **repetitive signals**

One-shot timing can be measured with SAR TDC

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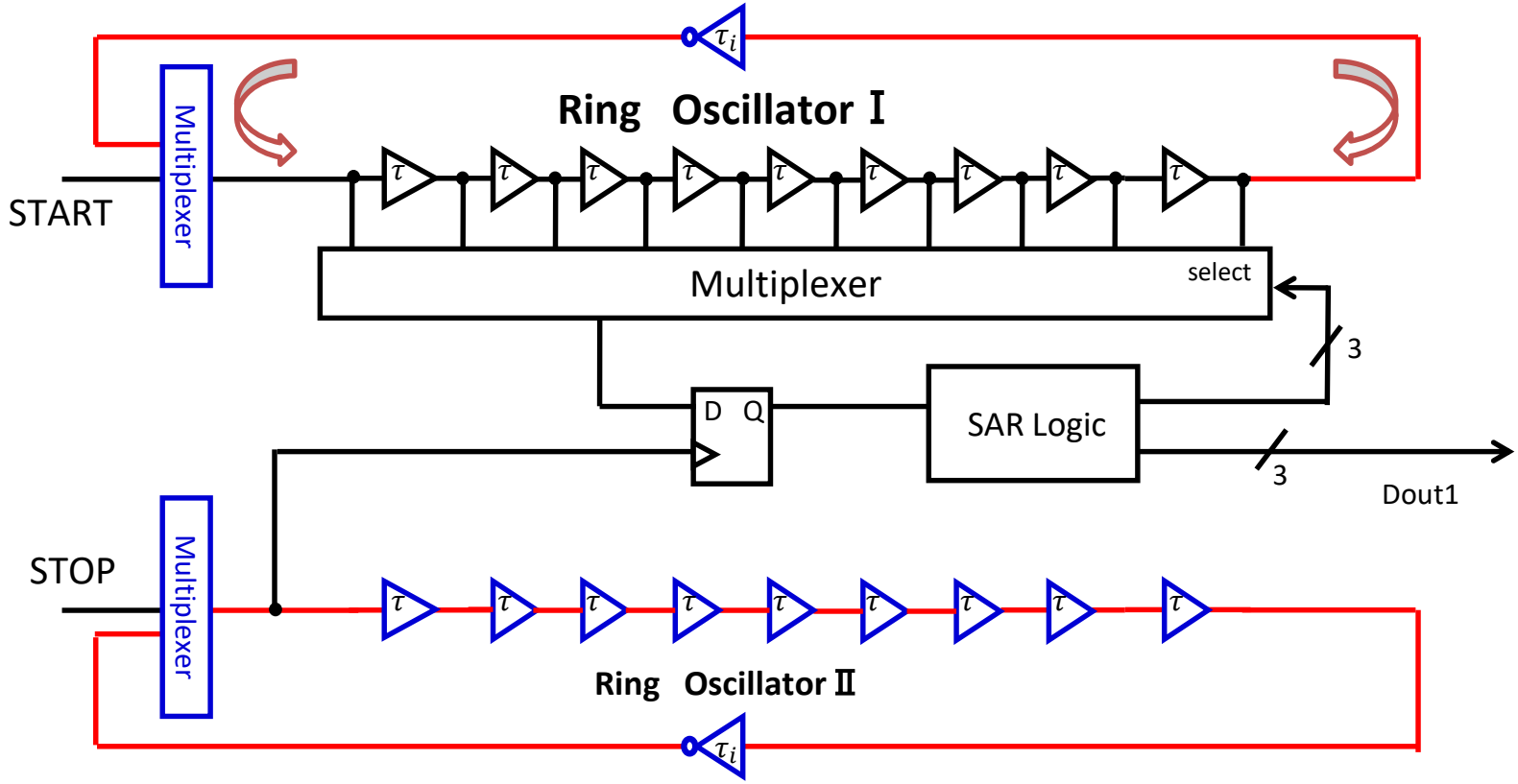
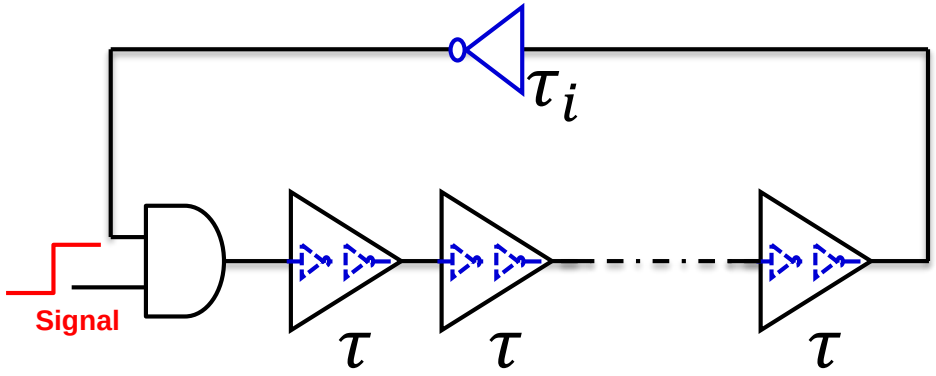
Ring Oscillator



Single-shot signal → Timing signal (Self replicating)

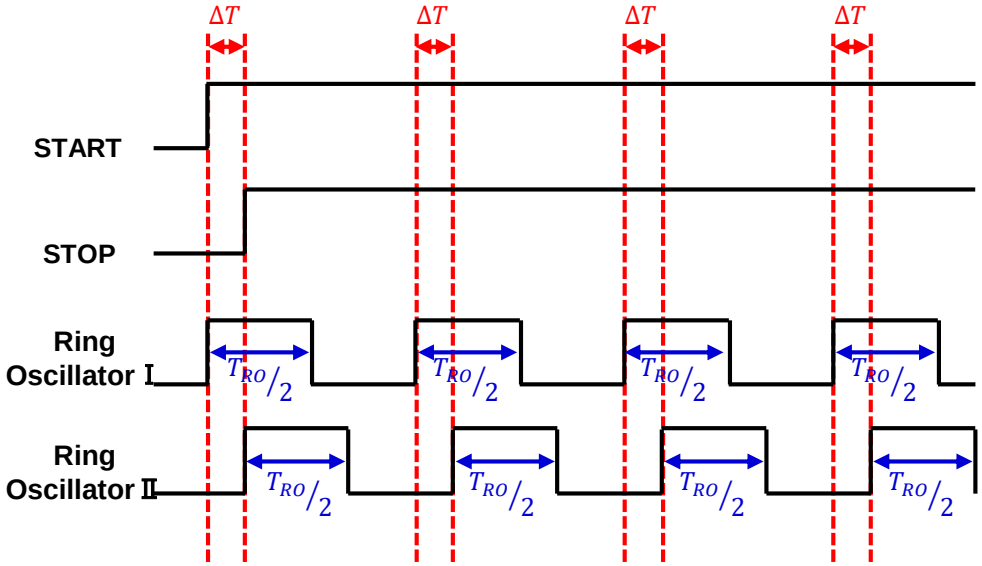
Ring Oscillator



Periodic time T_{RO}

$$T_{RO} = 2(n\tau + \tau_i)$$

$$\Delta T \leq T_{RO}/2$$



In 3-bit case

$$T_{RO}/2 = 7\tau + \tau_i$$

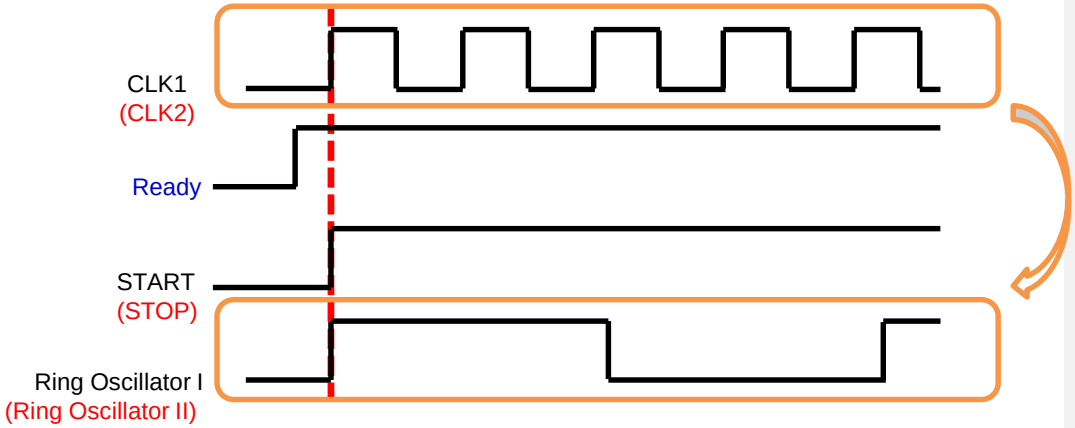
If $\tau = 1\text{ns}$ and $\tau_i = 1\text{ns}$,

$$\Delta T \leq T_{RO}/2 = 7 + 1 = 1\text{ns}$$

⇒ Resolution of 1ns

Frequency Repetitive Clock Measurement

High Frequency



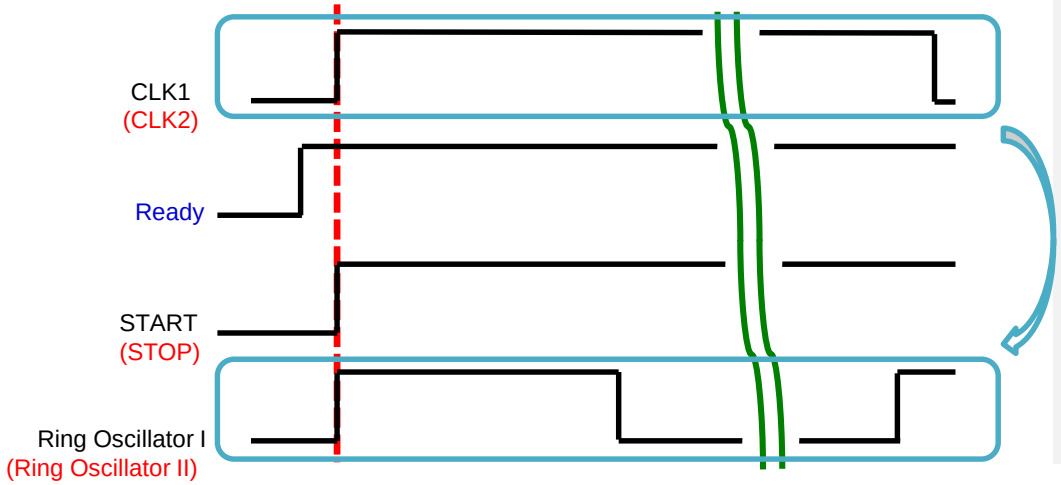
High Frequency

2GHz

Ring Oscillator

$$10ns \times 10 = 100ns$$

Low Frequency



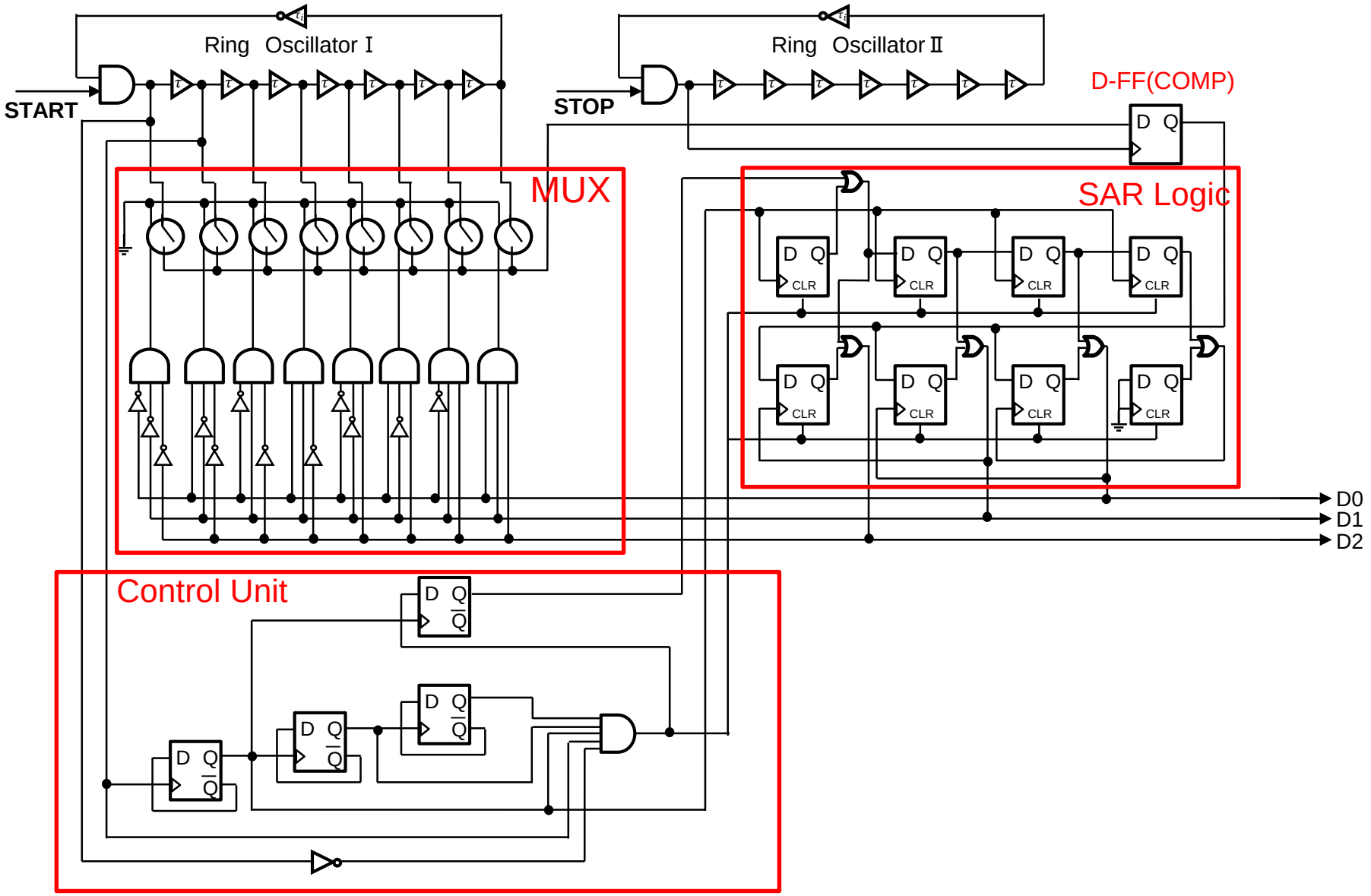
Low Frequency

0.01Hz

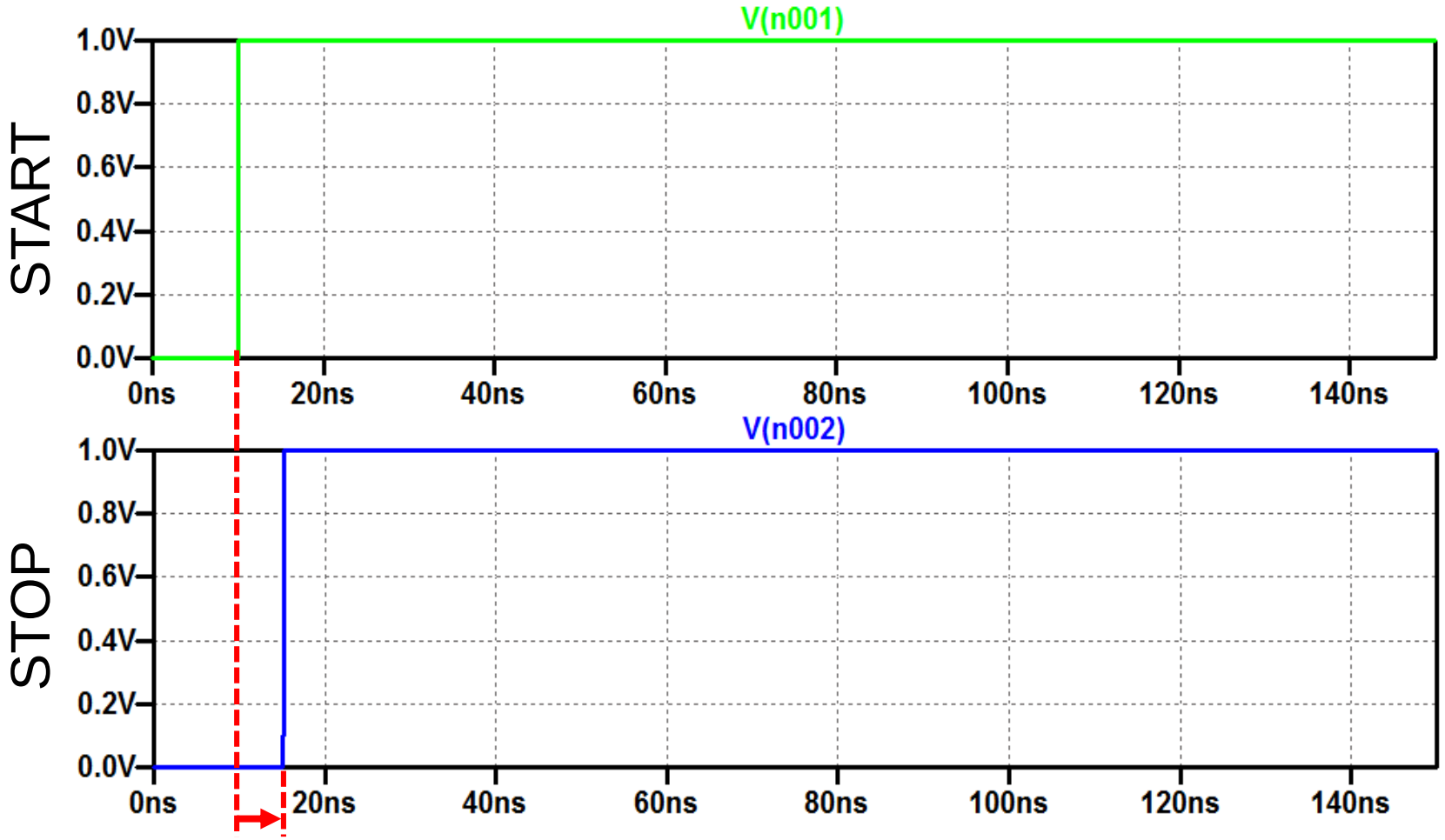
Ring Oscillator

$$10ns \times 10 = 100ns$$

Simulated Circuit

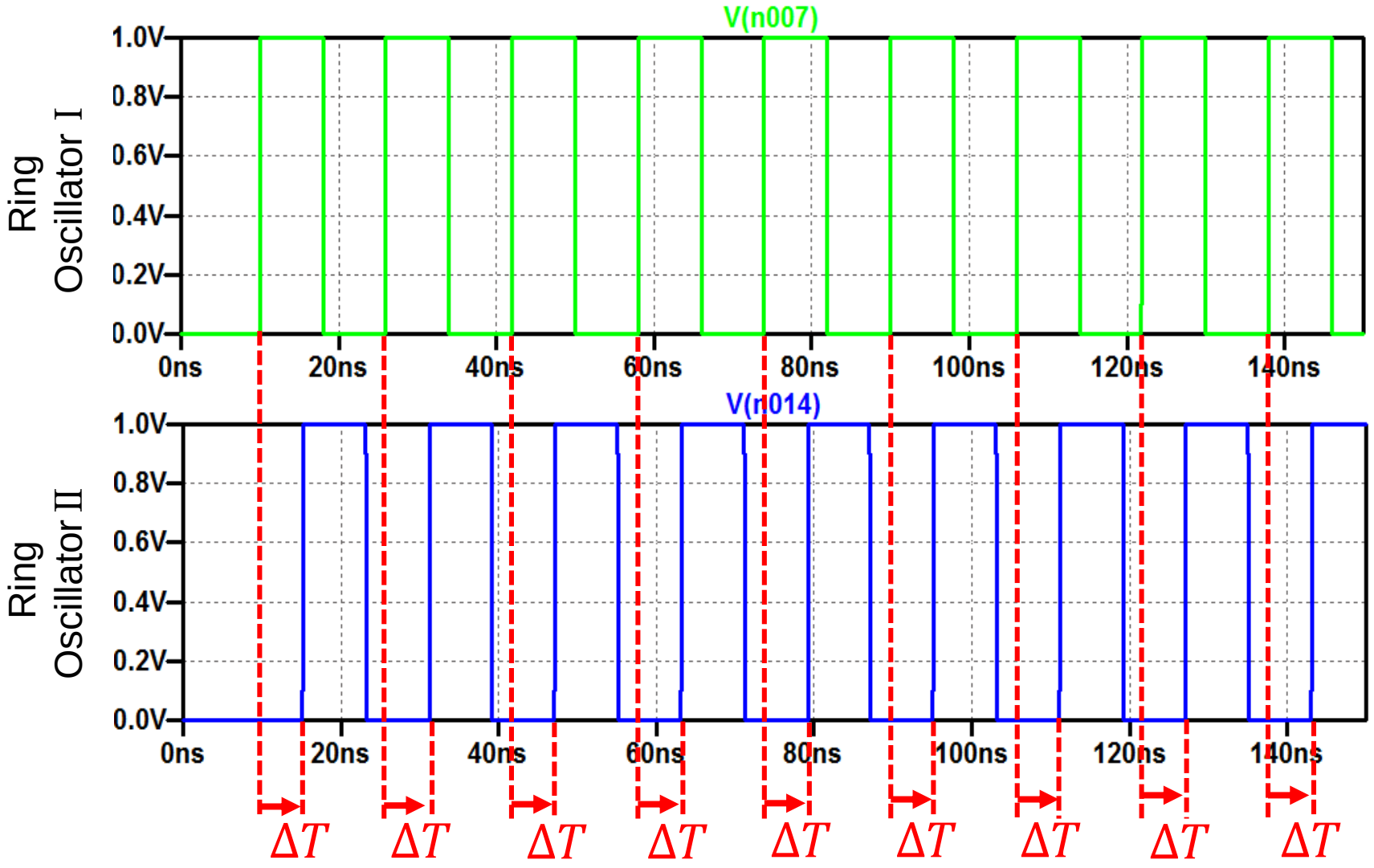


One-Shot Input Signal

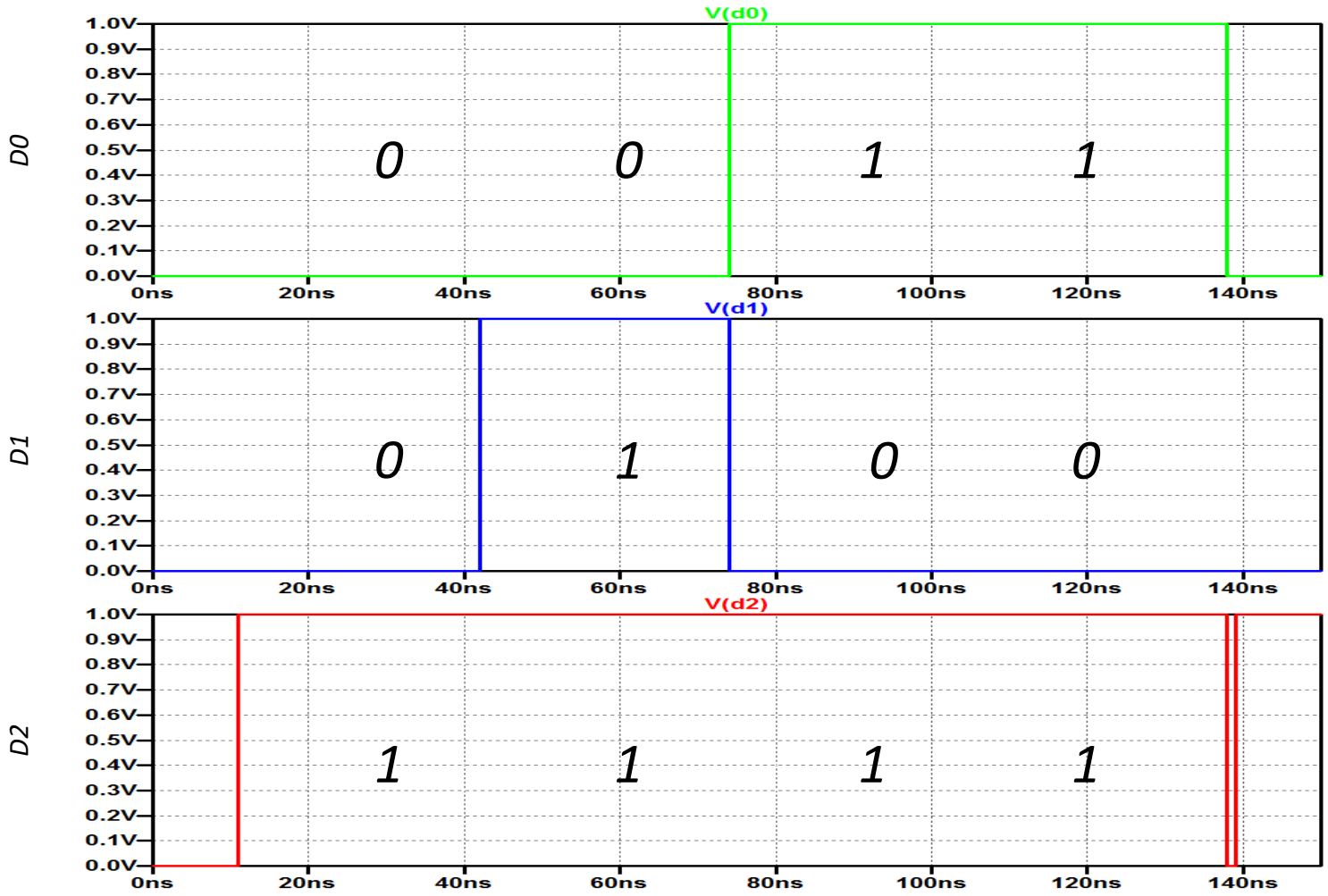


ΔT =5.2ns

Simulated Ring Oscillator Waveforms



D-FF Output Signal at Each Step



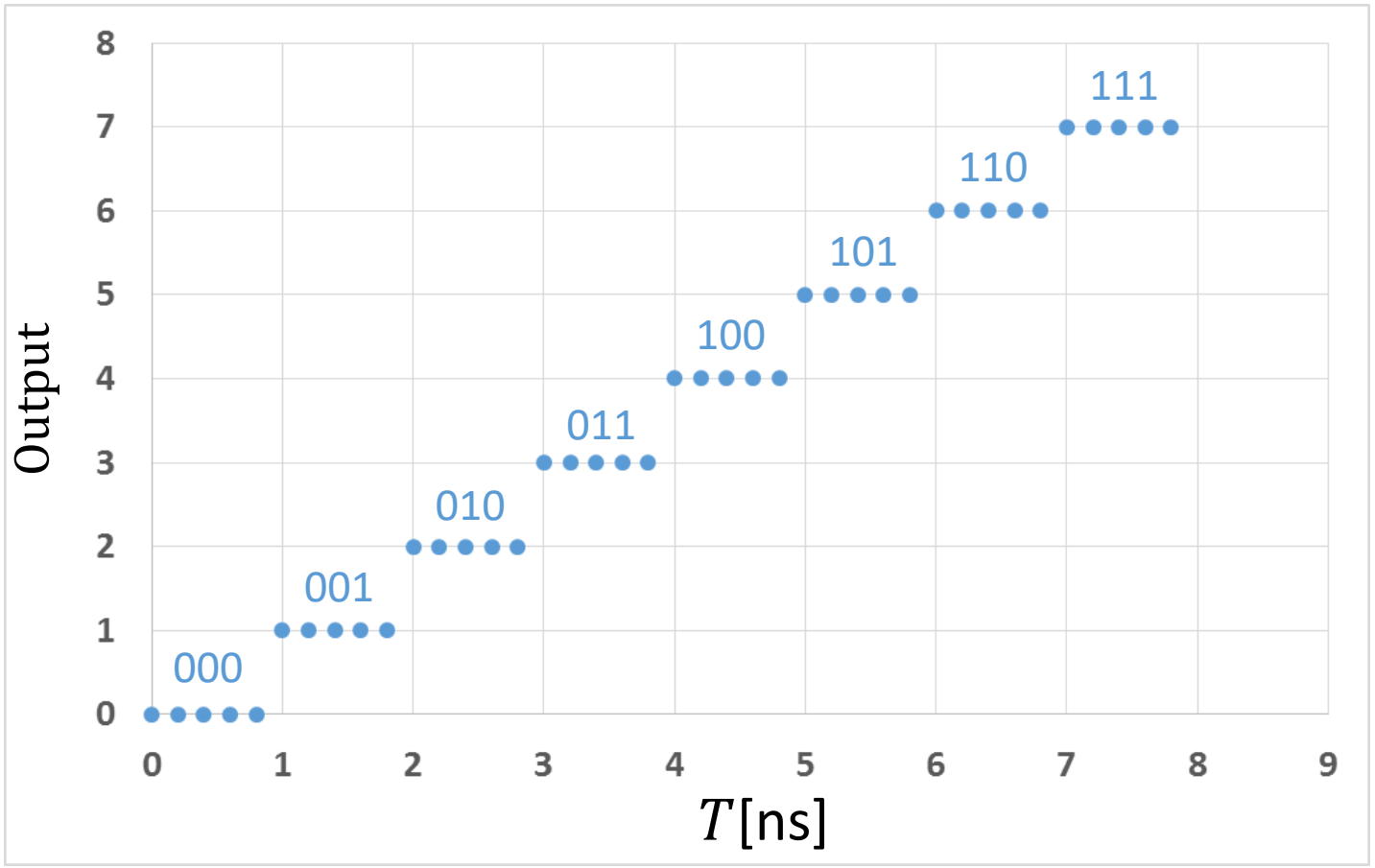
$\Delta T > 4\tau$ = 100

$\Delta T < 6\tau$ = 110

$\Delta T > 5\tau$ = 101

ΔT =5.2ns

Input Output Linearity



Proposed SAR TDC input & output have linear relationship

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Discussion (1)

SAR TDC operates with external clock

Operation speed depends on measured clock witch may be variable

Employing ring oscillators

Frequency is fixed

Reasonable as mixed-signal circuit design

Discussion (2)

Assumption

Two ring oscillators are completely matched

(oscillation frequencies are the same)

In reality they are not

Future work

Mismatch compensation or self-calibration method

(e.g. redundancy SAR algorithm)

Conclusion

✓Trigger circuit can generate repetitive signals

✓ Ring oscillator helps the realization of full digital FPGA

✓ One shot timing can be measured with SAR TDC

◆ The remaining work

Taking care of mismatches between two ring oscillators

Time continues indefinitely.

Kobayashi Laboratory

Time is GOLD !!

TDC is a key.