SAR TDC Architecture for One-Shot Timing Measurement with Full Digital Implementation

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Objective

Development of highly-linear, fine time-resolution TDC for high-speed digital I/O interface timing measurement
Innovation

✓ **Trigger Circuit**
  
  One-shot timing measurement &

  Good for low frequency repetitive timing

✓ **Ring Oscillator**
  
  One-shot timing measurement &

  Good for high & low frequency repetitive timing
Approach

SAR TDC

SAR TDC + Trigger Circuit

- 😊 Measure one-shot timing
- 😞 Include analog circuit

SAR TDC + Ring Oscillator

- 😊 Measure one-shot timing
- 😊 Without analog circuit

Full digital FPGA implementation
Problems in Operation of SAR

During measurement

The necessity to always input certain time difference

Input signal → SAR TDC → Output signal

Circuit approach to problem

Digital ↔ Analog

Multiple steps required
Outline

- Research Objective
- Conventional TDC Architecture
  - Flash TDC
- SAR TDC Architecture & Operation
- Proposed SAR TDC – Analog Centric
- Proposed SAR TDC – Digital Centric
  - Architecture & Operation
  - High Frequency
  - Low Frequency
  - Simulation
- Conclusion
Outline

● Research Objective
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● Conclusion
Time to Digital Converter (TDC)

- Time interval $\rightarrow$ Measurement $\rightarrow$ Digital value

- Key component of Time-domain analog circuit
- Higher resolution can be obtained with scaled CMOS

Higher resolution with CMOS scaling
A Time-to-Digital Converter (TDC) provides a digital output proportional to time between two clock transitions.

The TDC is a key component in time-domain analog circuits, (e.g. I/O interface, Sensor Interfaces, All-Digital PLLs, ADCs, .. )
Time Domain Analog Circuit Features

- **Voltage domain:**
  - Signal range: Up to power supply voltage

- **Time domain:**
  - Signal range: Time continues indefinitely
    - Large dynamic range

- **Time domain analog circuit:**
  - Binary amplitude \((V_{ss}, V_{dd})\)
    - Can consist of digital circuit
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Flash-type TDC

Start

\[ \tau \]

\[ \triangle T \]

Stop

Digital output: 0111

Time resolution: \( \tau \)

\[ \triangle T = 3 \tau \]

# of buffers: \( 2^{n-1} \) (10bit → 1023)

# of DFFs: \( 2^{n-1} \) (10bit → 1023)

Time resolution: buffer gate delay \( \tau \) → Too coarse

Large circuit → Large power
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SAR ADC is digital centric.

→ Suitable for fine CMOS implementation.
D-FF can be greatly reduced by using MUX

Circuit operation loop can be made with Successive Approximation

SAR : Successive Approximation Register
SAR-ADC VS SAR-TDC

SAR ADC:
- Comparator
- DAC

SAR TDC:
- D-FF
- Delay Line
STEP 1

Example

\[ \Delta T = 4.3 \tau \]
SAR TDC Operation

STEP2

CLK1

CLK2

Multiplexer

Example

$\Delta T = 4.3 \tau$

SAR Logic

Dout

$\tau$

$\tau$

$\Delta T$

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SAR TDC Operation

STEP3

CLK1

CLK2

ΔT = 4.3τ

Example

ΔT = 4.3τ

Digital Output: 4
SAR TDC Operation

STEP4 (Stable)

$\Delta T = 4.3 \tau$

Example $\Delta T = 4.3 \tau$

CLK1

CLK2

Multiplexer

SAR Logic

Digital Output: 4
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Output starts to oscillate at rising timing edge of input

Output waveform with no transient change
T/H Circuit

Vin

Vout

Track

Hold

Track

Hold

$V_{in} = V_{out}$

$V_C = V_{out}$
Trigger Circuit Waves

cosωt

Trigger Circuit Waves

Track&Hold

Output

sinωt

Input

Sine, Cosine

Trigger

Output

Time
Combination of Trigger Circuit & SAR TDC

Proposed Circuit

One-shot signal

Rerpetitive signals
Simulation Results

2 trigger circuits can generate repetitive signals

One-shot timing can be measured with SAR TDC
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Ring Oscillator

Single-shot signal  →  Timing signal
Ring Oscillator

Periodic time $T_{RO}$

$$
T_{RO} = 2(n\tau + \tau_i)
$$

$$
\Delta T \leq T_{RO}/2
$$

In 3-bit case

$$
T_{RO}/2 = 7\tau + \tau_i
$$

If $\tau = 1\text{ns}$ and $\tau_i = 1\text{ns},$

$$
\Delta T \leq T_{RO}/2 = 7 + 1 = 1\text{ns}
$$

$\Rightarrow$ Resolution of $1\text{ns}$
Frequency Repetitive Clock Measurement

**High Frequency**

- CLK1 (CLK2)
- Ready
- START (STOP)

Ring Oscillator I (Ring Oscillator II)

High Frequency

2GHz

10ns × 10 = 100ns

**Low Frequency**

- CLK1 (CLK2)
- Ready
- START (STOP)

Ring Oscillator I (Ring Oscillator II)

Low Frequency

0.01Hz

10ns × 10 = 100ns
Simulated Circuit

START

STOP

D-FF(COMP)

MUX

Control Unit

D0
D1
D2
One-Shot Input Signal

\[ \Delta T = 5.2\text{ns} \]
Simulated Ring Oscillator Waveforms

Ring Oscillator I

Ring Oscillator II

V(n007)

V(n014)

ΔT ΔT ΔT ΔT ΔT ΔT ΔT ΔT ΔT ΔT

0ns 20ns 40ns 60ns 80ns 100ns 120ns 140ns

0.0V 0.2V 0.4V 0.6V 0.8V 1.0V

D-FF Output Signal at Each Step

\[ \Delta T > 4\tau = 100 \]
\[ \Delta T < 6\tau = 110 \]
\[ \Delta T > 5\tau = 101 \]

\( \Delta T = 5.2\text{ns} \)
Input Output Linearity

Proposed SAR TDC input & output have linear relationship
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SAR TDC operates with external clock

Operation speed depends on measured clock which may be variable

Employing ring oscillators

Frequency is fixed

Reasonable as mixed-signal circuit design
Assumption

Two ring oscillators are completely matched
(oscillation frequencies are the same)

In reality they are not

Future work

Mismatch compensation or self-calibration method
(e.g. redundancy SAR algorithm)
Conclusion

✓ Trigger circuit can generate repetitive signals
✓ Ring oscillator helps the realization of full digital FPGA
✓ One shot timing can be measured with SAR TDC

◆ The remaining work
  Taking care of mismatches between two ring oscillators
Time continues indefinitely.

Time is GOLD !!

TDC is a key.