

Delay-time Suppression Technique for DC/DC Buck Converter Using Voltage Mode PWM Control

M. W. D. SAHAN *

N.Tsukiji, Y.Kobori, K. Asaishi, N.Takai, H. Kobayashi

Faculty of Science and Technology

Kobayashi laboratory

Gunma University

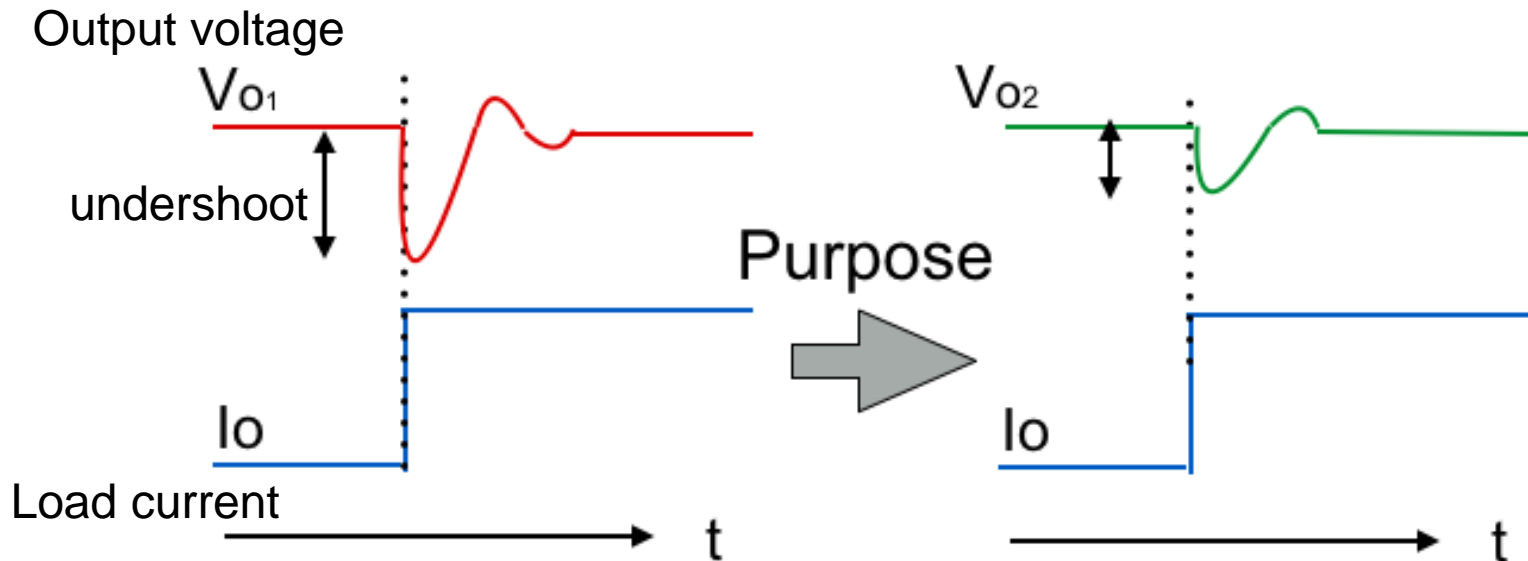


Outline

1. Purpose of This work
2. Research Background
3. Approach
4. Delay time suppression
5. Measurements results & Comparisons
6. Conclusion

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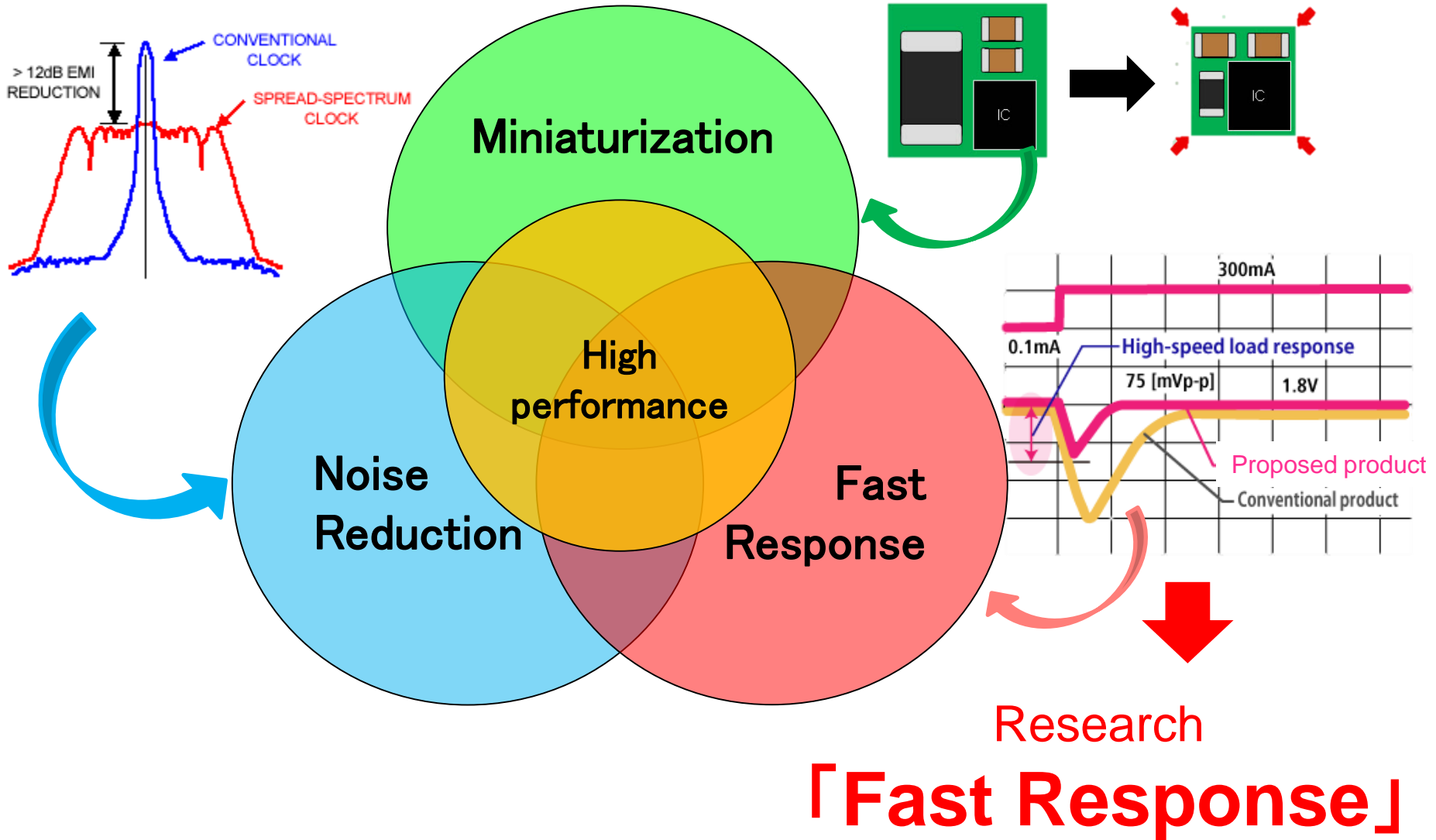
Lower output undershoot/overshoot voltage of the DC/DC buck converter



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Research background



Outline

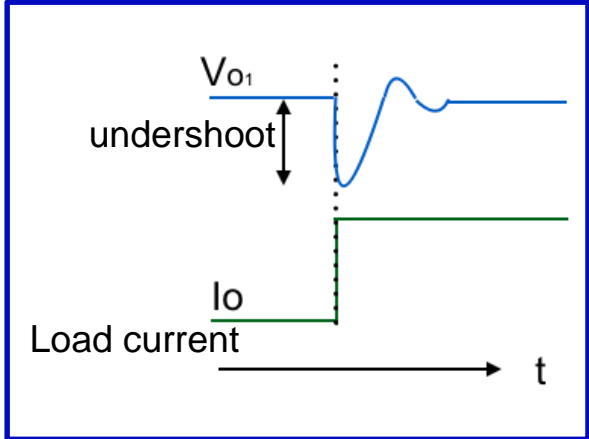
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Approach

Micro chip
DC/DC
converter

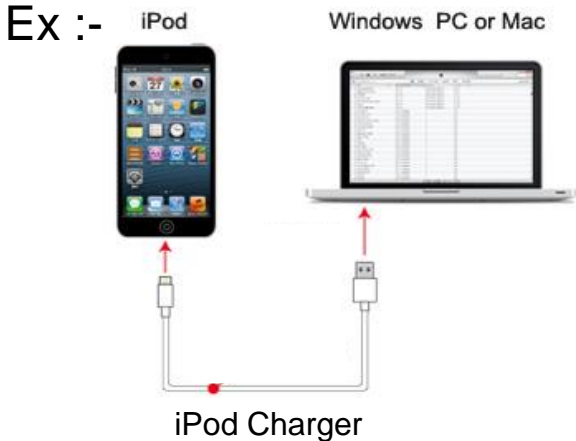
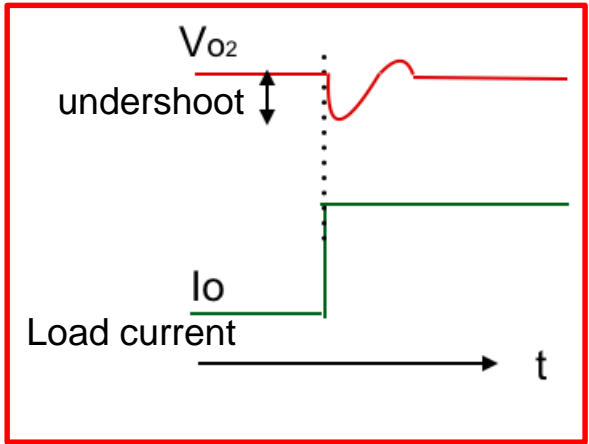


Conventional
method

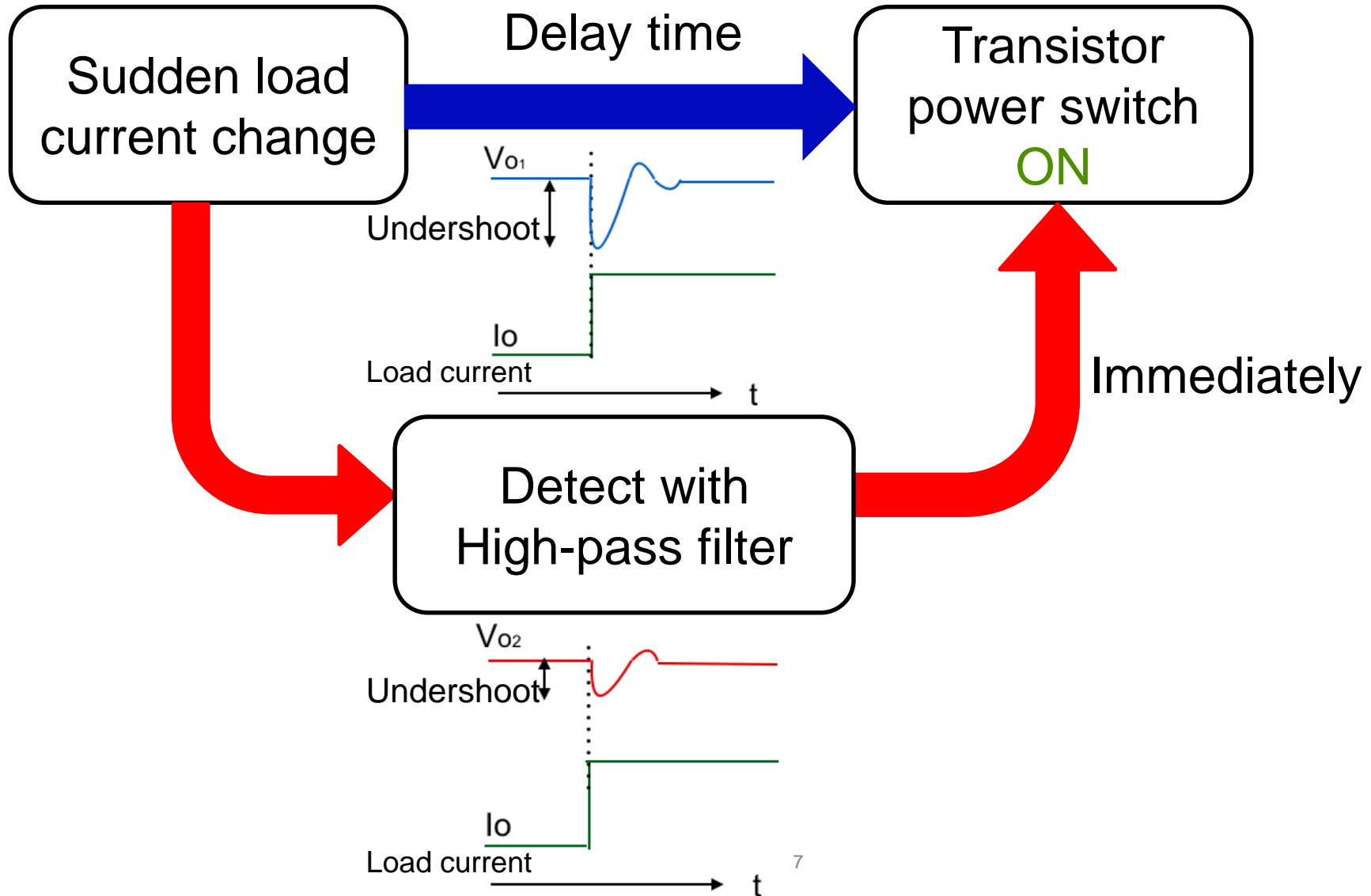


Sudden
Load current

proposed
method



Delay time Suppression

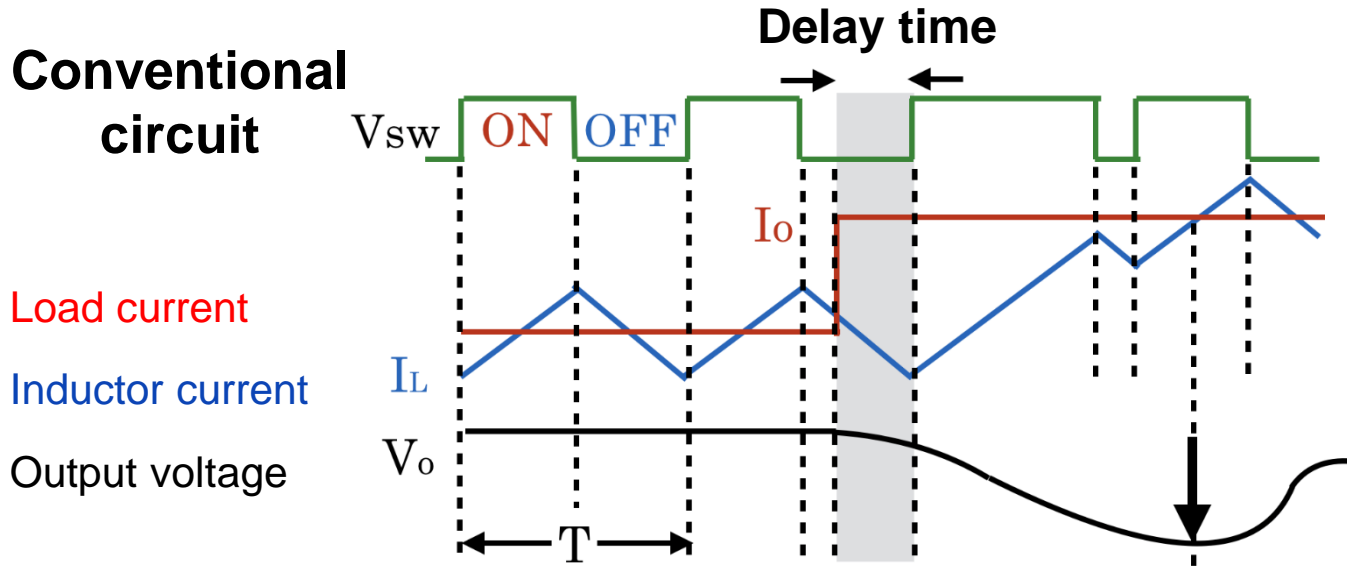


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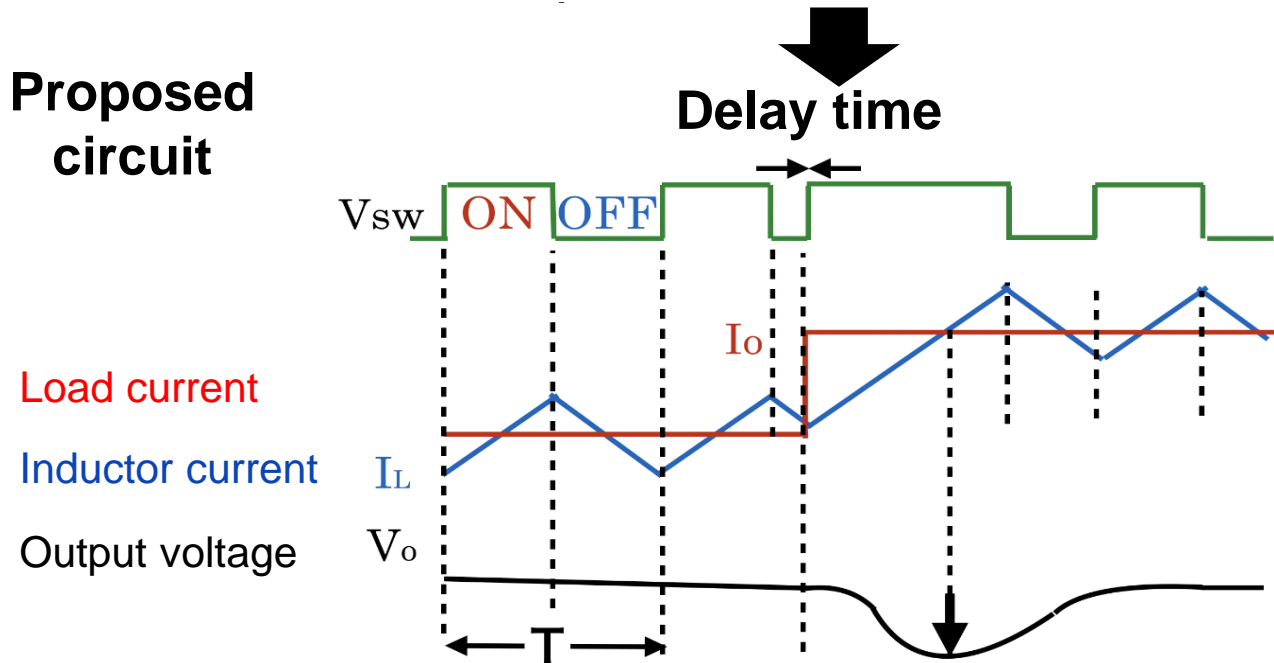
Delay time Suppression

Conventional circuit



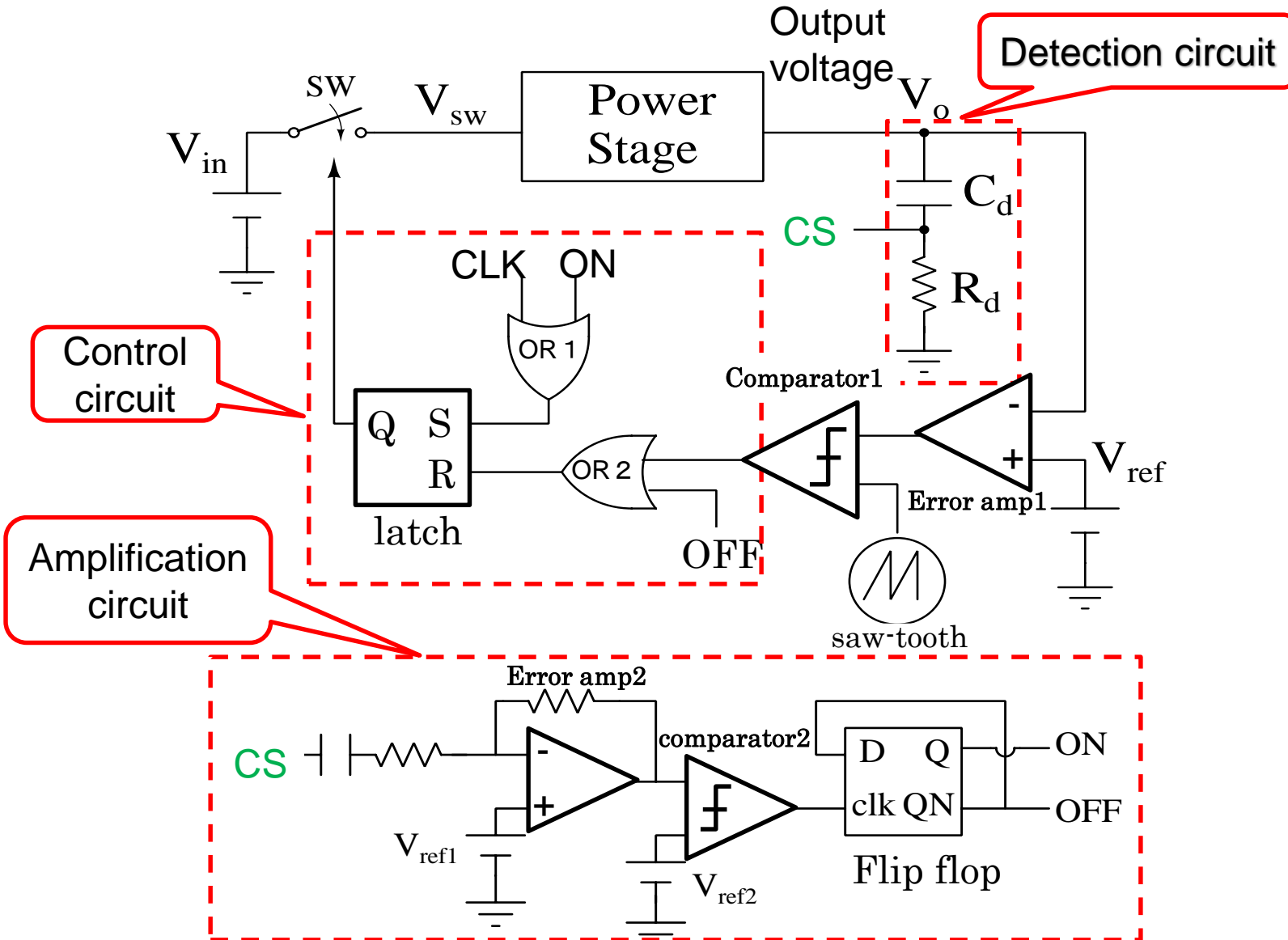
- Disadvantages**
- Large output undershoot voltage
 - Worse load current response

Proposed circuit

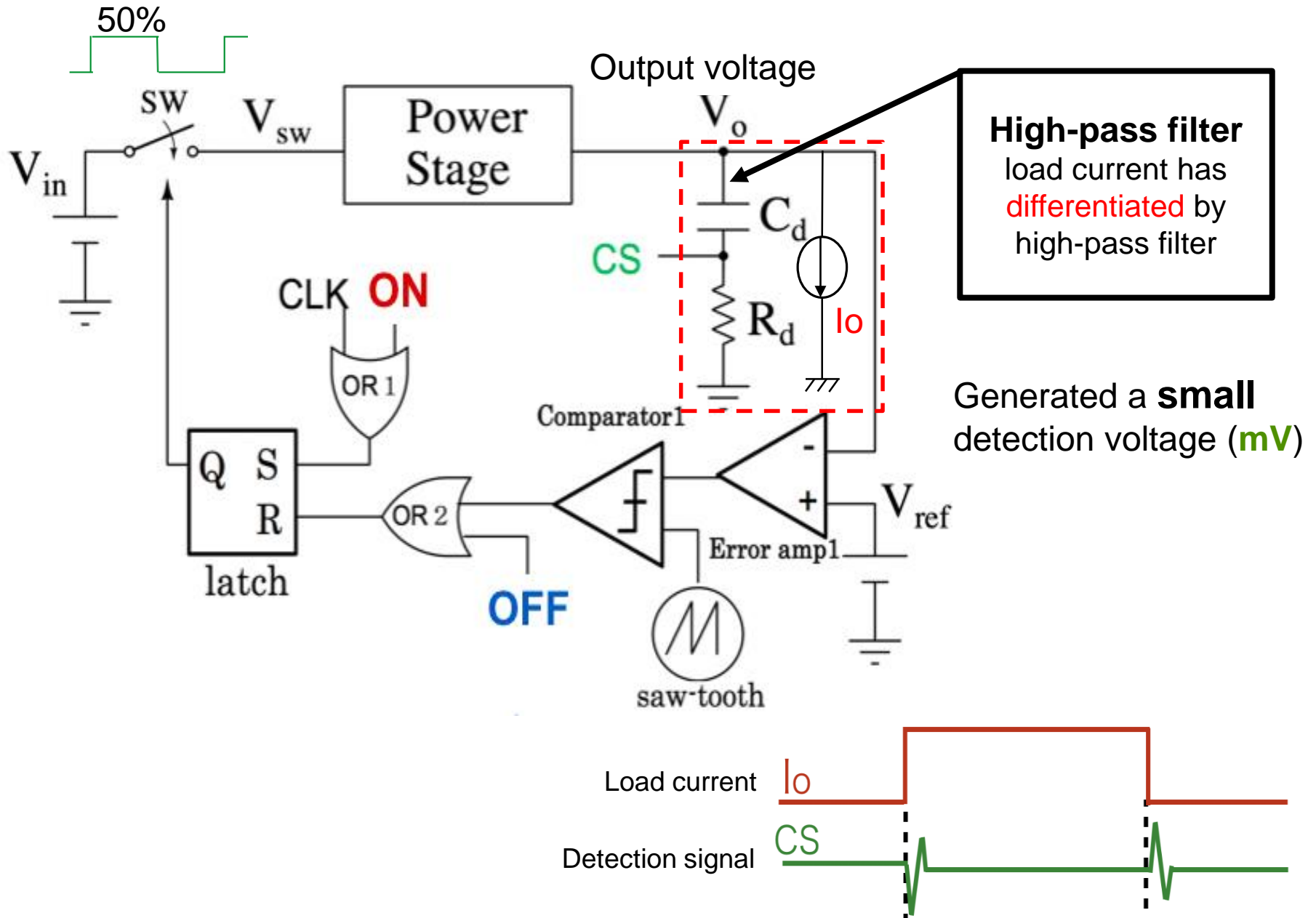


- Advantages**
- Decrease output voltage
 - Fast response sudden load current

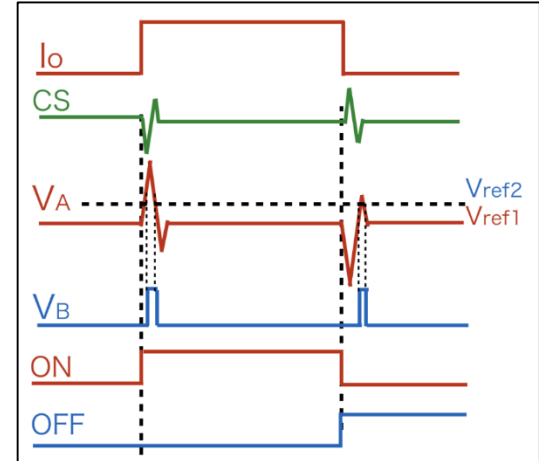
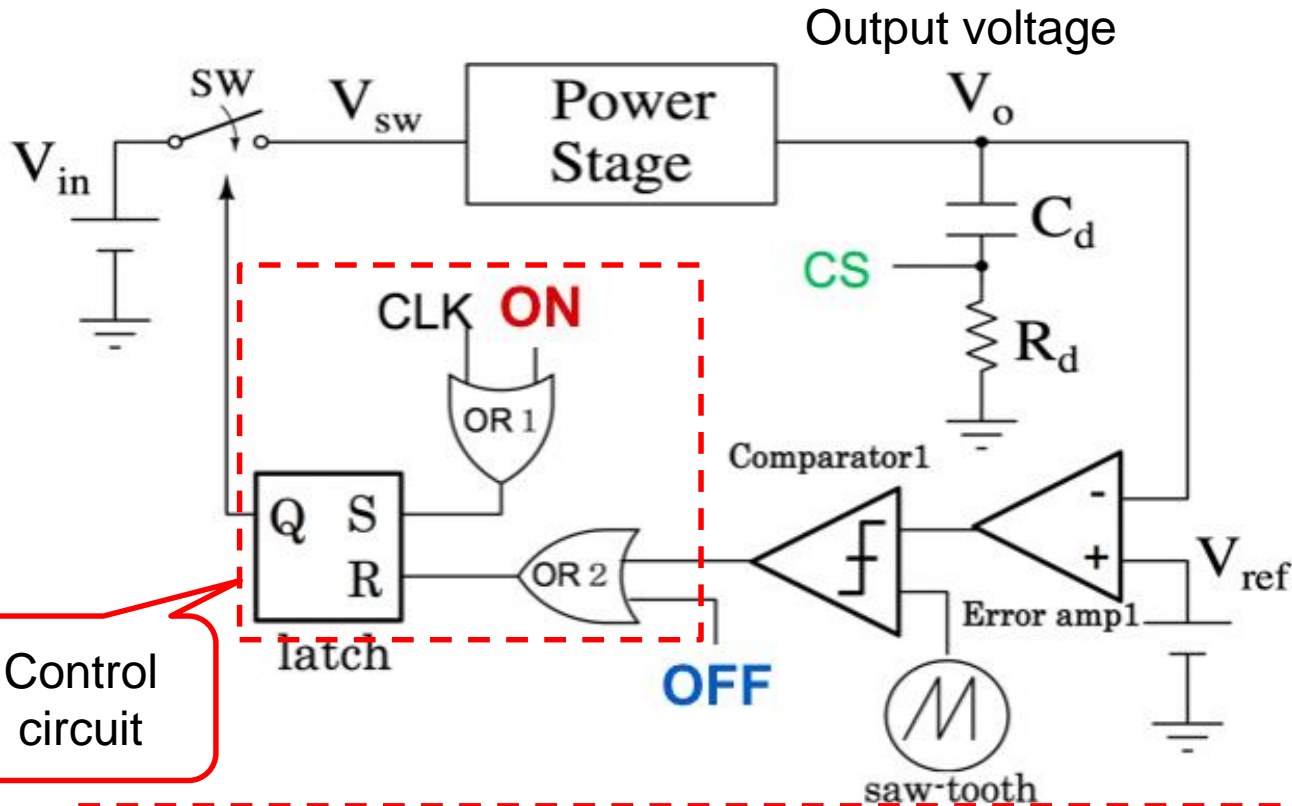
Proposed Converter Architecture



Detection circuit

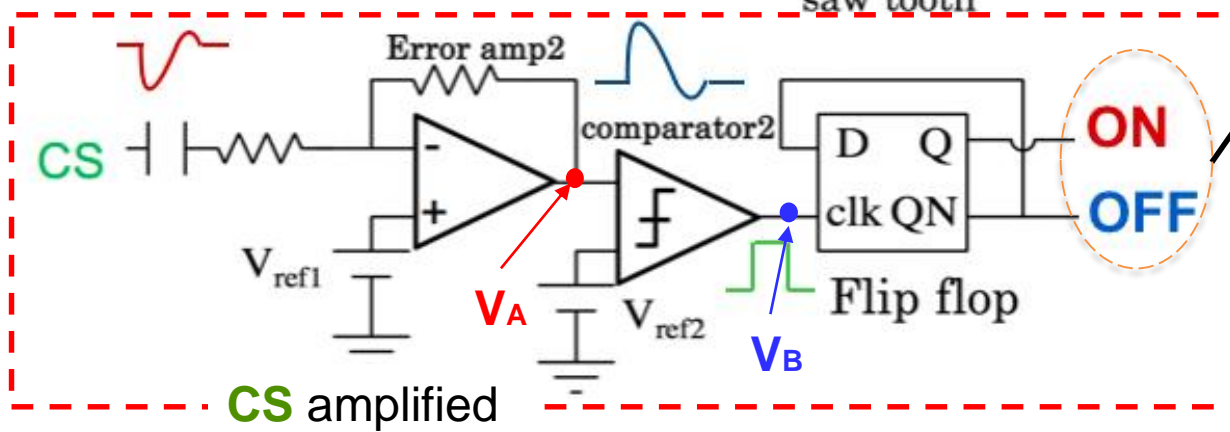


Amplification circuit & Control circuit



Control circuit

ON OFF signals converted to **Control circuit**



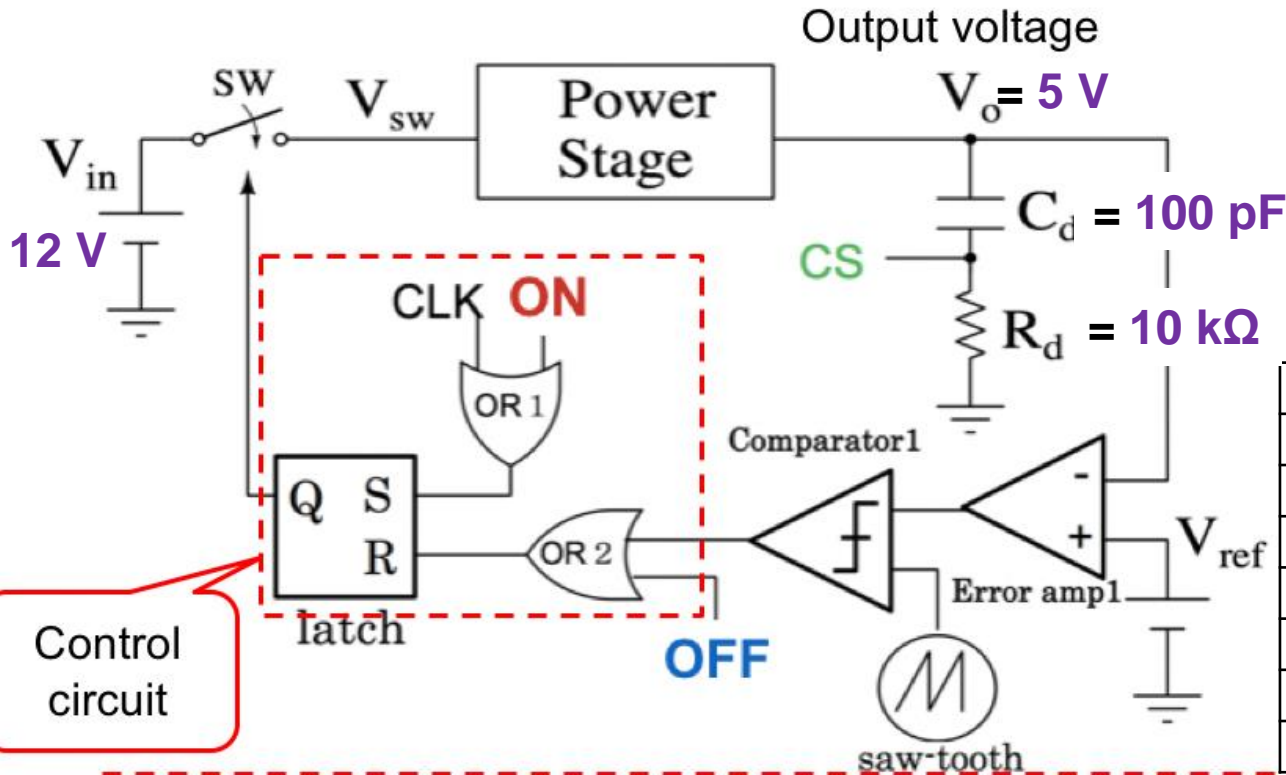
CS amplified

Amplification circuit

Outline

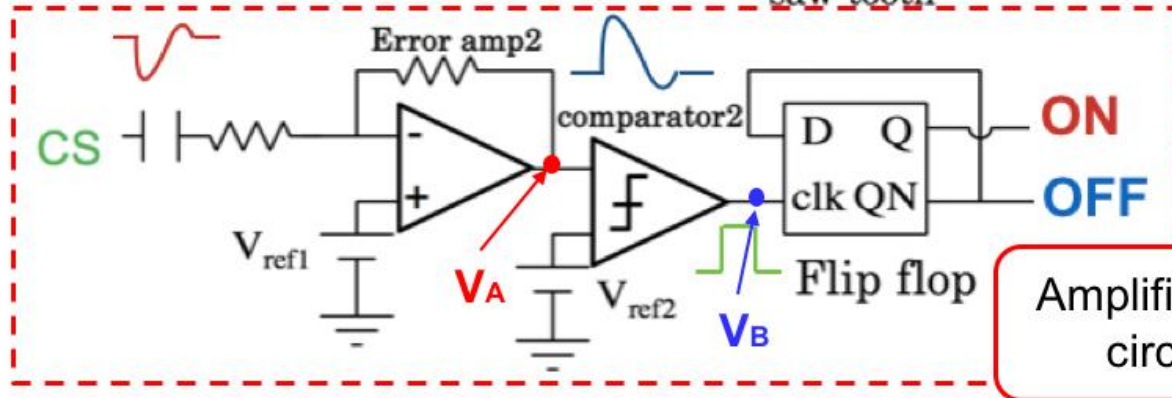
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Simulation setup



Parameter	Value
Vin	12 V
Vo	5 V
Frequency	350 kHz
L	10 μH
Co	20 μF
Rd	10 kΩ
Cd	100 pF

Control circuit



Amplification circuit

Simulation results

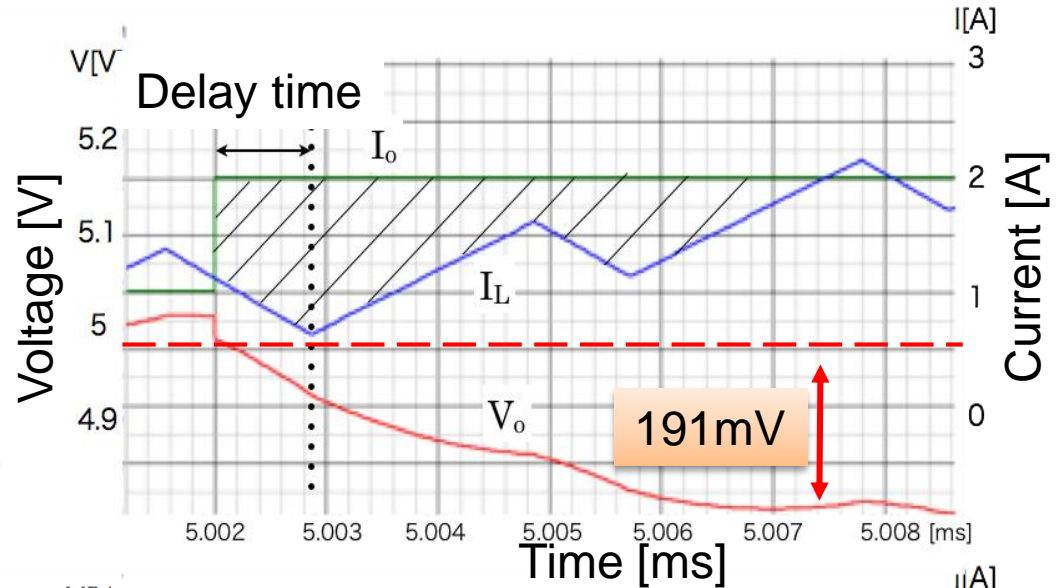
Conventional method

Undershoot
191mV

Load current

Inductor current

Output voltage



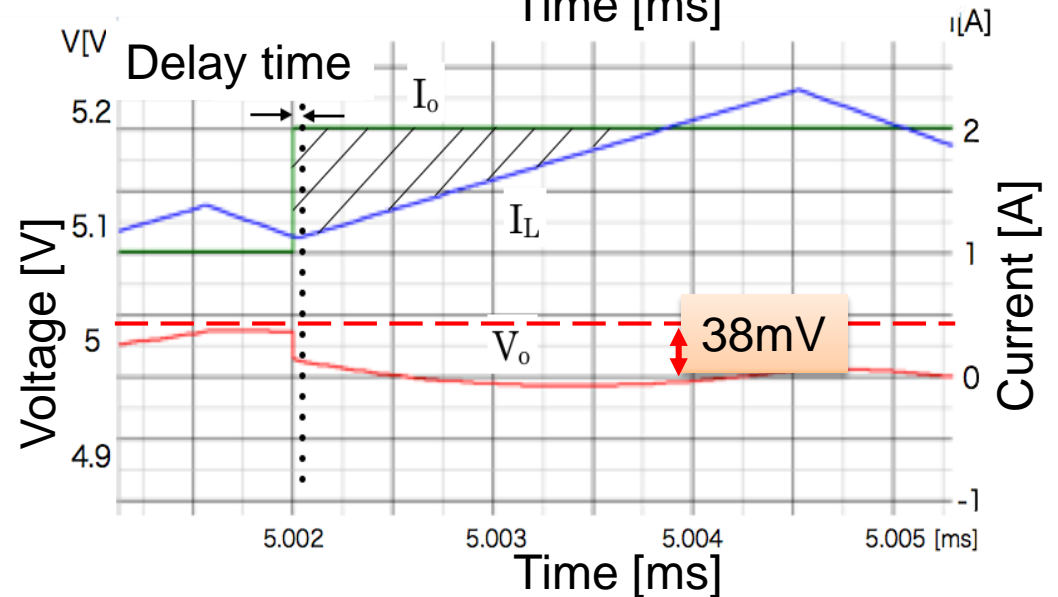
Proposed method

Undershoot
38mV

Load current

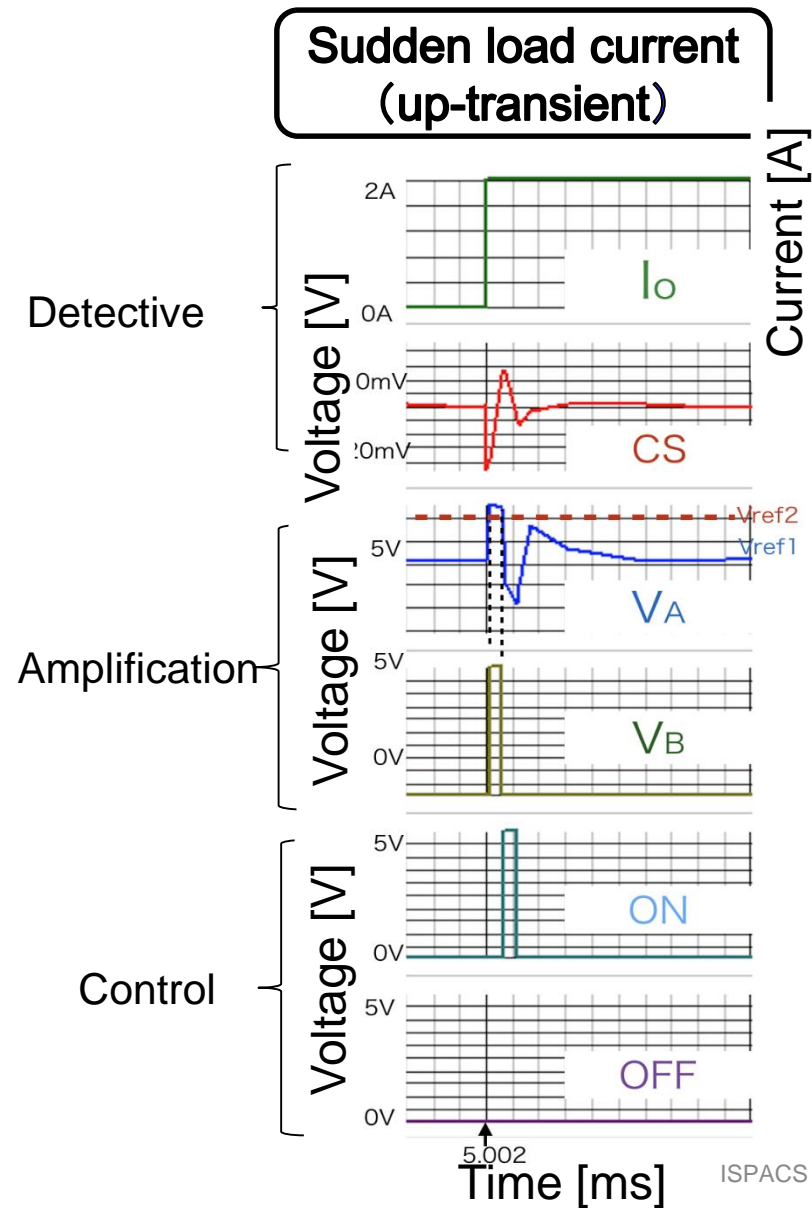
Inductor current

Output voltage



Reduce 80% 😊

Simulation Results



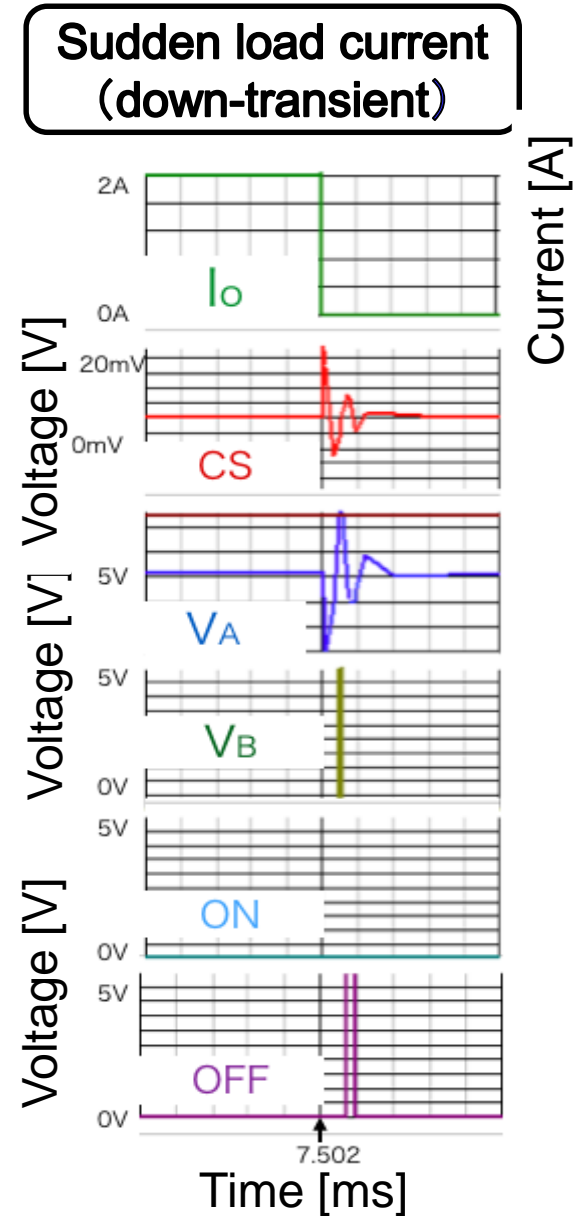
Sudden load current

Detective circuit output signal

Error amp 2 Output signal

Comparator 2 Output signal

Flip flop output signal



Logical calculation(1)

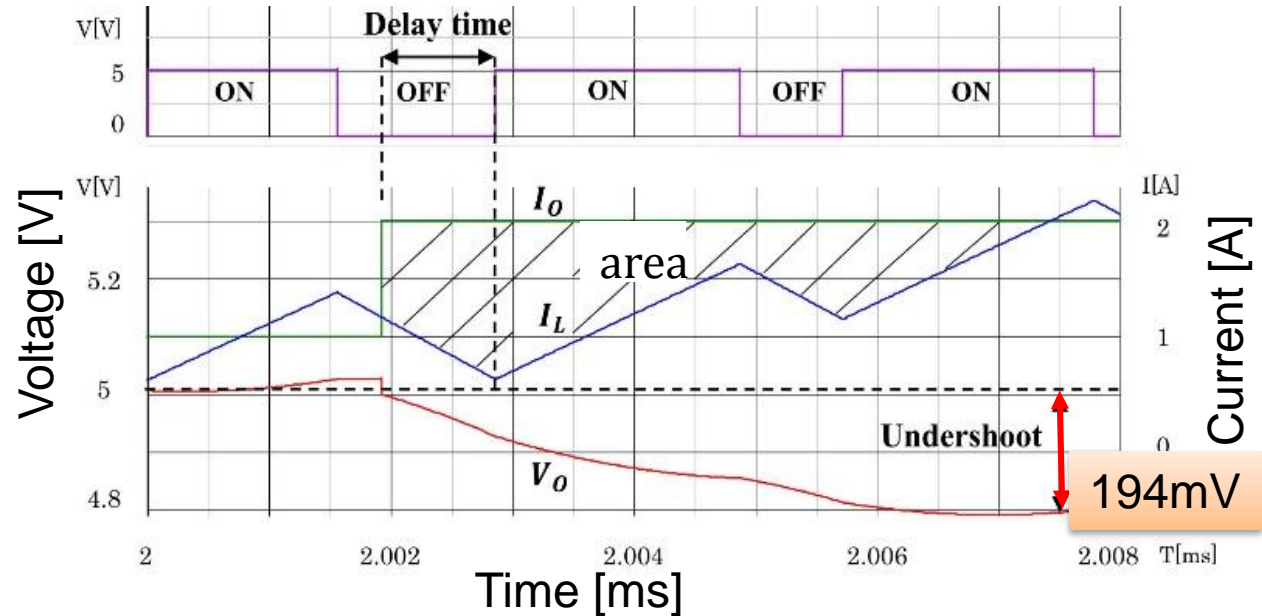
Conventional method (include delay time)

Transistor power switch

Load current I_o

Inductor current I_L

Output voltage V_o



$$Q = it$$

Total area =

$$\text{Capacity} = 3.890 \times 10^{-6} \text{C}$$

$$V_o = \frac{Q}{C_o} = \frac{3.890 \times 10^{-6} \text{C}}{20 \times 10^{-6} \text{C}} = 194 \text{mV}$$

V_o : Voltage change

Q : Capacity

i : Load current

t : Time

C_o : capacitor

Simulation result

191mV

Calculation result

194mV

Logical calculation (2)

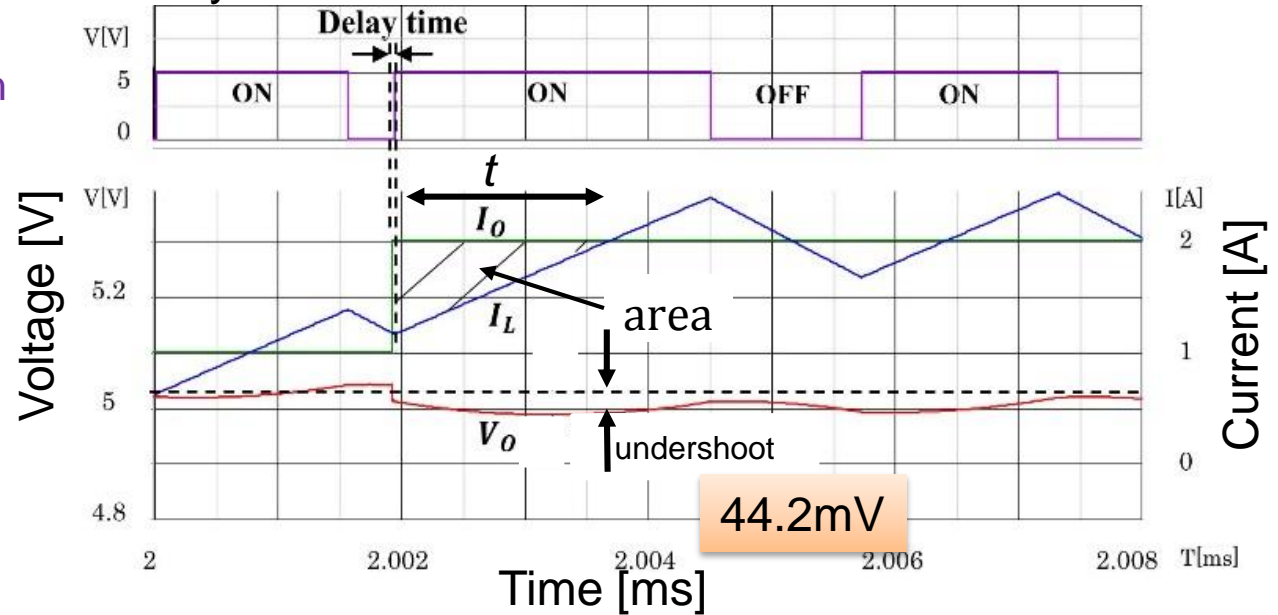
Proposed circuit (without delay time)

Transistor power switch

Load current I_o

Inductor current I_L

Output voltage V_o



$$Q = it$$

$$\text{Total area} = 8.84 \times 10^{-7} C$$

$$\begin{aligned} V_o &= \frac{Q}{C} \\ &= \frac{0.884 \times 10^{-6} C}{20 \times 10^{-6} C} \\ &= 44.2 \text{mV} \end{aligned}$$

V_o : Voltage change

Q : Capacity

i : Load current

t : Time

C_o : capacitor

Simulation result

38mV

Calculation result

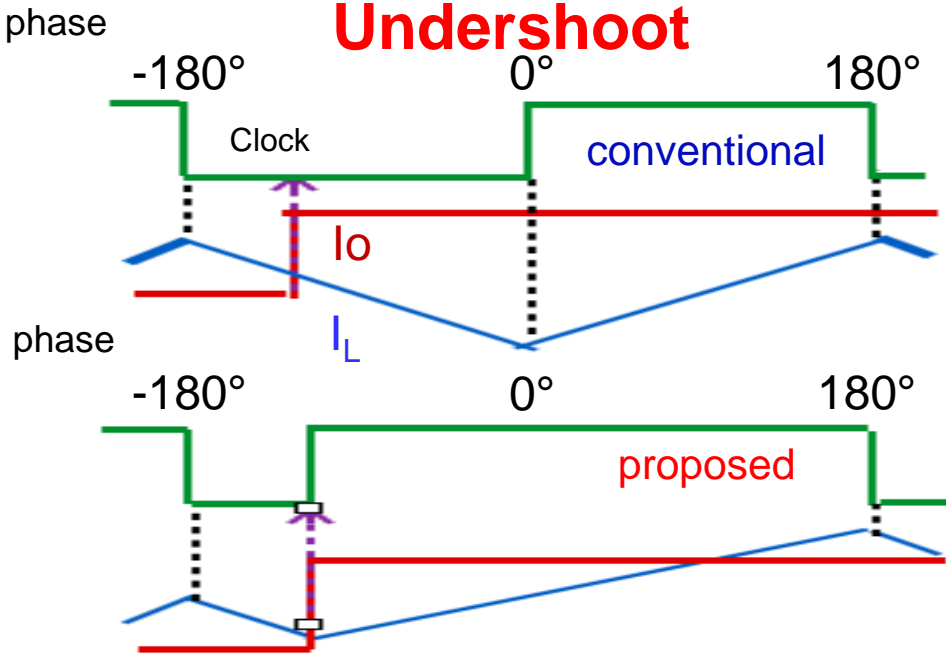
44.2mV

Conventional : 194mV

Proposed : 44.2mV

Comparison with Undershoot

Undershoot

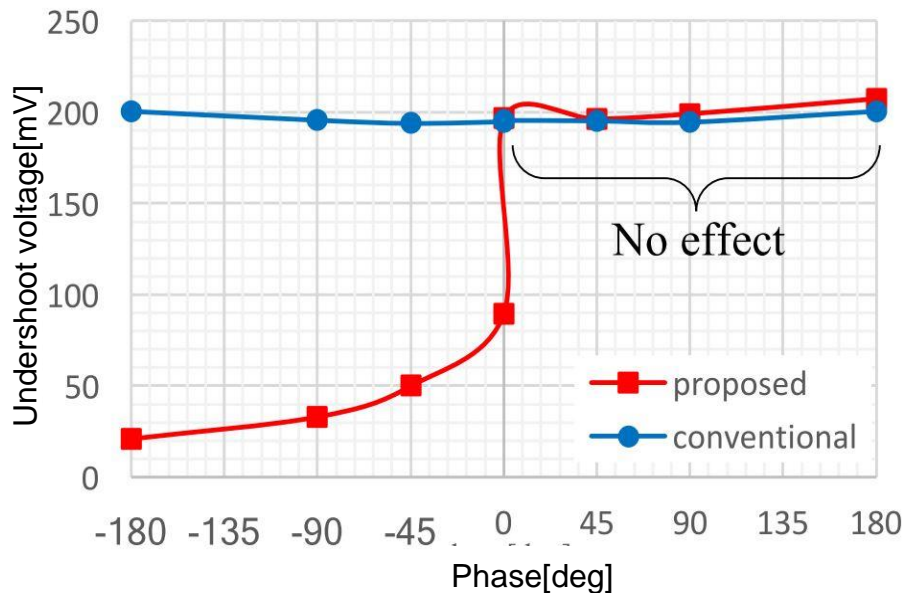


Conventional method

Inductance current does not change even if load current is generated

proposed method

When load current occur, Inductance current rises up at moment

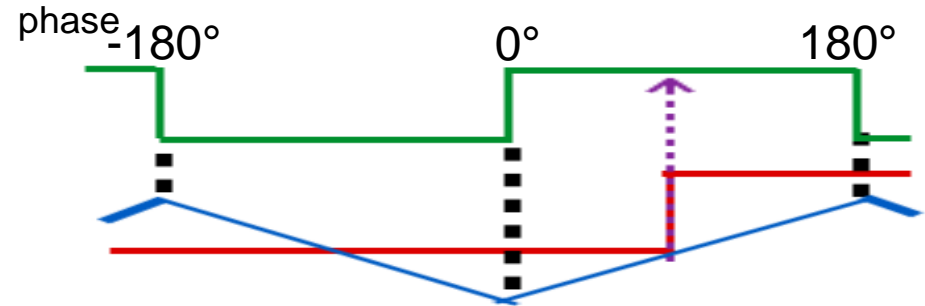


$$\frac{T_{ON}}{T} \times 360^\circ = \text{Phase}$$

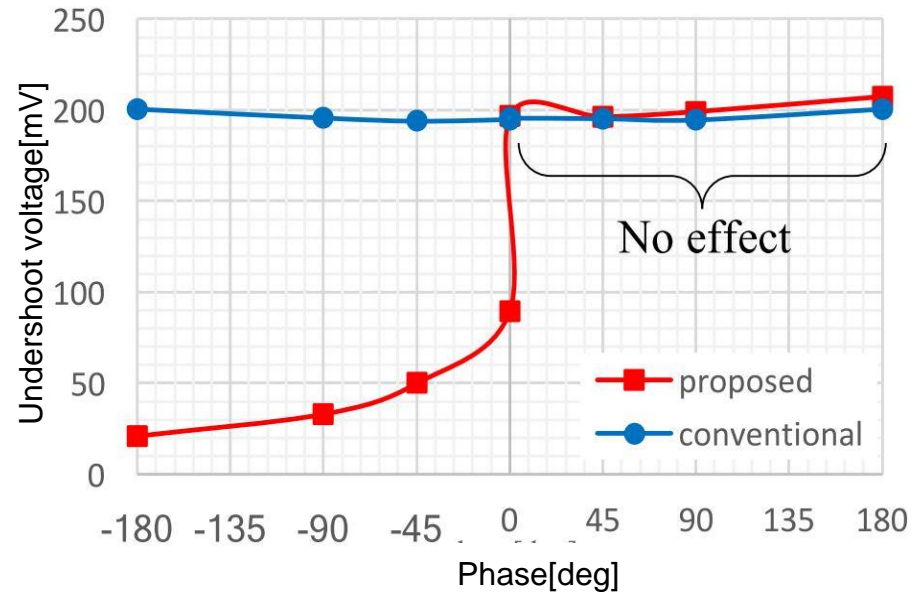
**Phase Between
-180° to 0°**

Undershoot

**NO effects in
Conventional method &
proposed method**

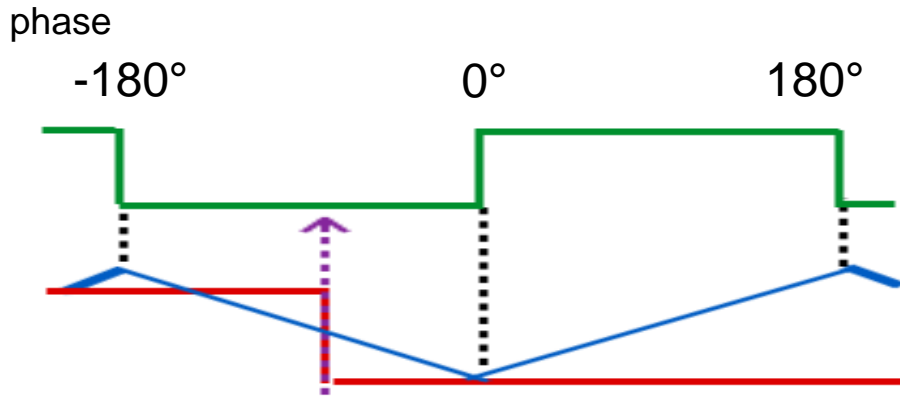


**Phase Between
0° to 180°**

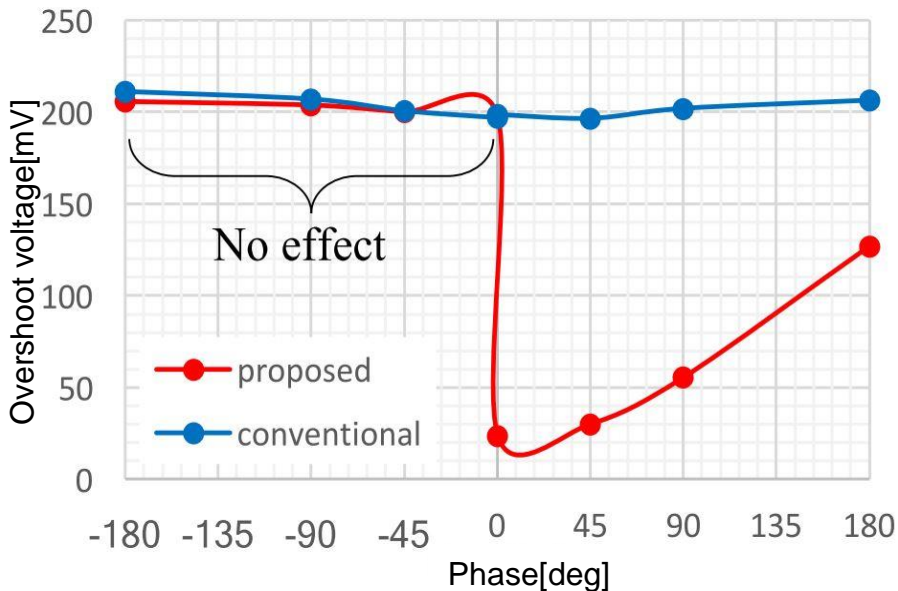


Comparison with Overshoot

Overshoot



**NO effects in
Conventional method
and proposed method**



**Phase Between
-180° to 0°**

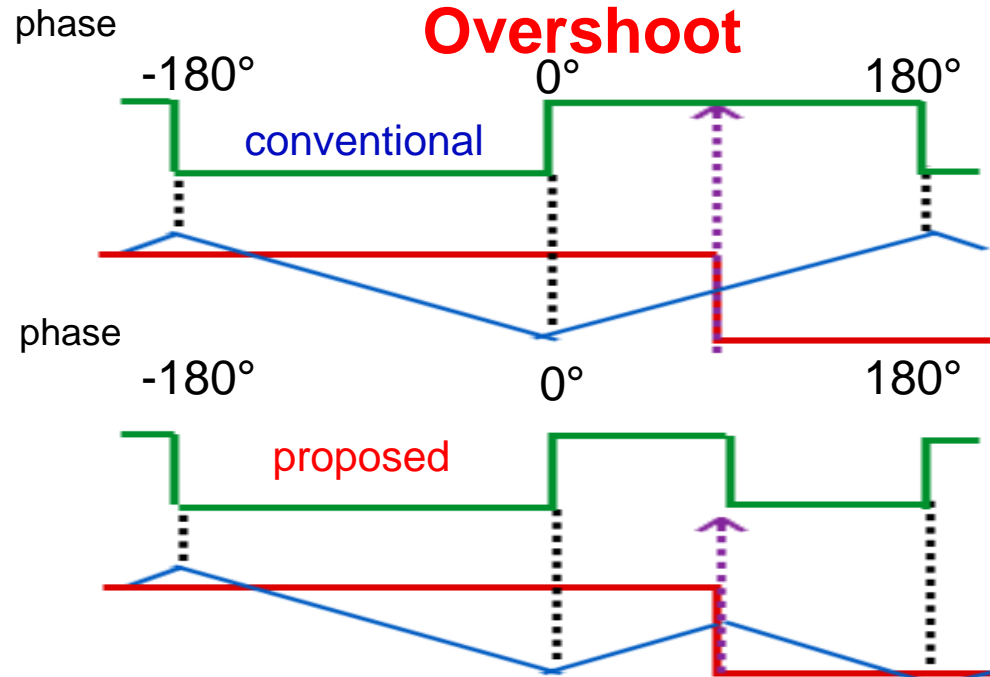
Comparison with Overshoot

Conventional method

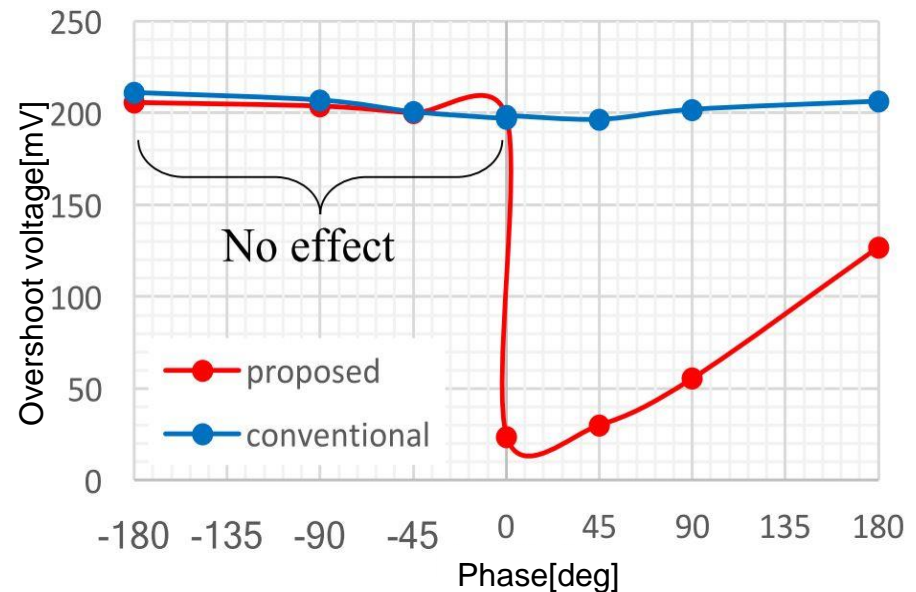
Inductance current does not change even if load current is occurred

proposed method

When load current occur, Inductance current rises down at moment

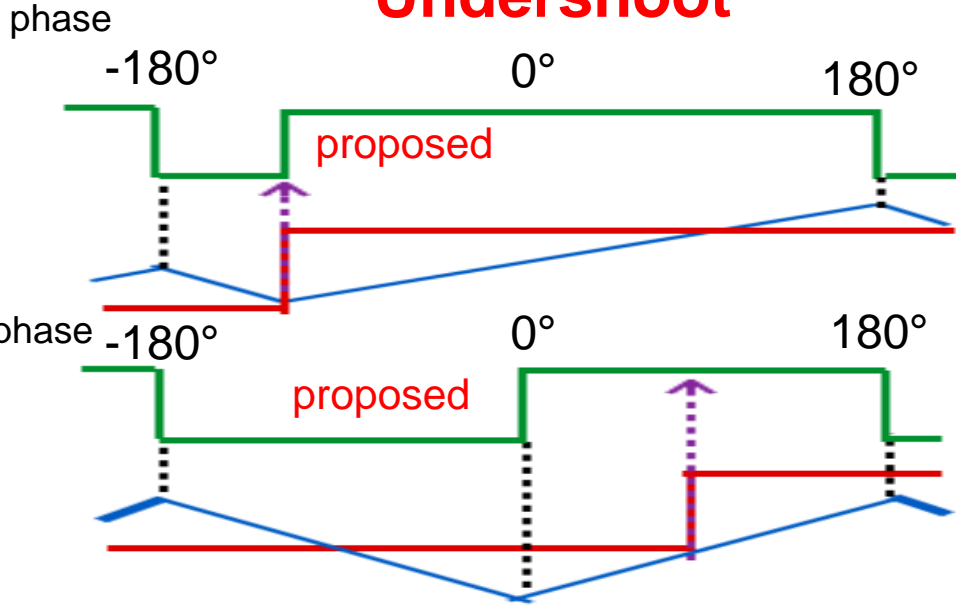


Phase Between 0° to 180°



Comparison with Clock Frequency(1)

Undershoot

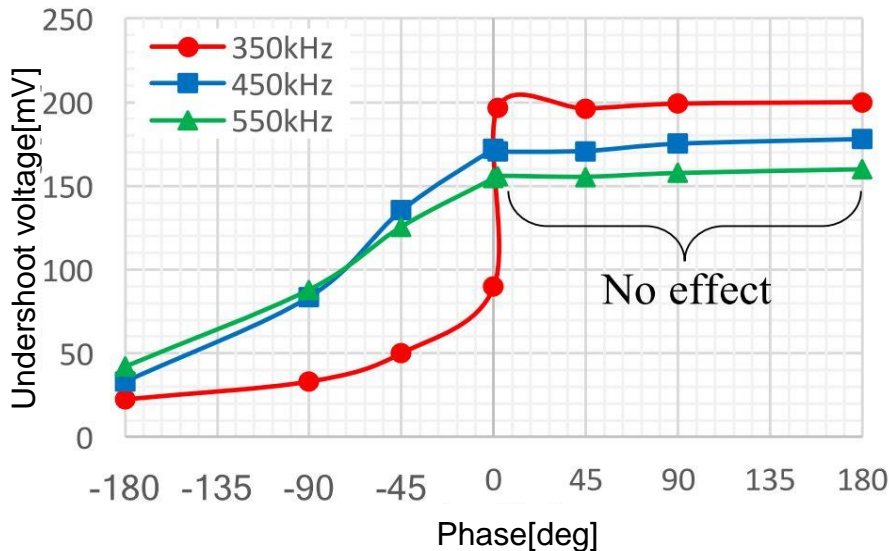


Phase -100°

When the load current occur, inductance current rises up at moment

Phase 90°

Inductance current does not change even if load current is occurred



Phase Between 0° to 180°

No effect

Comparison with Clock Frequency(2)

Phase -90°

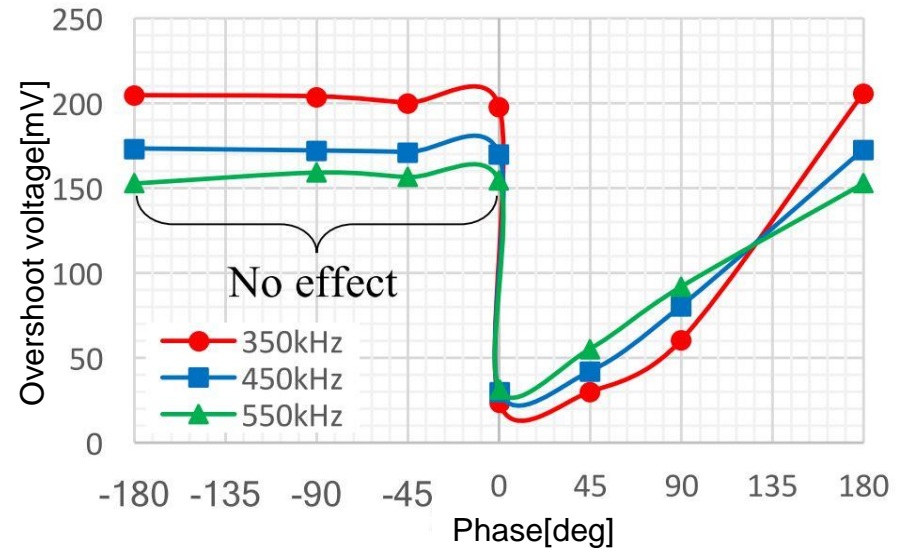
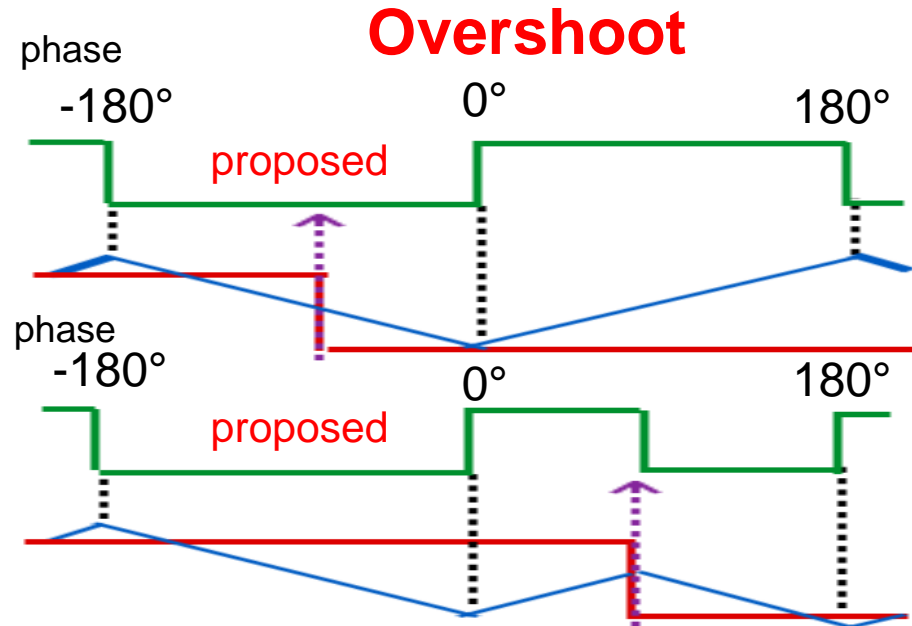
When the load current occur, Inductance current rises up at moment

Phase 90°

Inductance current does not change even if load current is occurred

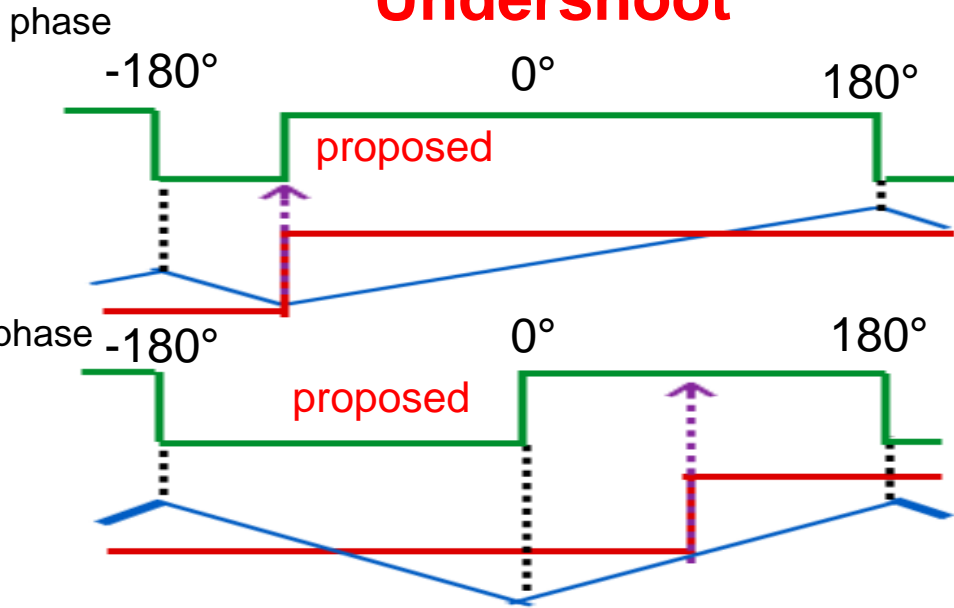
Phase Between -180° to 0°

No effect



Comparison with Load current(1)

Undershoot

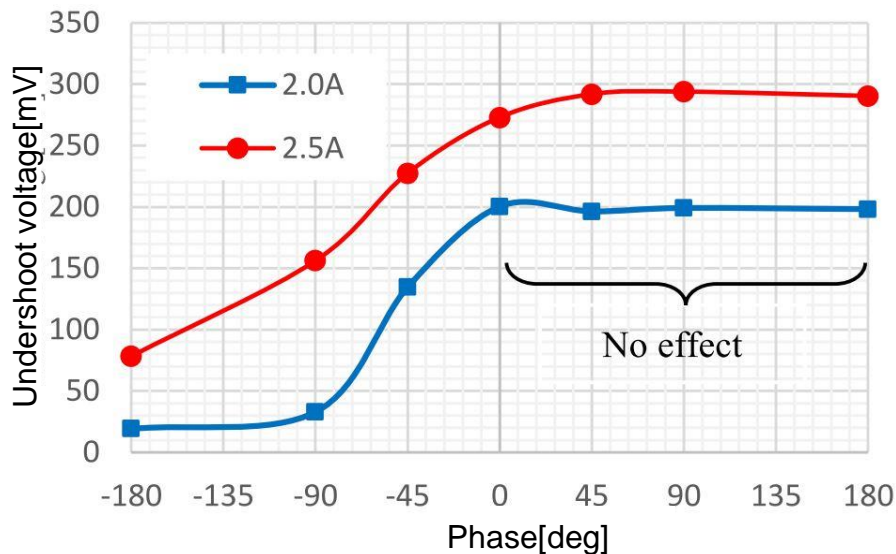


Phase -100°

When the load current occur, Inductance current rises up at moment

Phase 90°

Inductance current does not change even if load current is occurred



Phase Between 0° to 180°

No effect

Comparison with Load current(2)

Phase -90°

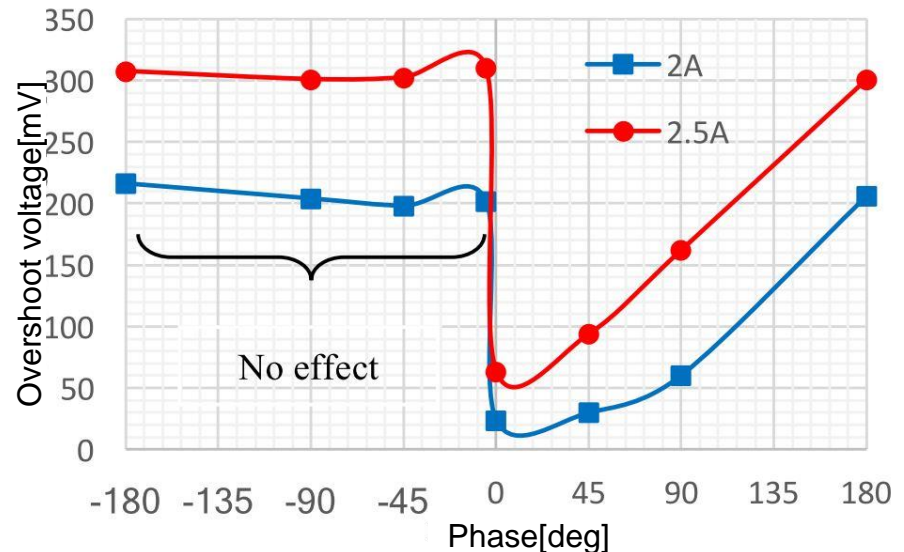
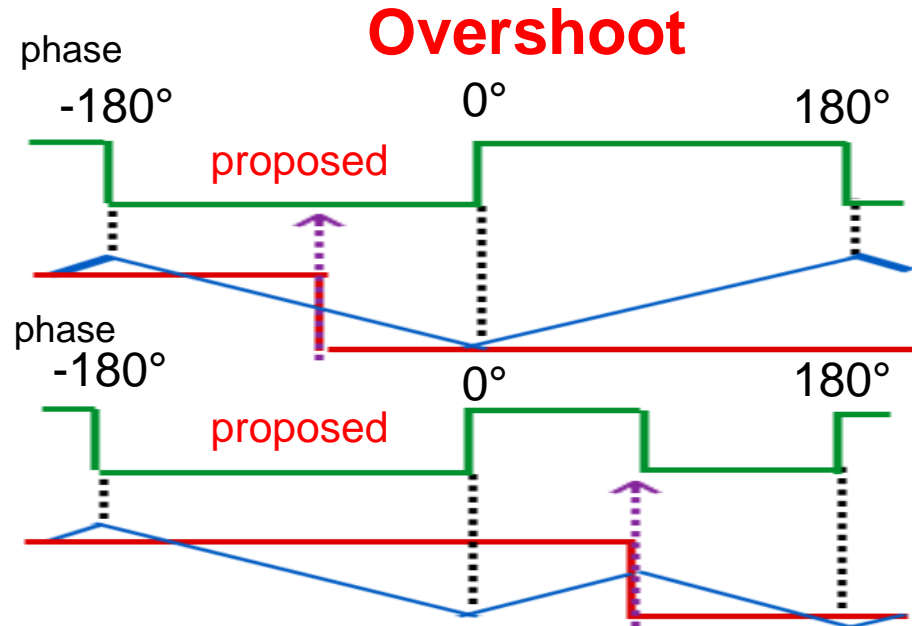
When load current occur, Inductance current rises up at moment

Phase 90°

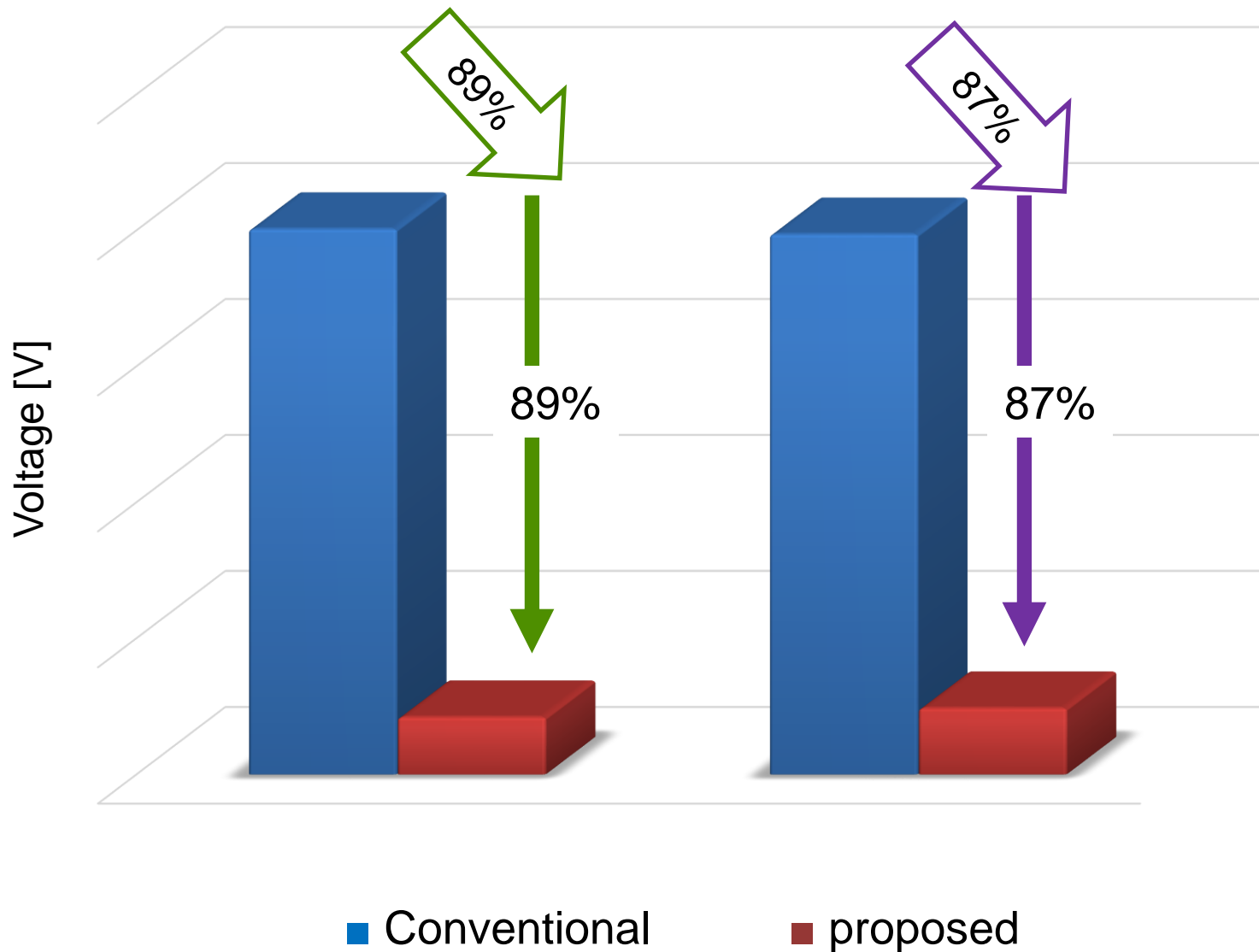
Inductance current does not change even if load current is occurred

Phase Between -180° to 0°

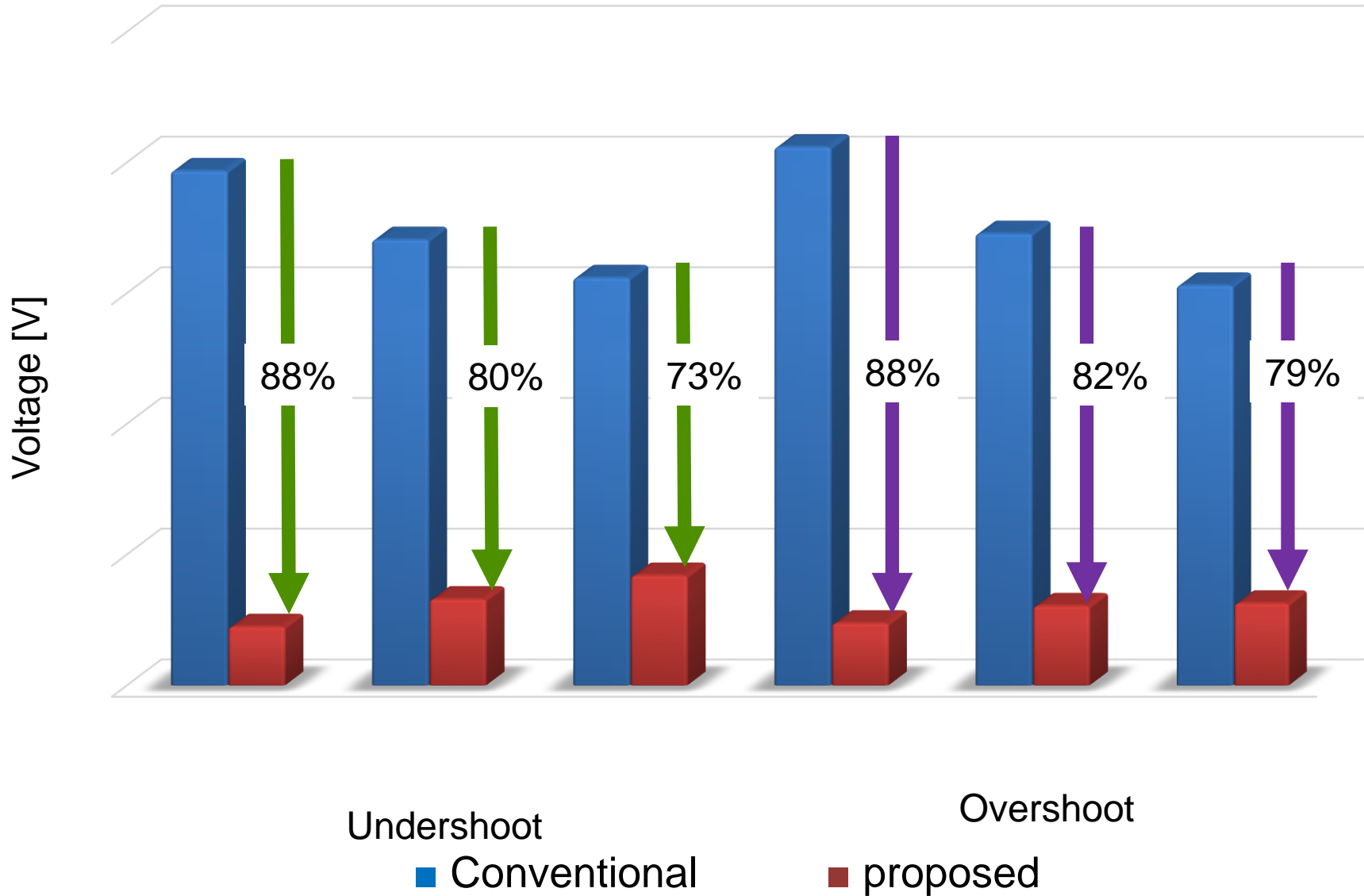
No effect



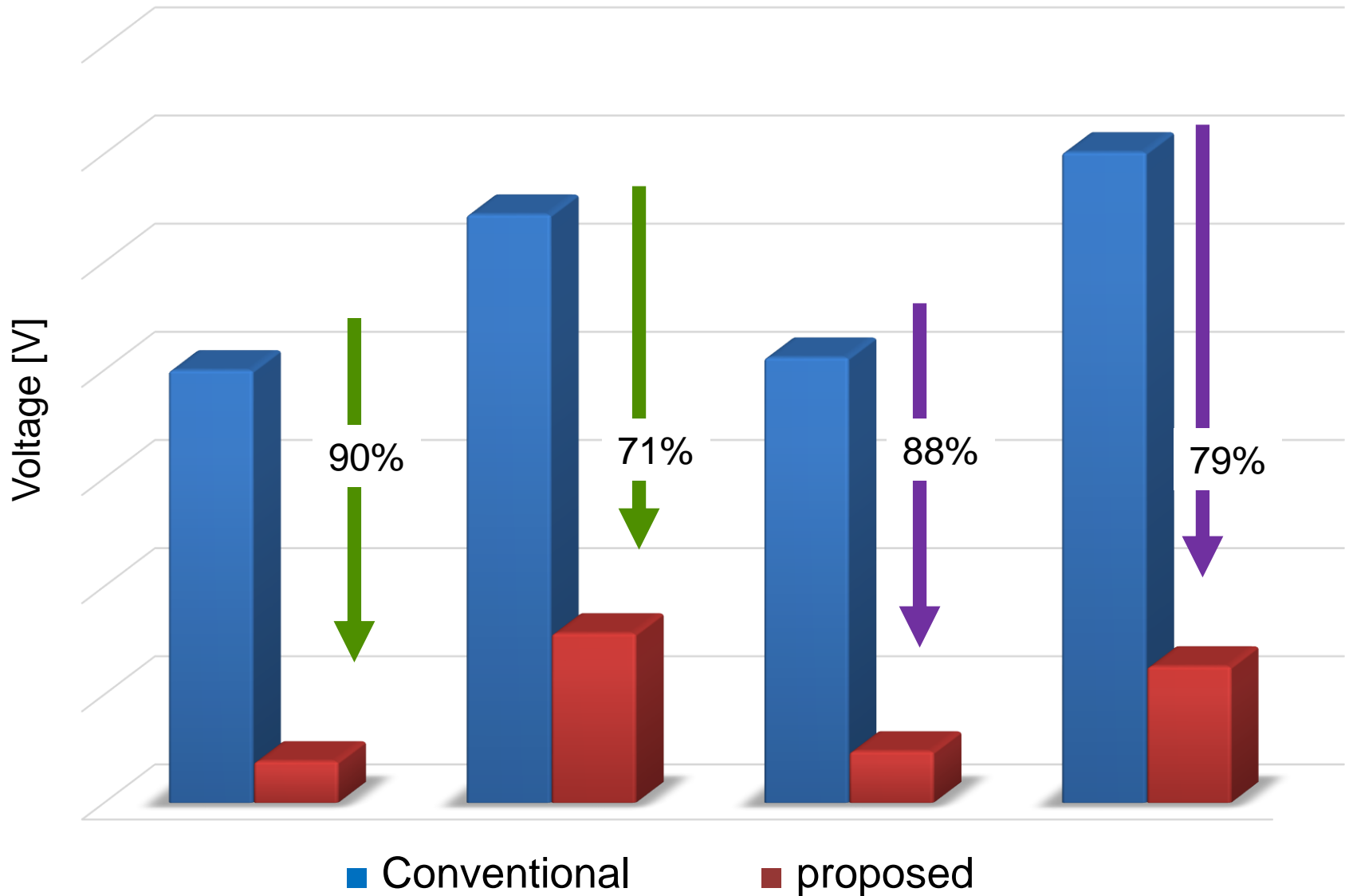
Result of conventional & proposed



Results with frequencies



Results with load currents



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Summary

- Delay time suppression
when load current occur, high-pass filter differentiates signal, amplifies, turns on transistor power switch immediately
- Proposed Buck DC/DC converter output voltage
 - undershoot/overshoot decreases approximately 80%
 - verification of calculations & simulations results
- Results Confirmed also in following
 - regulate clock frequency
 - undershoot/overshoot voltage with phase
 - load current range

Thanks for your attendance of my speech



http://www.dreamworks.com/kungfupanda/images/uploads/characters/li_action.png

Questions?