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Study of Multistage Oscilloscope Trigger Circuit

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群馬大学
GUNMA UNIVERSITY

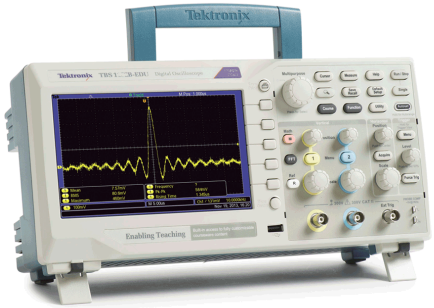
Outline

1. Research Objective
2. Analysis of Trigger Circuit
3. Multistage Trigger Circuit
4. Application to SAR-TDC
5. Summary

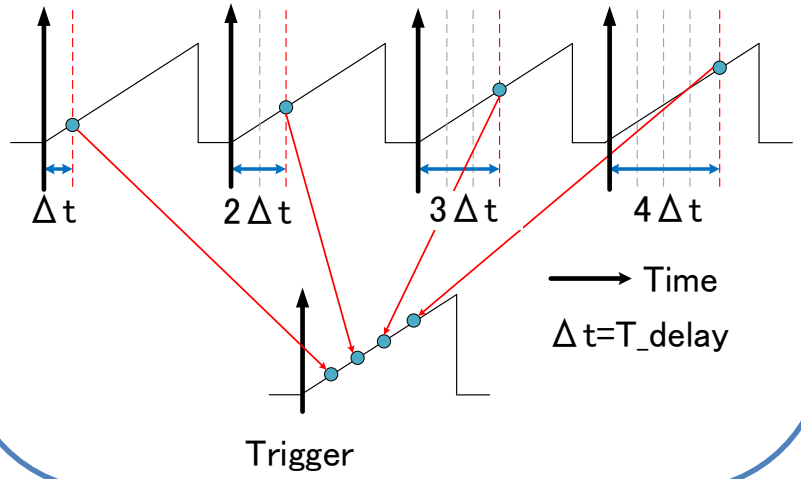
Outline

Oscilloscope Trigger Circuit

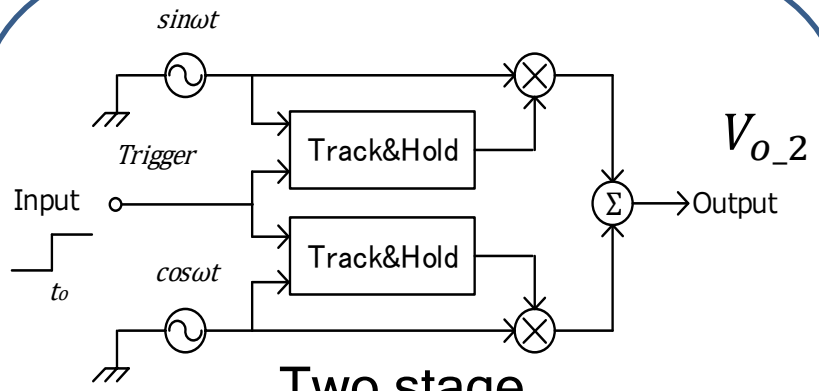
Application



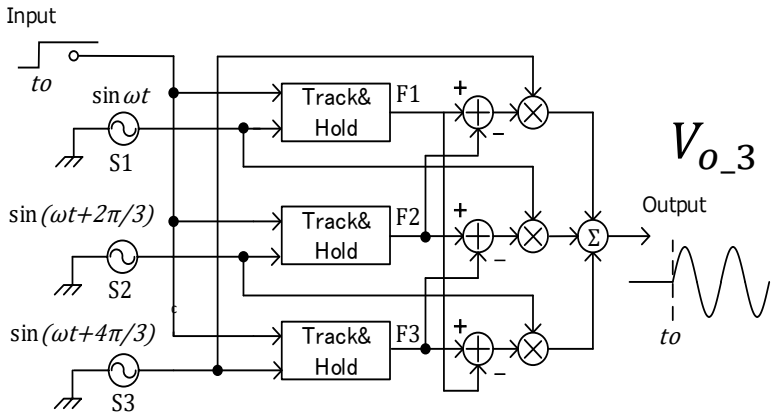
Sequential Sampling Oscilloscope



Trigger Circuit

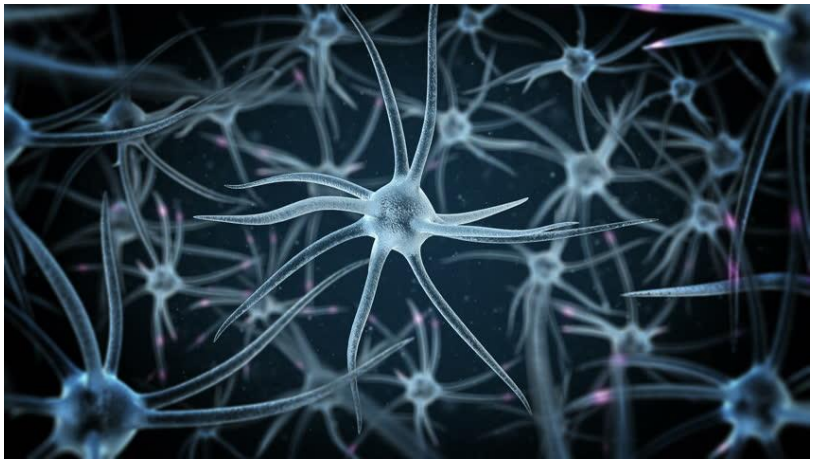


Two stage



Three stage

Research Motivation



Brain

↓

Smart

A lot of neurons

↓

Each neuron has low capability

Each transistor has only simple capability

Large number → Good performance

Research Objective

1. Analysis of basic trigger circuits
   (two-stage and three-stage)

2. Extension to an N-stage trigger circuit, and
   its output formula.

3. Application to SAR-TDC
   for one-shot timing measurement

Outline

1. Research Objective

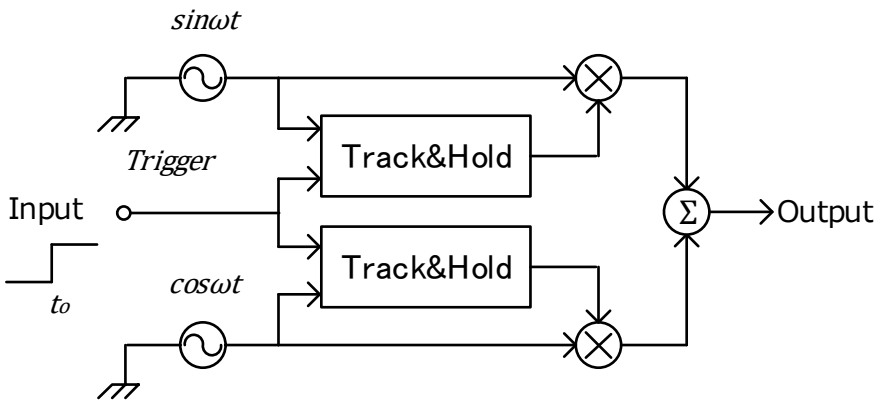
2. Analysis of Trigger Circuit
   - T/H Circuit, Gilbert Analog Multiplier
   - Basic Trigger Circuit

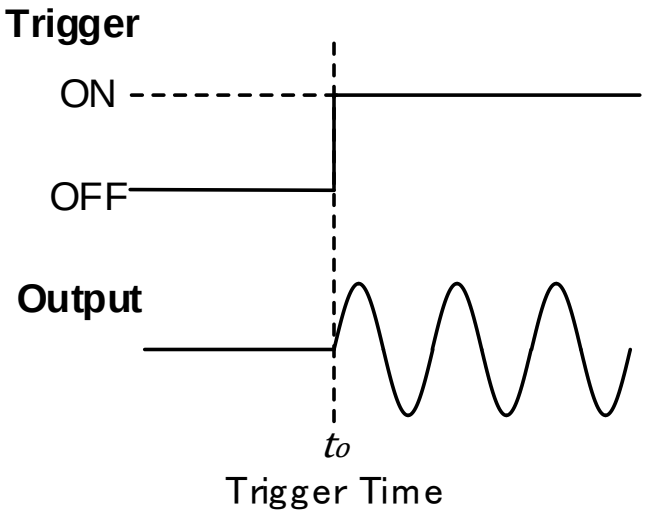
3. Multistage Trigger Circuit

4. Application to SAR-TDC

5. Summary

Trigger Circuit Configuration



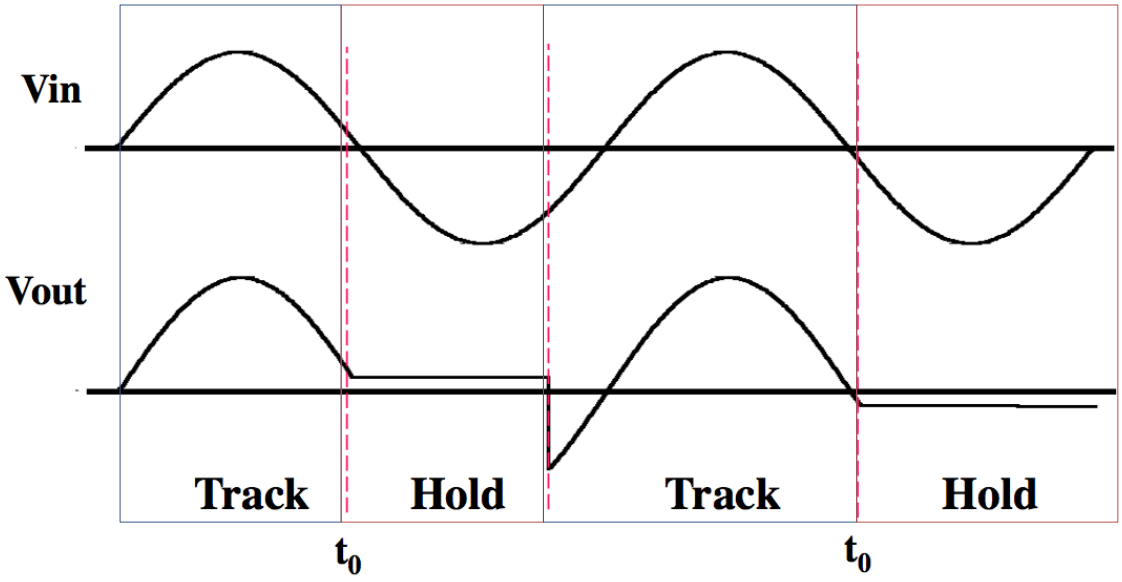


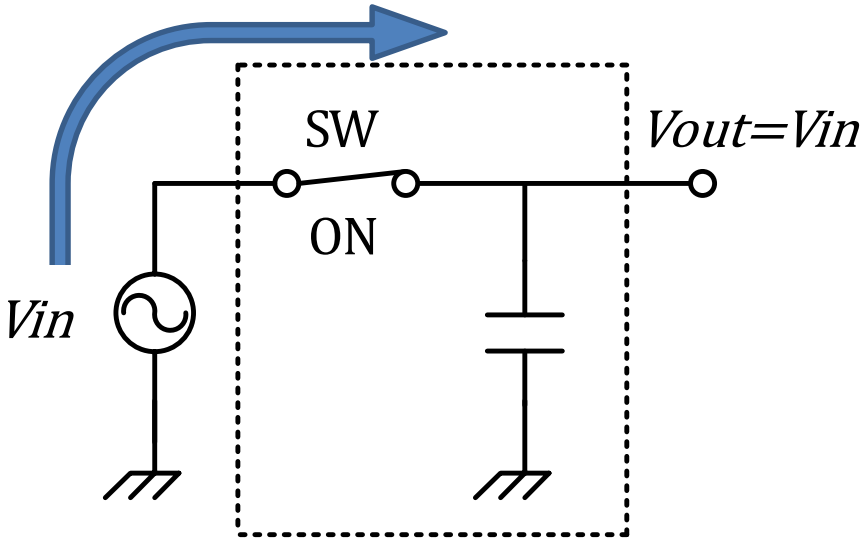
- Sinusoidal wave based on time t_0
- Output signal with zero phase

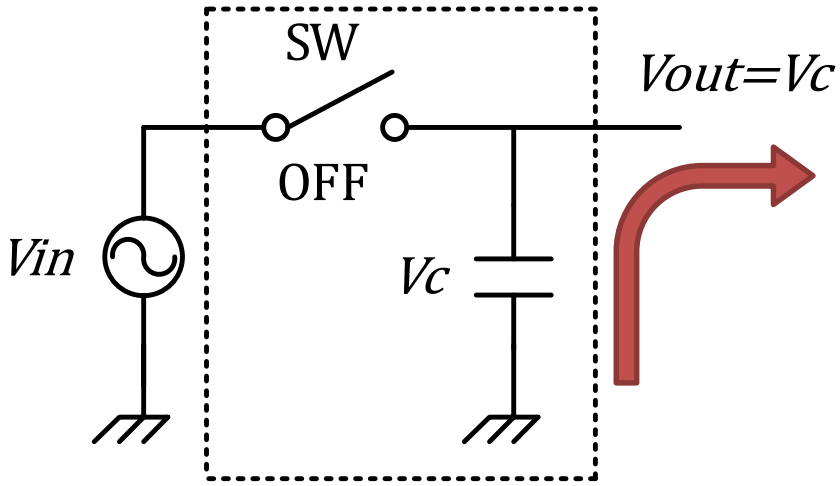
Construction with

Signal source
T/H circuit
Multiplier

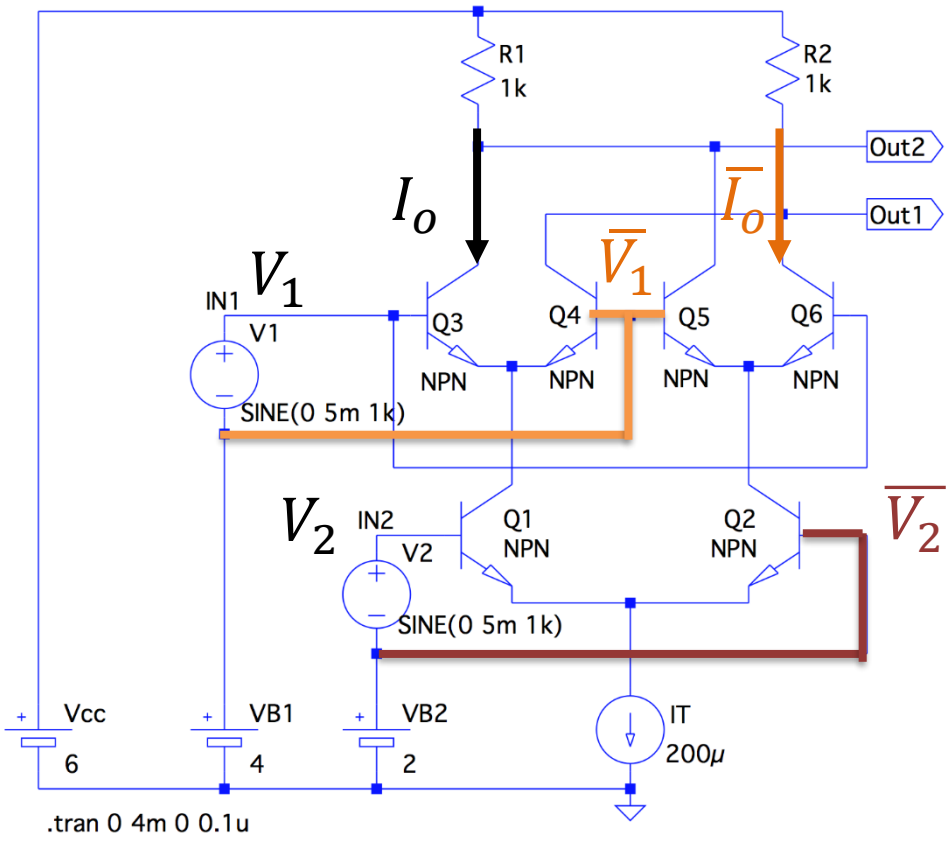
Track / Hold Circuit

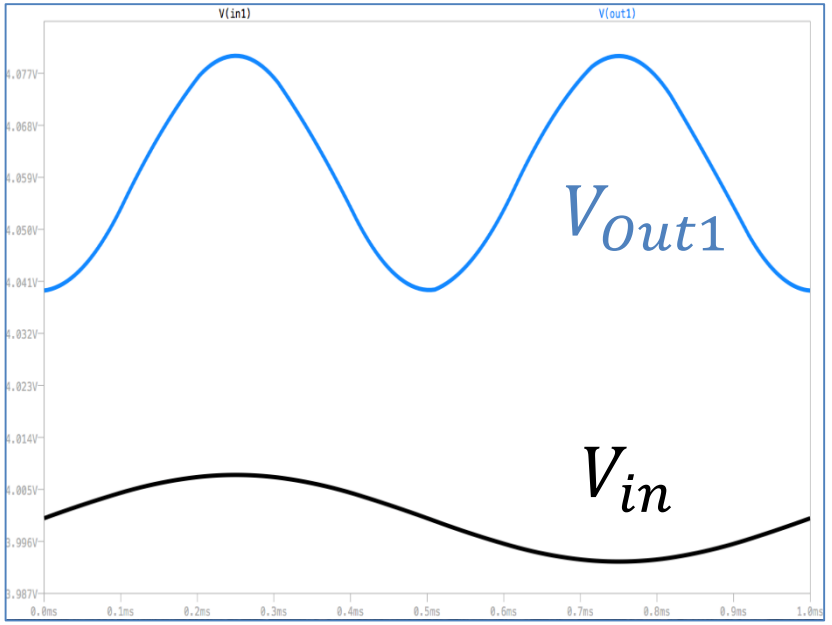






Gilbert Analog Multiplier



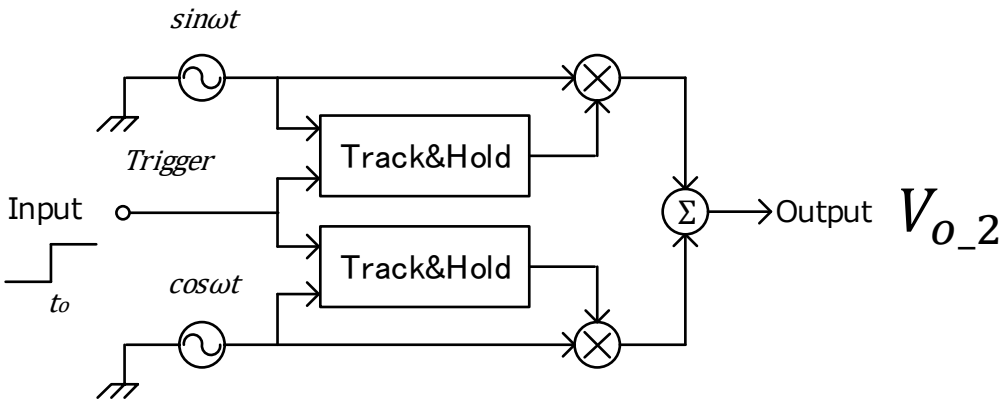


$$V_{Out1} = V_{cc} - R\overline{I_o}$$
$$V_{Out2} = V_{cc} - RI_o$$

$$V_{Out1} - V_{Out2} = R(I_o - \overline{I_o}) = RI_T * \tanh\left[\frac{V_1 - \overline{V_1}}{2V_T}\right] * \tanh\left[\frac{V_2 - \overline{V_2}}{2V_T}\right]$$

$$\cong V_1 * V_2$$

Analysis of Two-stage Trigger Circuit.



・Track mode

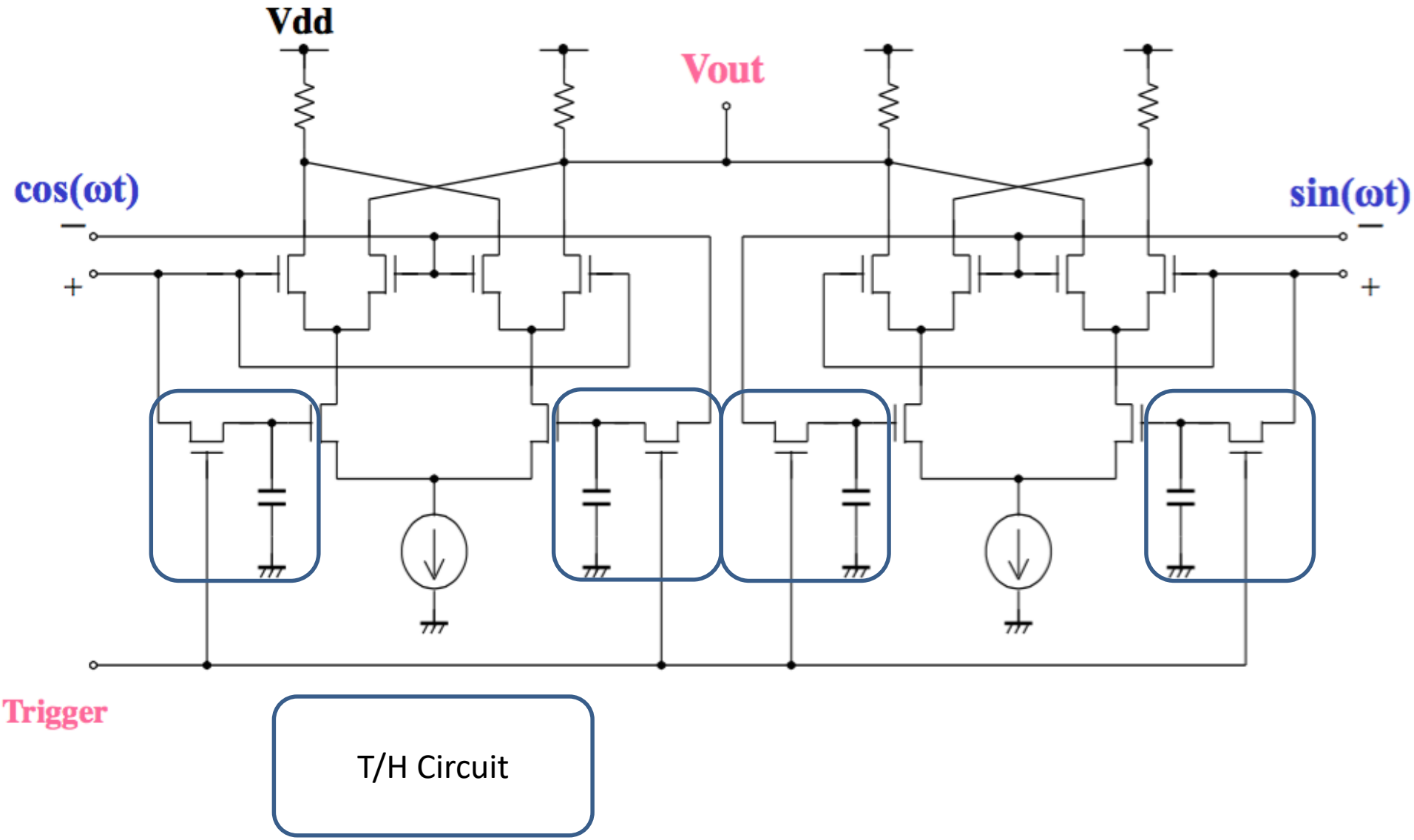
$$V_{o\,Track} = \cos(\omega t)\cos(\omega t) + \cos\left(\omega t + \frac{\pi}{2}\right)\cos\left(\omega t + \frac{\pi}{2}\right)$$
$$= \cos^2(\omega t) + \sin^2(\omega t)$$
$$= 1$$

・Hold mode

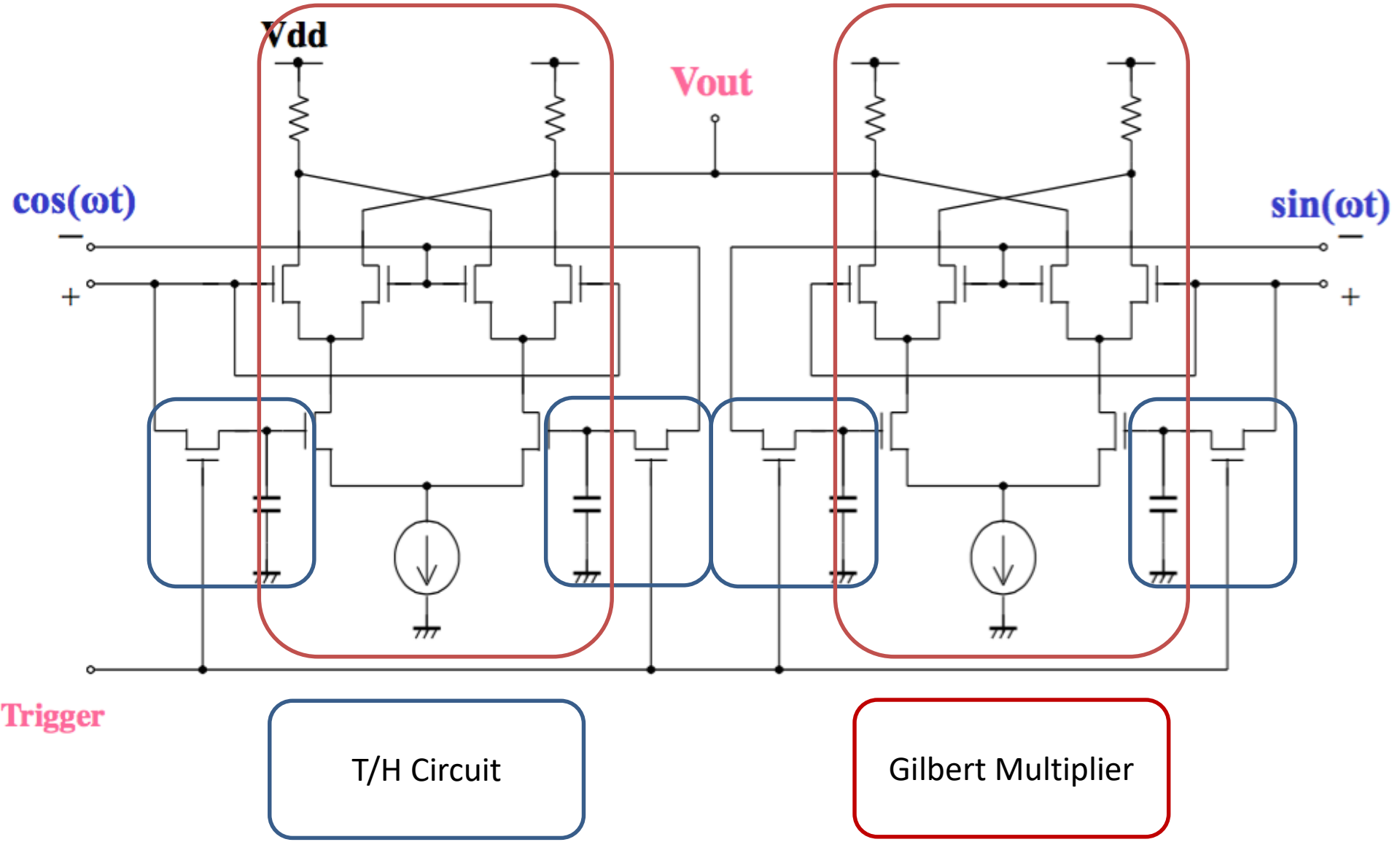
$$V_{o\,Hold} = \cos(\omega t)\cos(\omega t_0) + \sin(\omega t)\sin(\omega t_0)$$
$$= \cos(\omega(t - t_0))$$

※ Trigger time:t_0

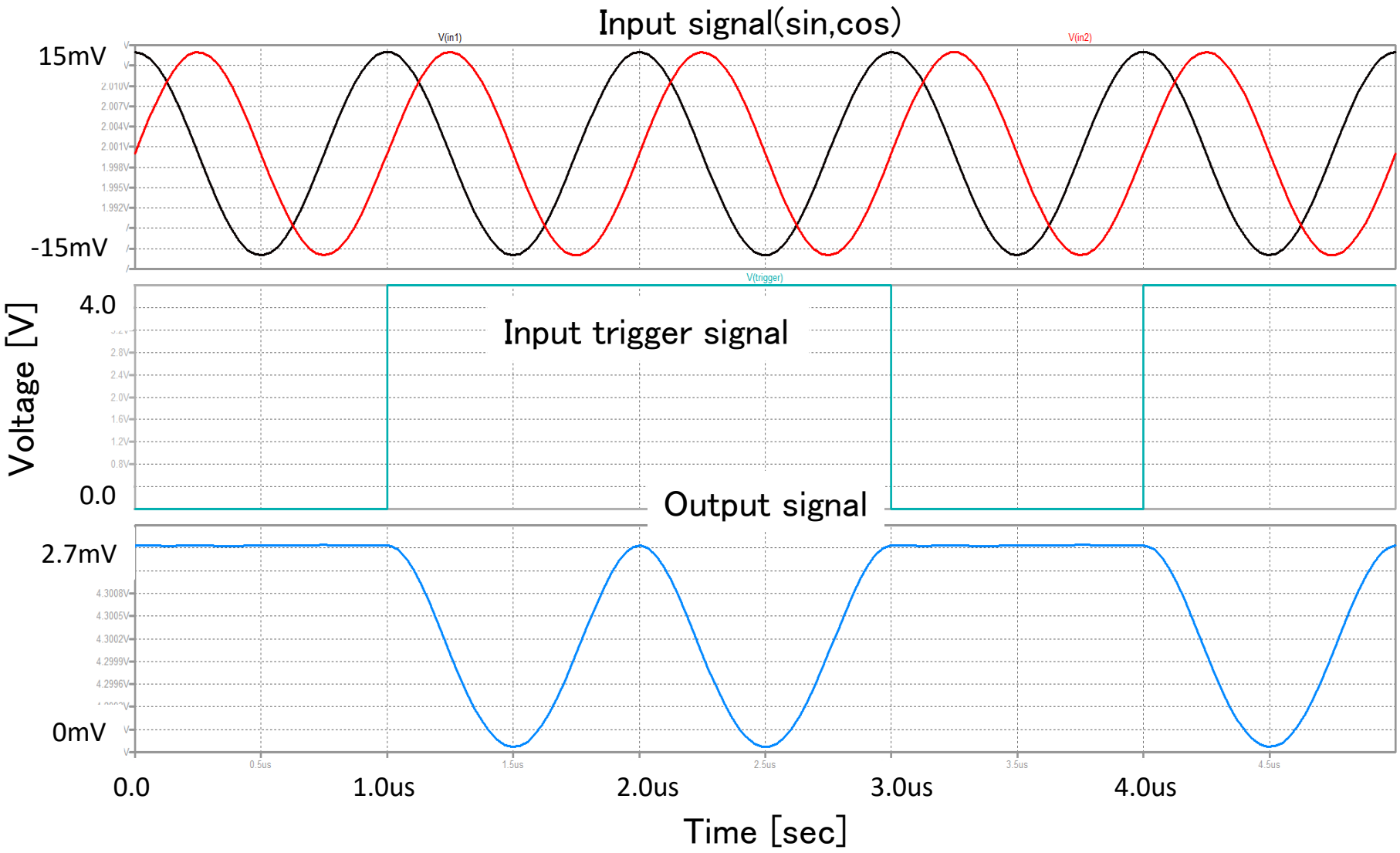
Two-stage CMOS Trigger Circuit



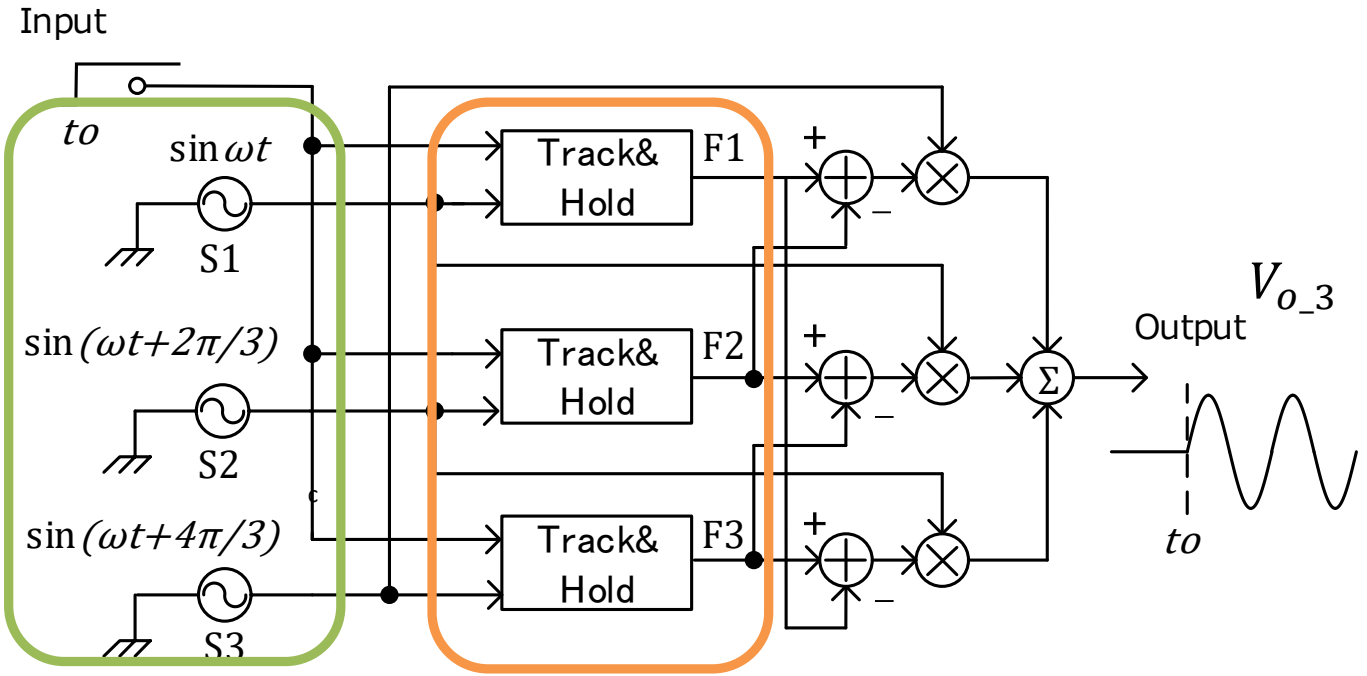
Two-stage CMOS Trigger Circuit



Simulation of Two-stage Trigger Circuit



Three-stage Trigger Circuit



Signal source

$$S_1 = \sin \omega t \ , \ S_2 = \sin\left(\omega t + \frac{2\pi}{3}\right) , \ S_3 = \sin\left(\omega t + \frac{4\pi}{3}\right)$$

Triggered signal

$$F_1 = \sin \omega t_0 \ , \ F_2 = \sin\left(\omega t_0 + \frac{2\pi}{3}\right) , \ F_3 = \sin\left(\omega t_0 + \frac{4\pi}{3}\right)$$

Analysis of Three-stage Trigger Circuit

Signal source

$$S_1 = \sin \omega t\,,\ S_2 = \sin\left(\omega t + \frac{2\pi}{3}\right),\ S_3 = \sin\left(\omega t + \frac{4\pi}{3}\right)$$

Triggered T/H circuit output

$$F_1 = \sin \omega t_0\,,\ F_2 = \sin\left(\omega t_0 + \frac{2\pi}{3}\right),\ F_3 = \sin\left(\omega t_0 + \frac{4\pi}{3}\right)$$

・Track mode

$$Vo_{track} = S_1(S_2 - S_3) + S_2(S_3 - S_1) + S_3(S_1 - S_2)$$

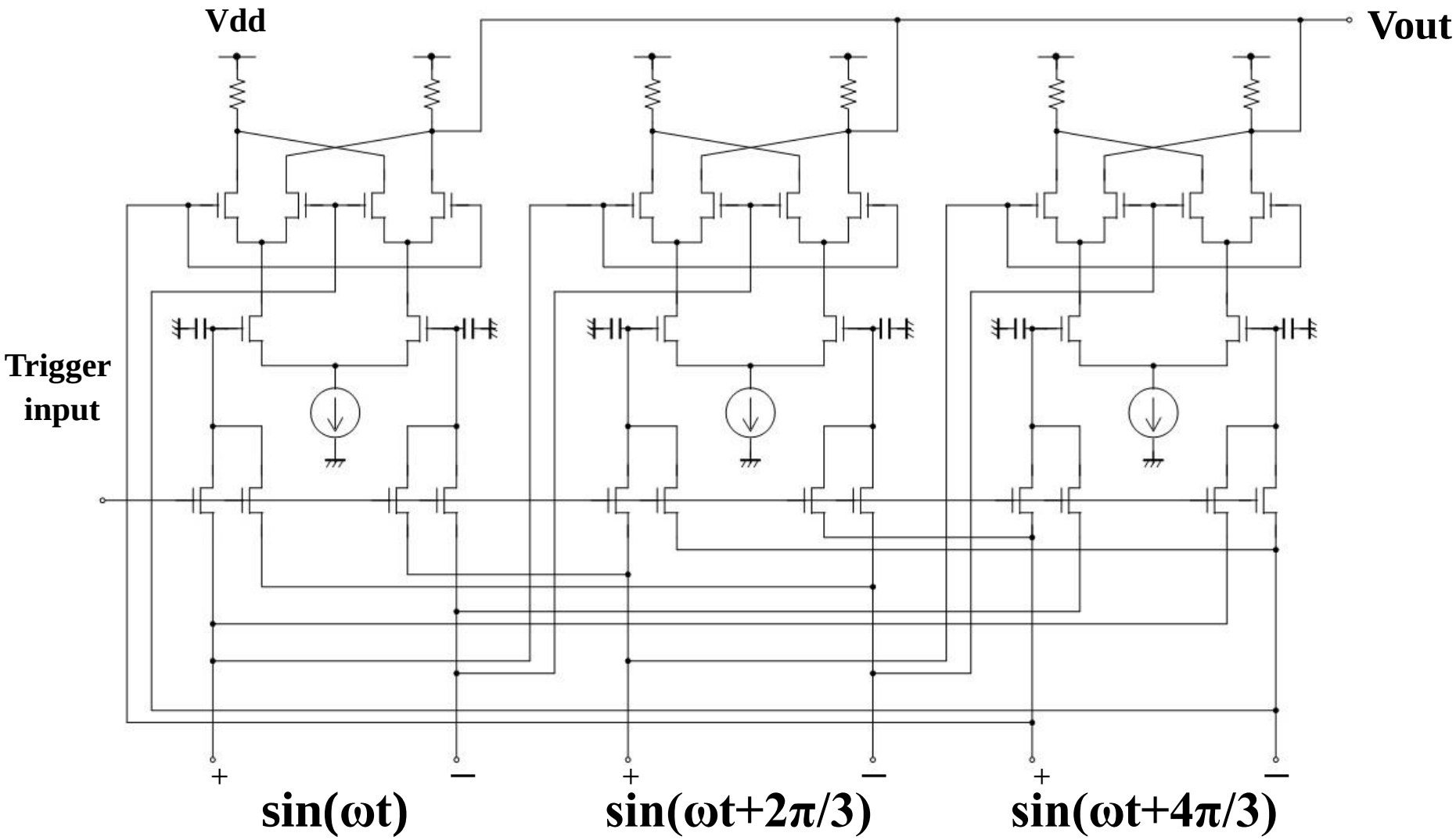
$$= 0 \qquad \textbf{(Constant)}$$

・Hold mode

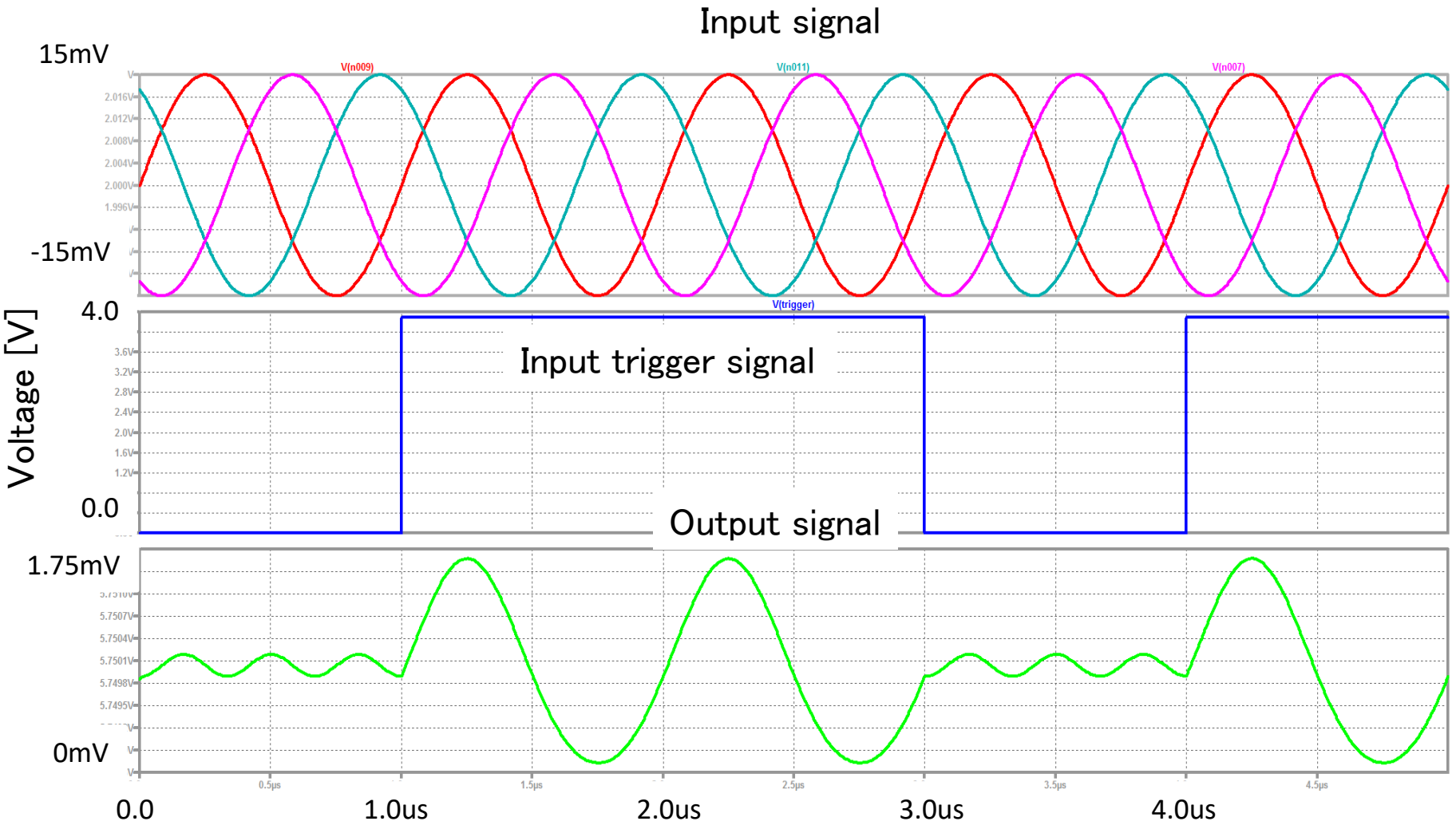
$$Vo_{hold} = S_1(F_2 - F_3) + S_2(F_3 - F_1) + S_3(F_1 - F_2)$$

$$= \frac{3\sqrt{3}}{2}\sin(\omega(t - t_0))$$

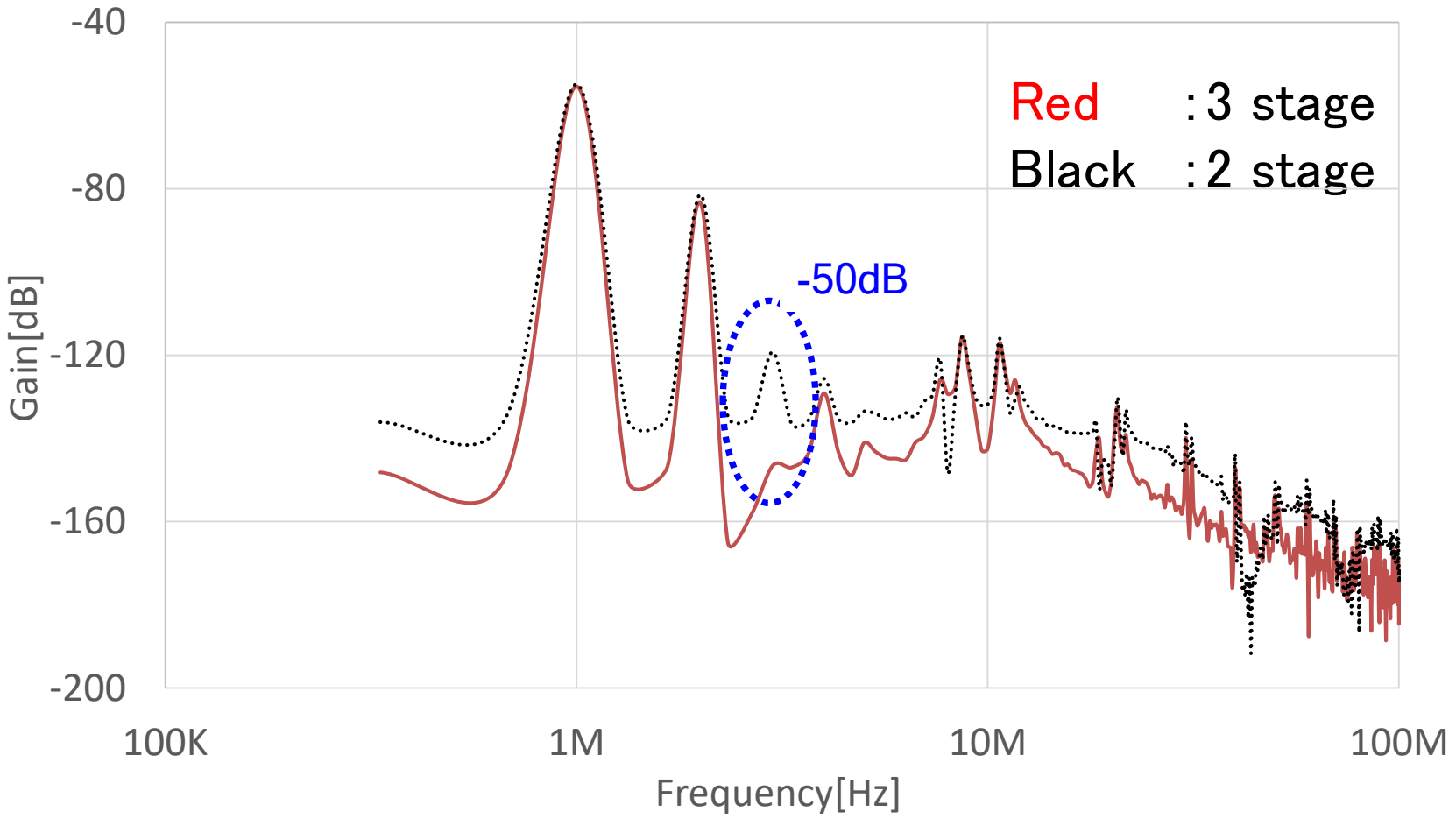
Three-stage CMOS Trigger Circuit



Simulation of Three-stage Trigger Circuit



Spectrum Comparison of Two-stage, Three-stage



Cancellation of the third harmonics due to three-stage structure.

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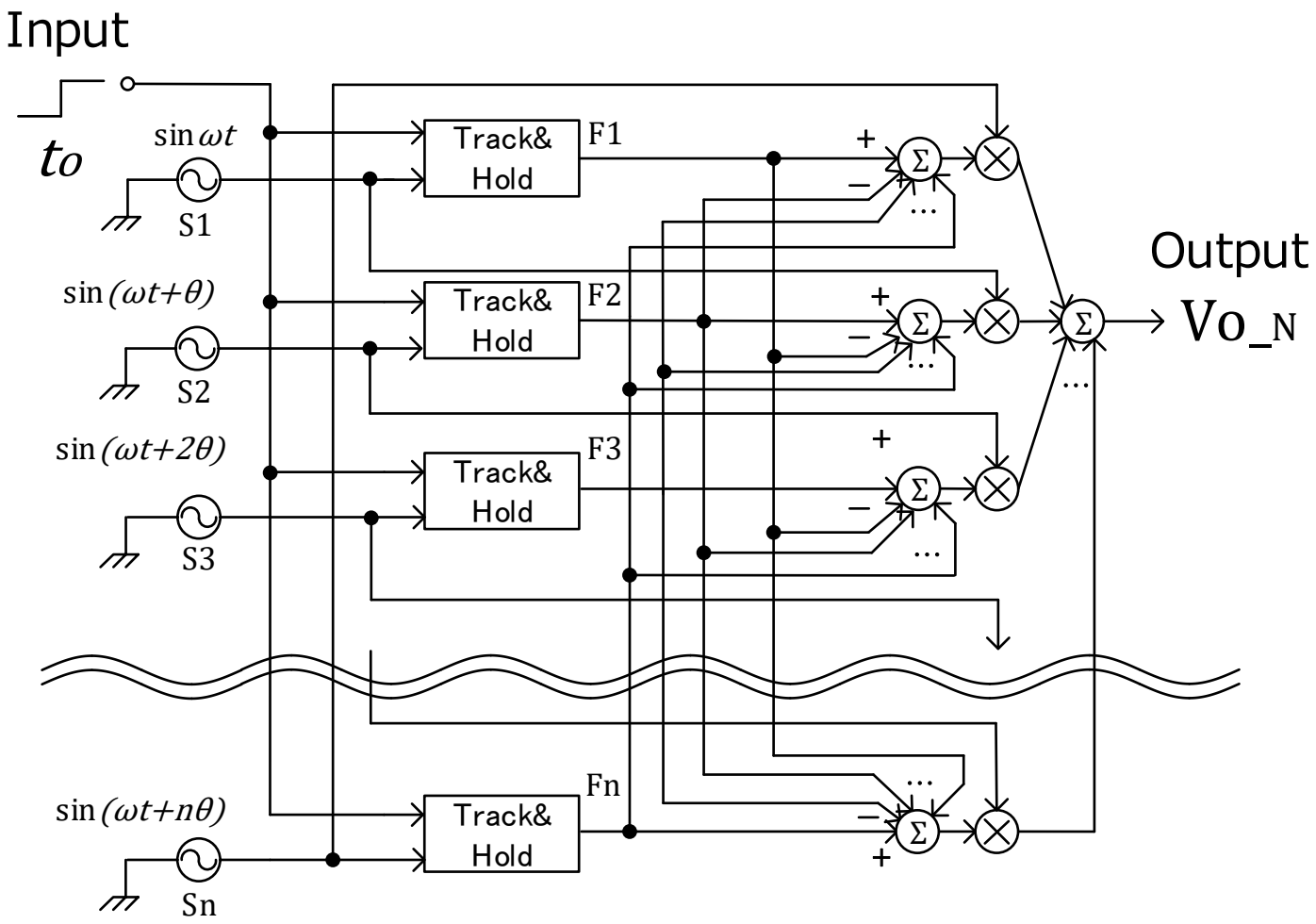
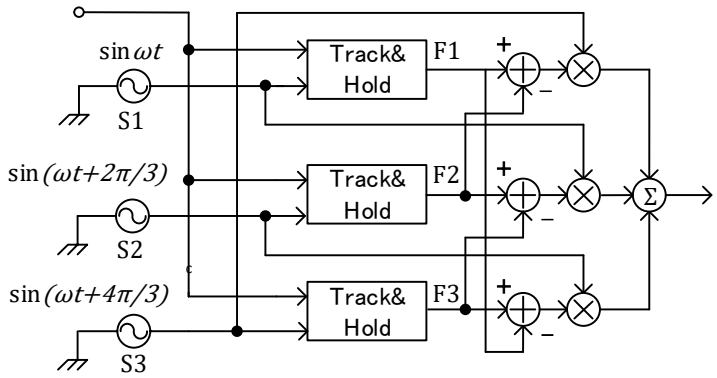
Configuration of N-stage Trigger Circuit



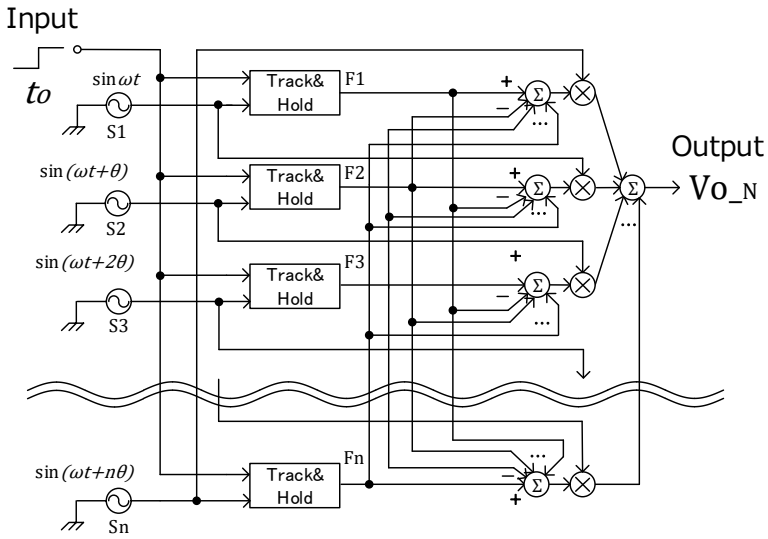
Consideration of N-stage Trigger Circuit



Output of three-stage

$$S_1(F_2 - F_3) + S_2(F_3 - F_1) + S_3(F_1 - F_2)$$

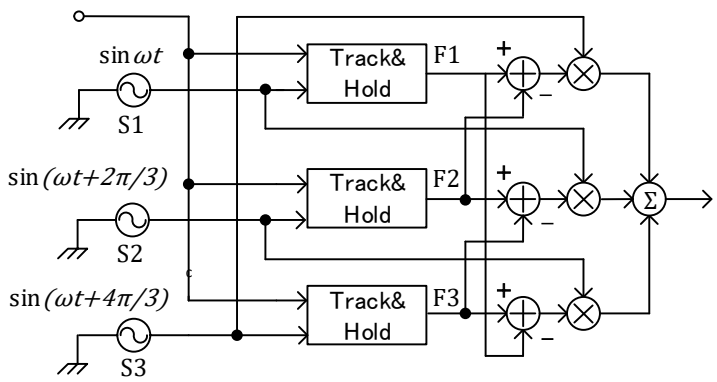
Same calculation



Extension to N-stage

$$\begin{aligned} &S_1(F_2 - F_3 - F_4 - \cdots - F_{N-1} - F_N) \\ &+S_2(F_3 - F_4 - F_5 - \cdots - F_N - F_1) \\ &+\cdots \\ &+S_N(F_1 - F_2 - \cdots - F_{N-2} - F_{N-1}) \end{aligned}$$

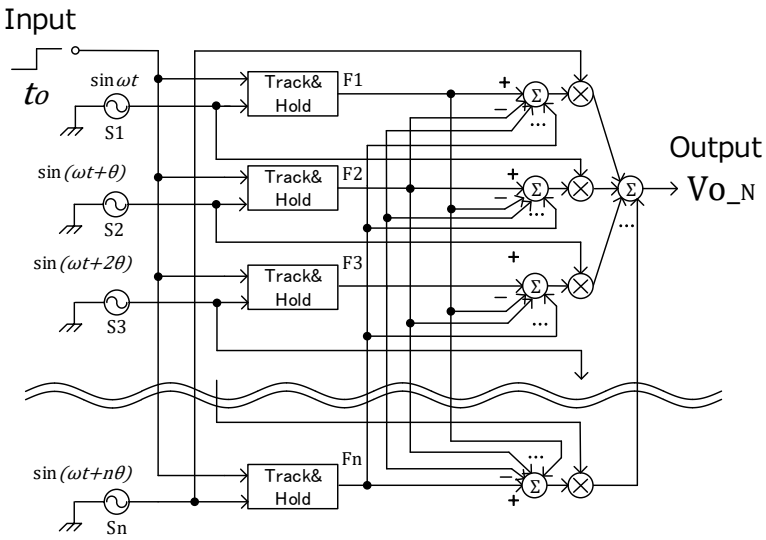
Consideration of N-stage Trigger Circuit



Signal source of three-stage

$$S_1 = \sin \omega t\,,\ S_2 = \sin\left(\omega t + \frac{2\pi}{3}\right),\ S_3 = \sin\left(\omega t + \frac{4\pi}{3}\right)$$

$$\theta_1 = 0 \qquad \theta_2 = \frac{2\pi}{3} \qquad \theta_3 = \frac{4\pi}{3}$$

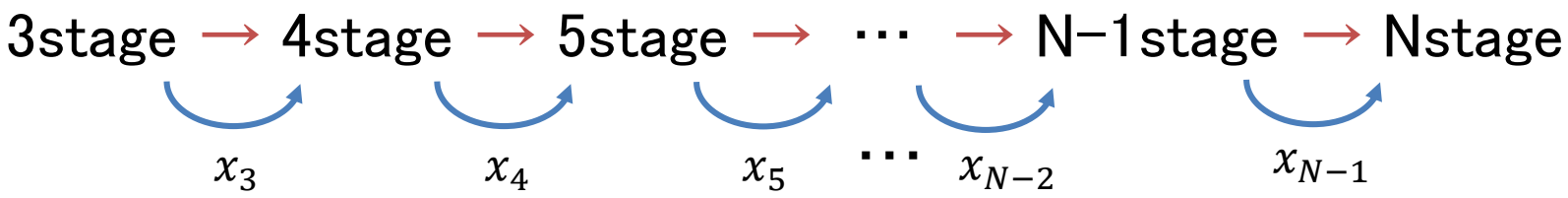


Signal source of N-stage

$$S_n = \sin(\omega t + (n-1)\theta)\,,\quad \theta = \frac{2\pi}{N}$$

Derivation of N-stage Output

Using difference sequence



Increment when increasing the stage number

$$x_k = V_{k+1} - V_k$$
$$= F_{k+1}\left(S_k - \sum_{l=1}^{k-1} S_l\right) - 2S_kF_1 + S_{k+1}\left(F_1 - \sum_{m=2}^{k-1} F_m\right)$$

N−stage Output

$$V_N = S_1F_2 + S_2F_1 + \sum_{k=2}^{N-1}\left[F_{k+1}\left(S_k - \sum_{l=1}^{k-1} S_l\right) - 2S_kF_1 + S_{k+1}\left(F_1 - \sum_{m=2}^{k-1} F_m\right)\right]$$

Confirmation of N-stage Output

Matching with Three-stage

$$V_{o\_N} = a_2 + \sum_{k=2}^{N-1}\left[F_{k+1}\left(S_k - \sum_{l=1}^{k-1} S_l\right) - 2S_kF_1 + S_{k+1}\left(F_1 - \sum_{m=2}^{k-1} F_m\right)\right]$$

$$V_{o\_3} = S_1F_2 + S_2F_1 + \sum_{k=2}^{2}\left[F_{k+1}\left(S_k - \sum_{l=1}^{1} S_l\right) - 2S_kF_1 + S_{k+1}\left(F_1 - \sum_{m=2}^{1} F_m\right)\right]$$

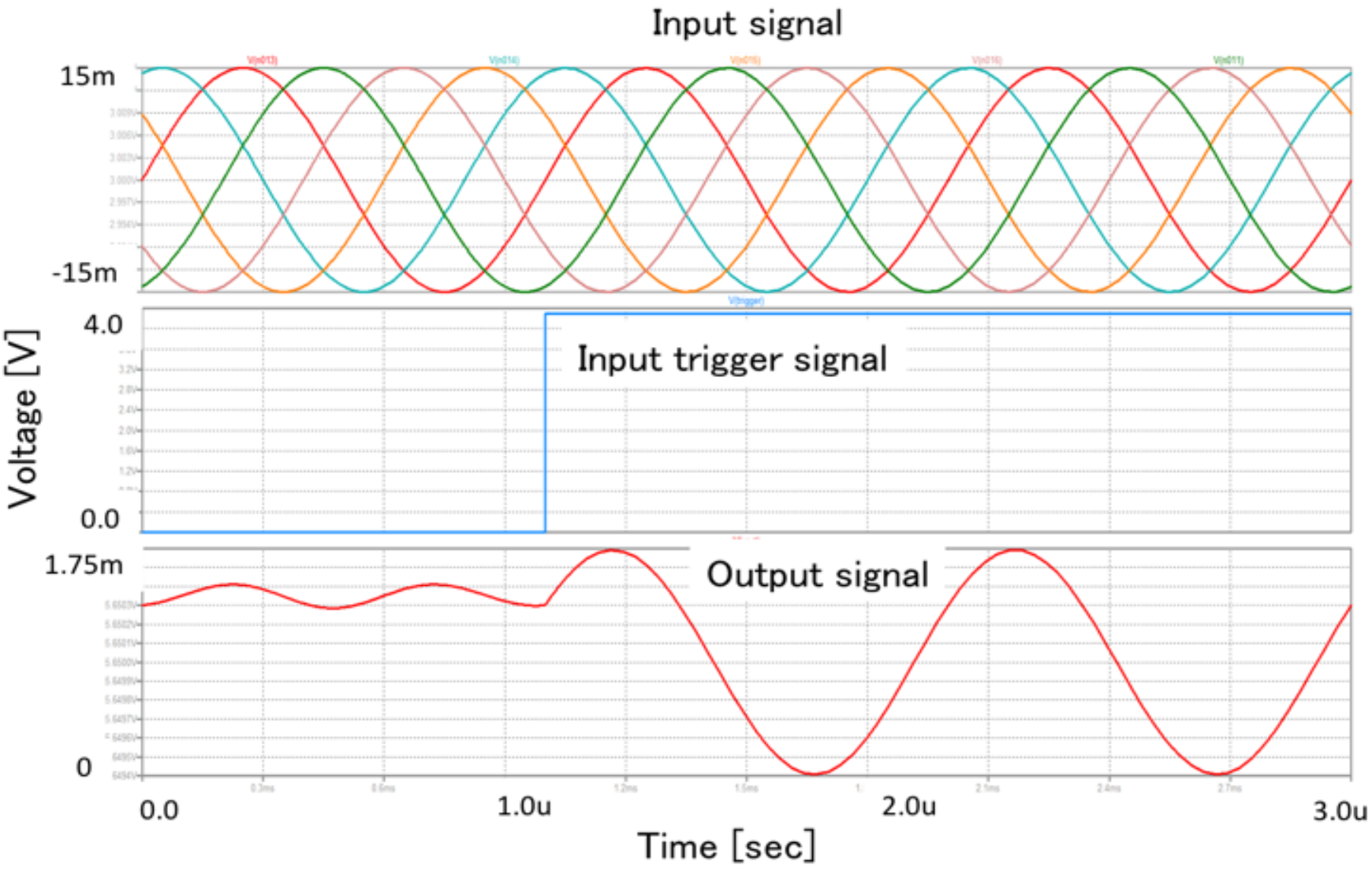
$$= S_1F_2 + S_2F_1 + [F_3(S_2 - S_1) - 2S_2F_1 + S_3(F_1 - F_2)]$$

$$= S_1(F_2 - F_3) + S_2(F_3 - F_1) + S_3(F_1 - F_2)$$

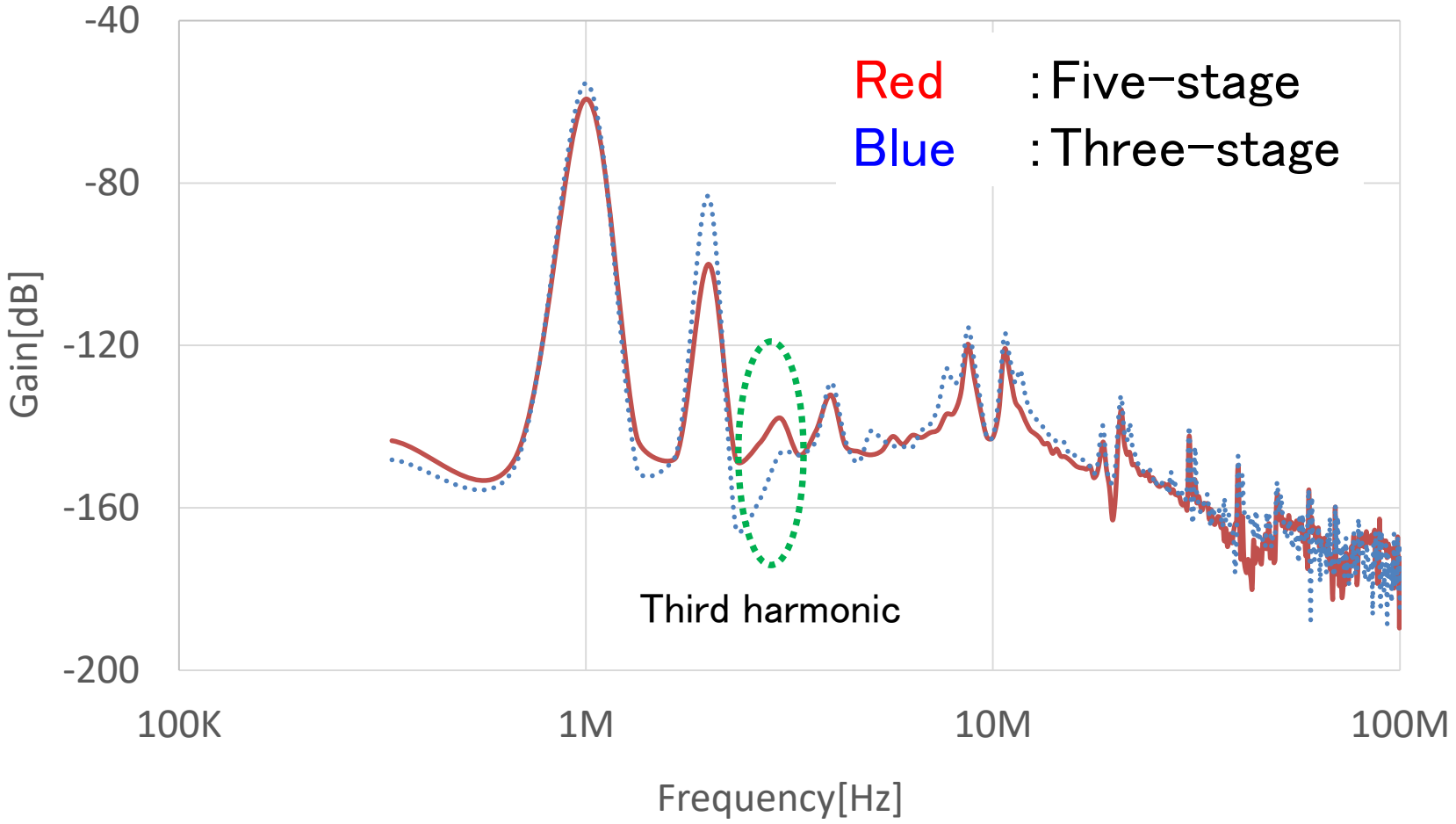
$$V_{o\_3} = S_1(F_2 - F_3) + S_2(F_3 - F_1) + S_3(F_1 - F_2)$$

Match

Output of Five-stage Trigger Circuit



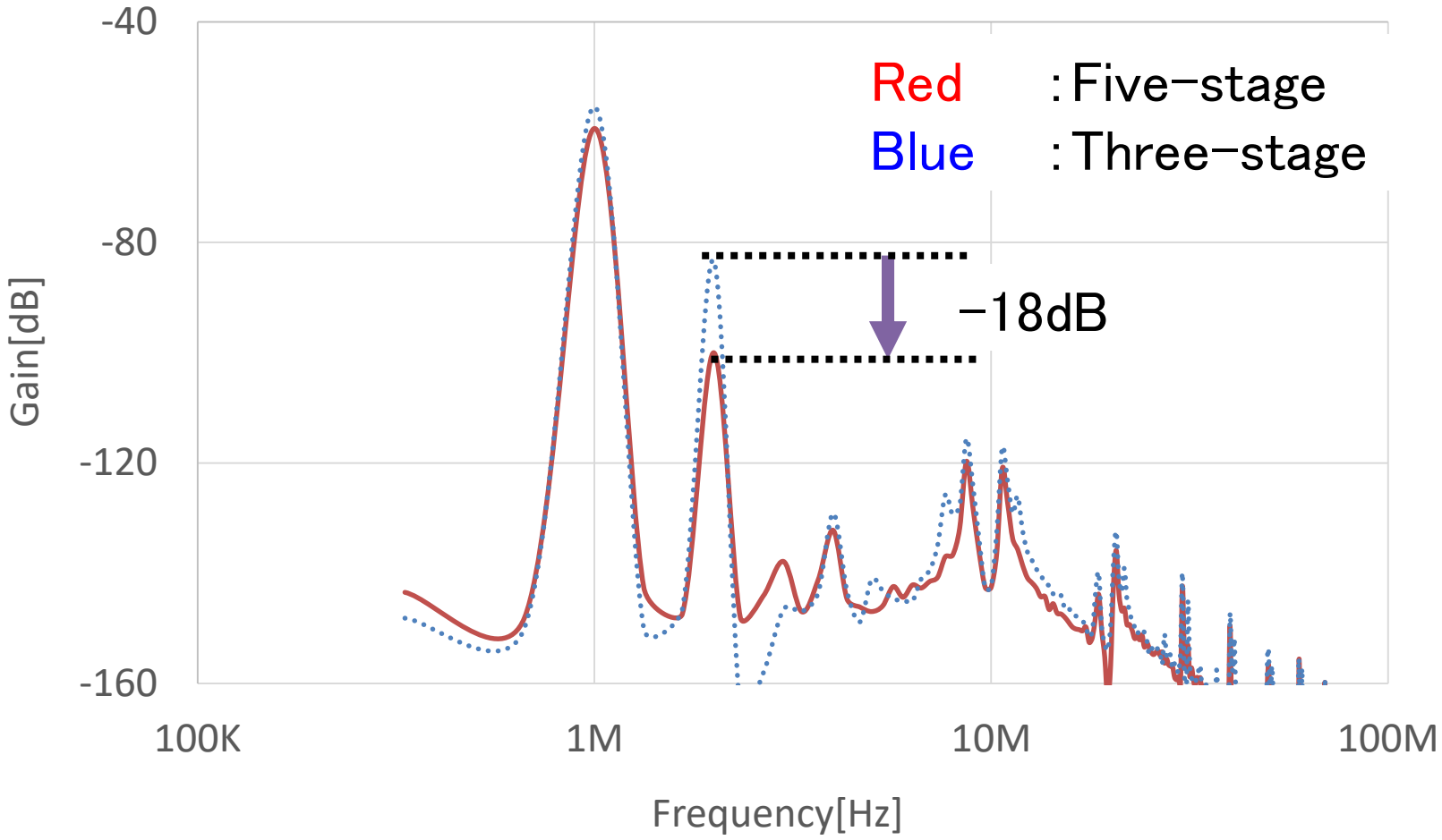
Output Spectrum Comparison



Third harmonic cancellation

Second harmonic reduction by 30%

Multistage Configuration Merit



Third harmonic cancellation

Second harmonic reduction by 30%

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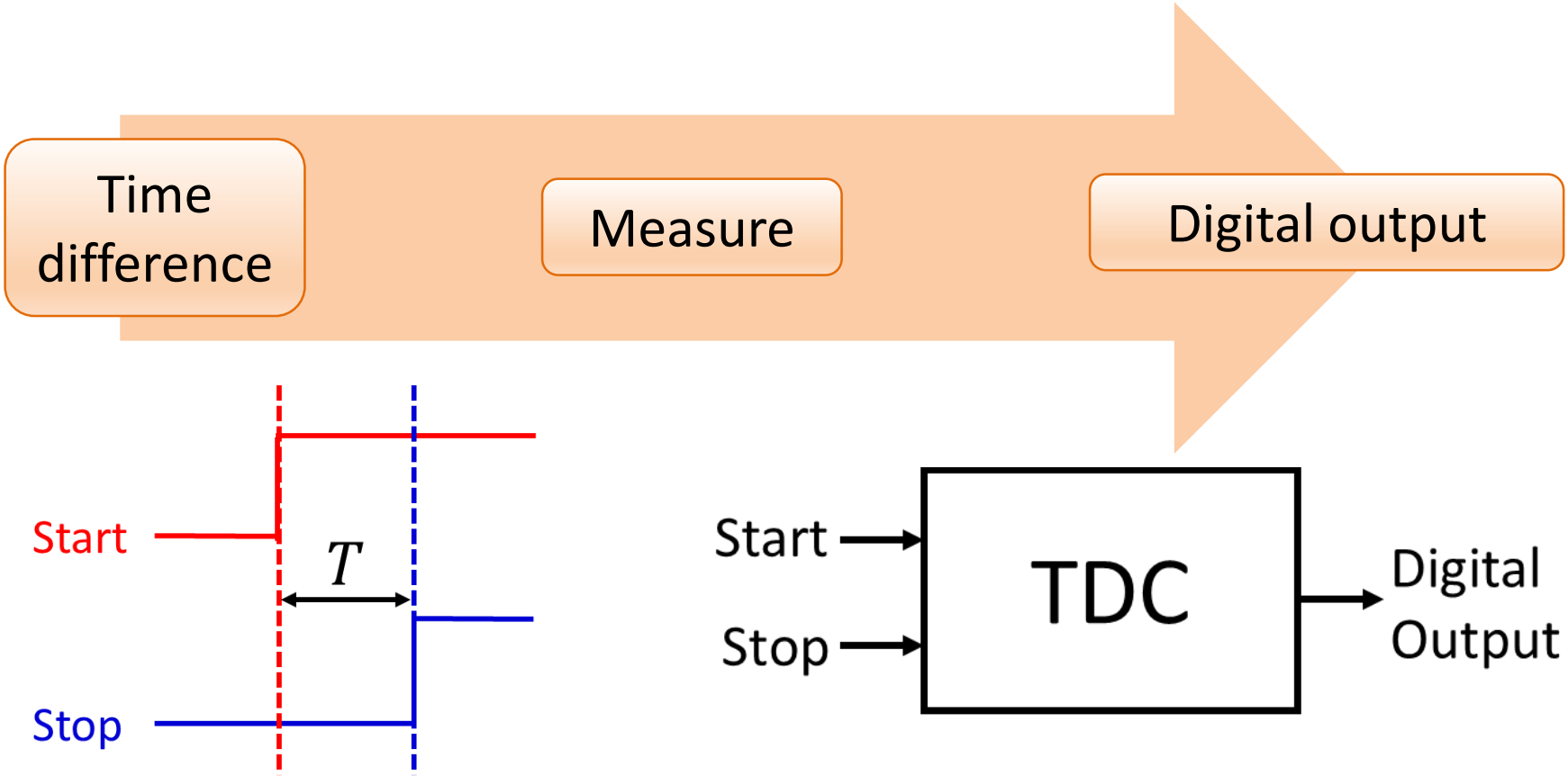
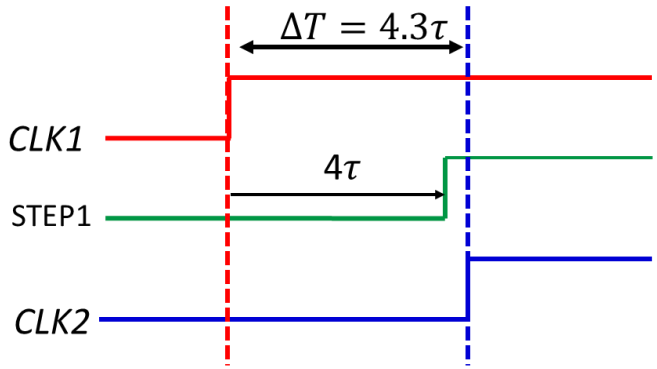
Time Digitizer Circuit

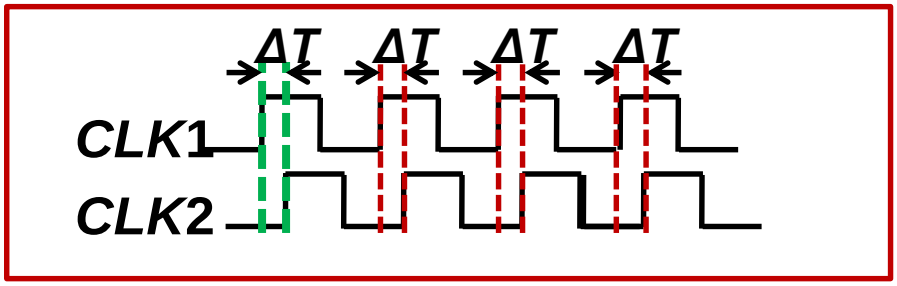


Time-to-Digital Converter (TDC)

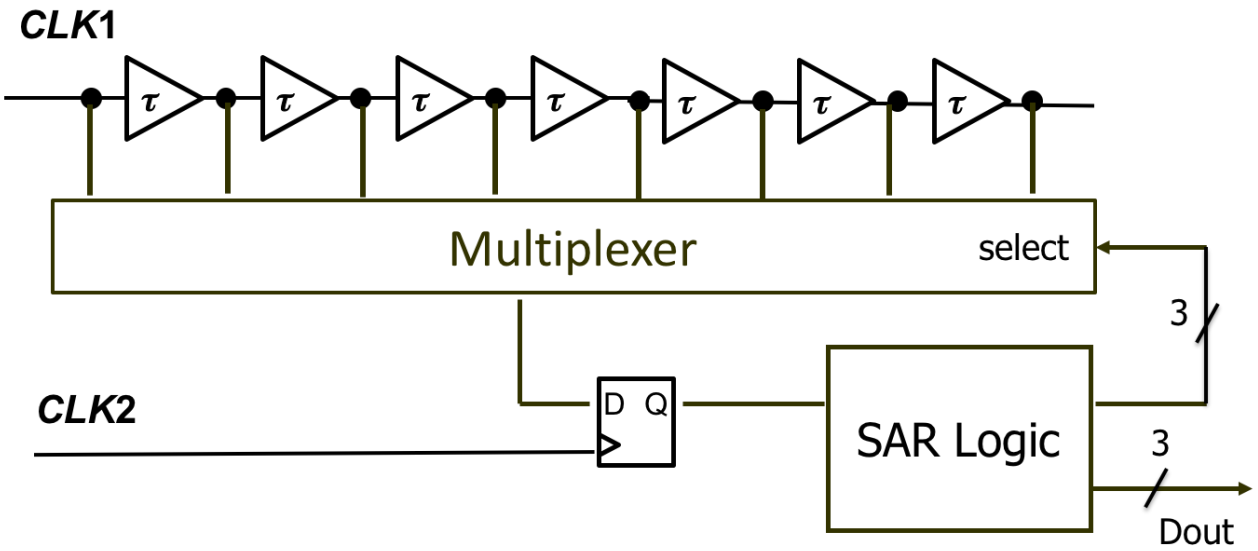
Measure time difference between Start and Stop signals.

SAR-TDC Configuration





Need cycle clock for measurement



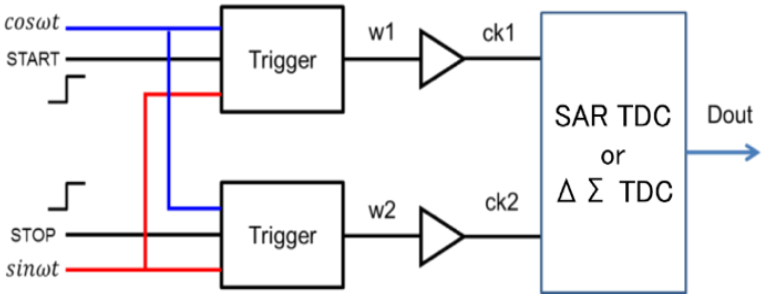
Reference[5]
Y. Ozawa, T. Ida, S. Sakurai, R. Jiang, H. Kobayashi, R. Shiota, “SAR ADC Architecture for One-Shot Timing Measurement with Full Digital Implementation,”

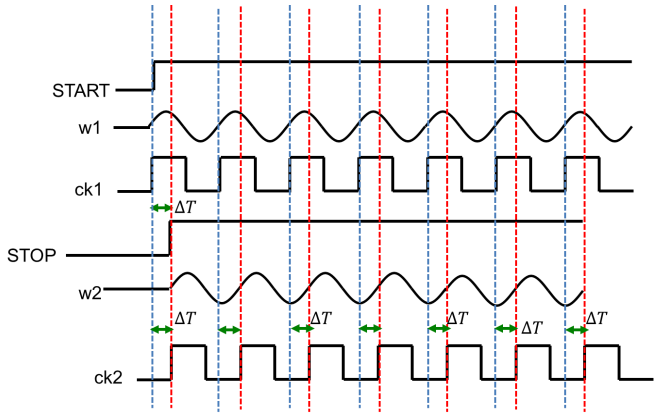
Problem of SAR-TDC and Remedy

Myth

Voltage signal can be held.

Timing signal cannot be held.





Our argument

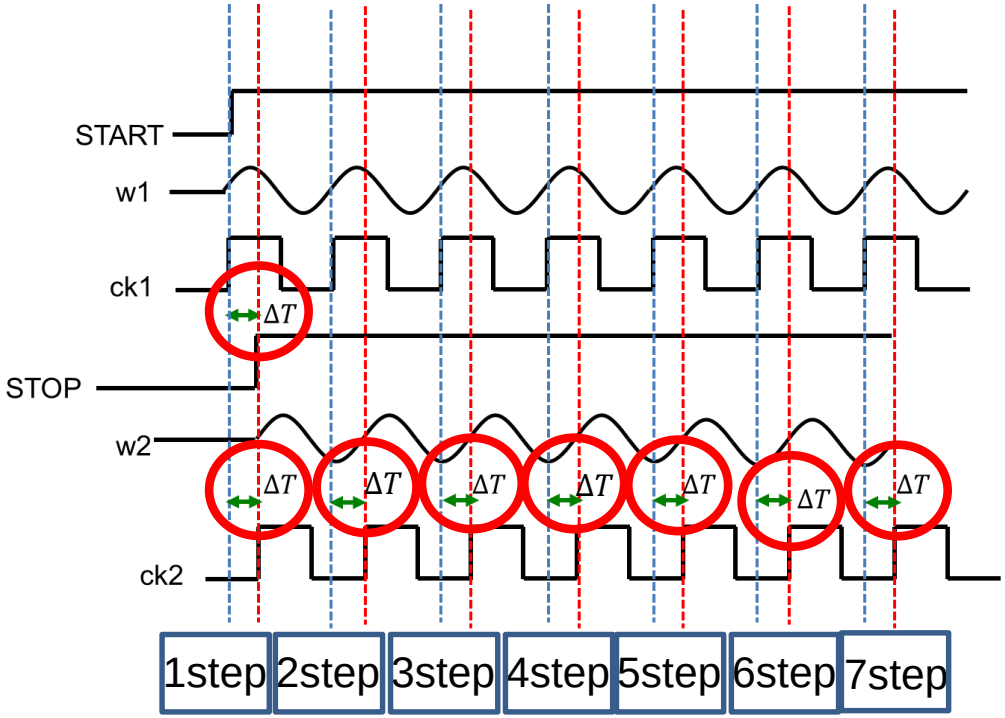
Timing signal can be held !

One-shot Timing Measurement Using Trigger Circuit

Suggestion

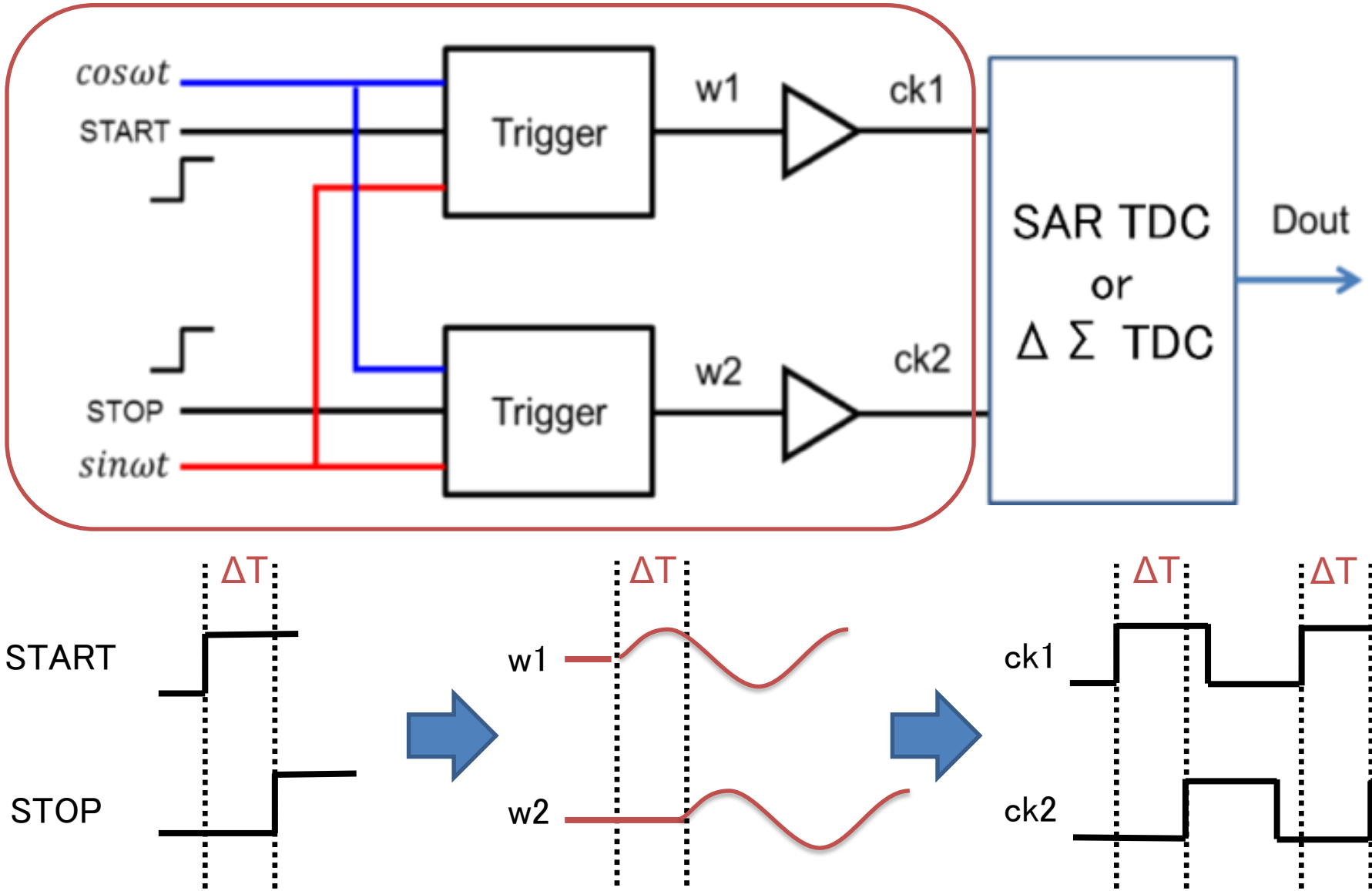
Input START,STOP signal

Oscillate with initial phase at input timing

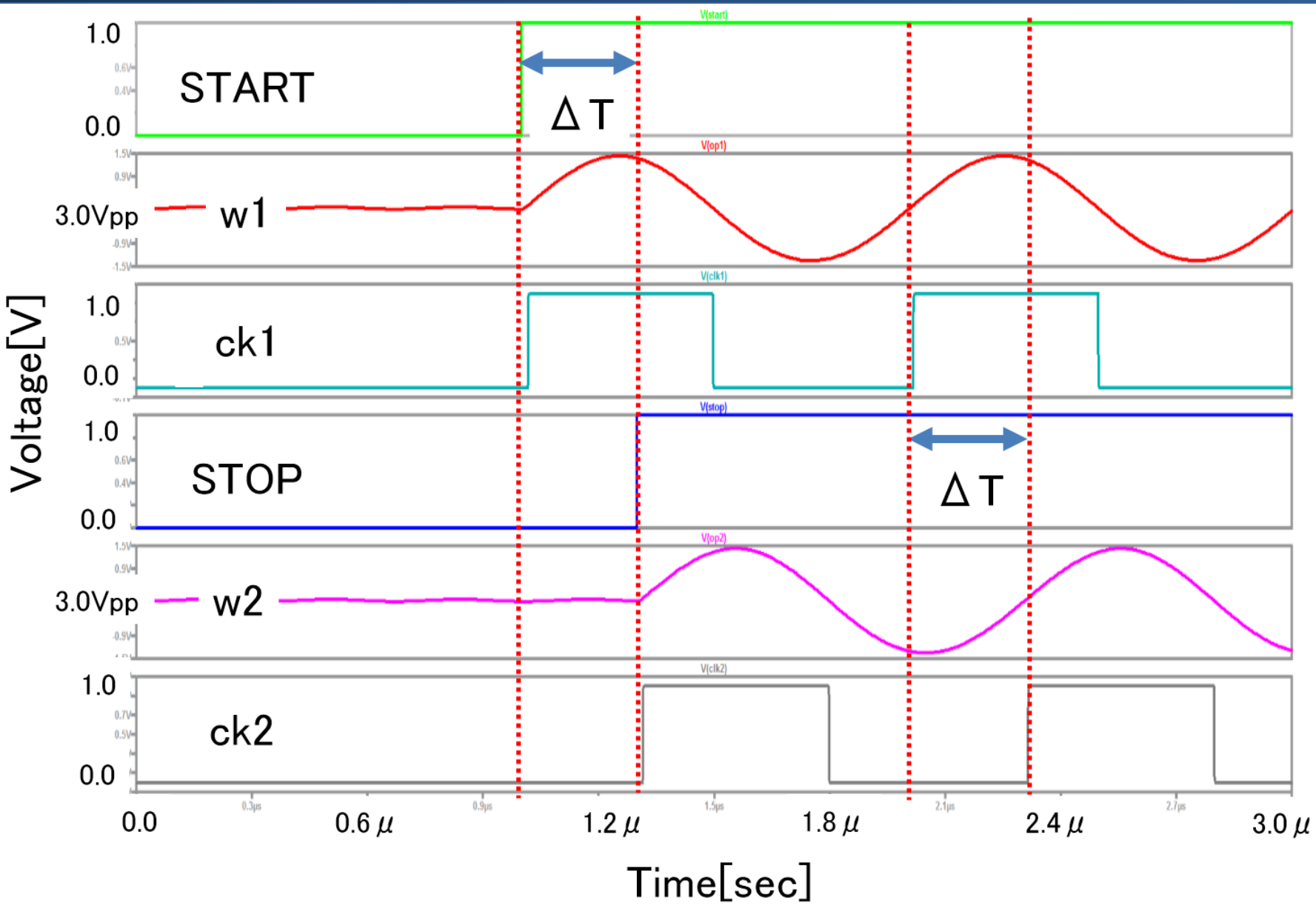


It can hold the time difference using two trigger circuits.

One-shot Timing Measurement Configuration



One-Shot Timing Measurement Simulation



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Summary

- Investigation of CMOS trigger circuit

- Extension to N-stage trigger circuit, and its confirmation with SPICE simulated sinusoidal output power spectrum.

  ⇒ Harmonics reduction

- Proposal of one-shot timing measurement with trigger circuits and SAR-TDC.

Future works

- Harmonics suppression analysis based on derived formula.
- Circuit configuration that reduces Gilbert cell nonlinearity
- Implementation consideration including SAR-TDC.

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Back Up