



# IEEE International Symposium on Intelligent Signal Processing and Communication Systems 2017

NOVEMBER 6-9, 2017, XIAMEN, CHINA



Nov. 9 NA-L2 8:30-9:50

## Gray-Code Input DAC Architecture for Clean Signal Generation

Richen.Jiang, G.Adhikari, Yifei.Sun, Dan.Yao,  
R.Takahashi, Y.Ozawa, N.Tsukiji, H.Kobayashi, R.Shiota  
*Gunma University, Socionext Inc.,*



# OUTLINE

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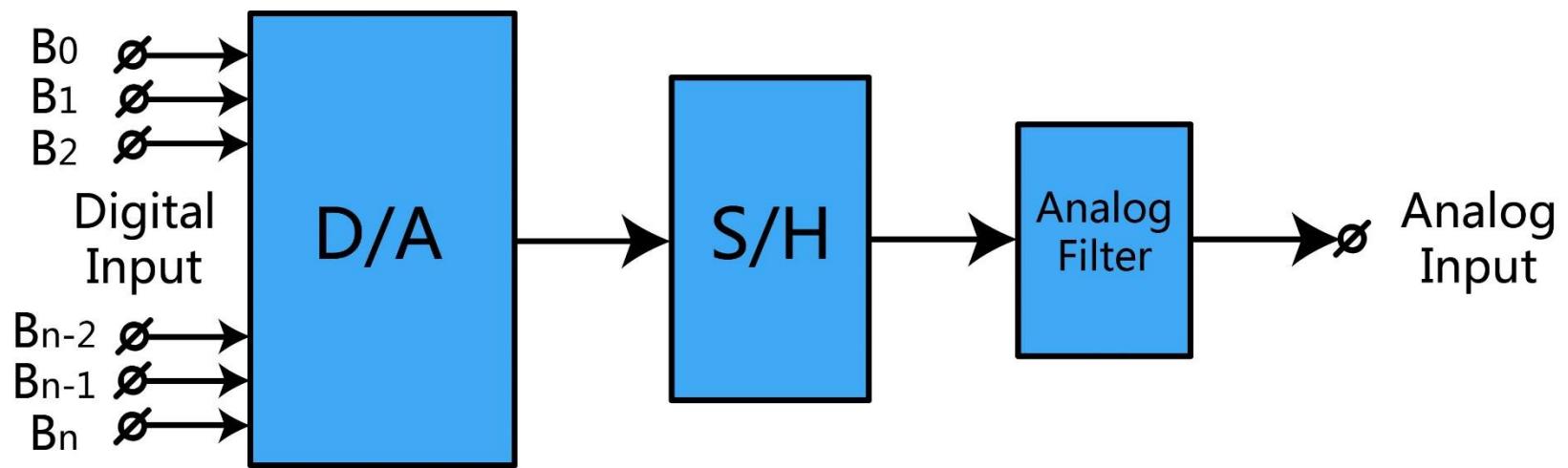
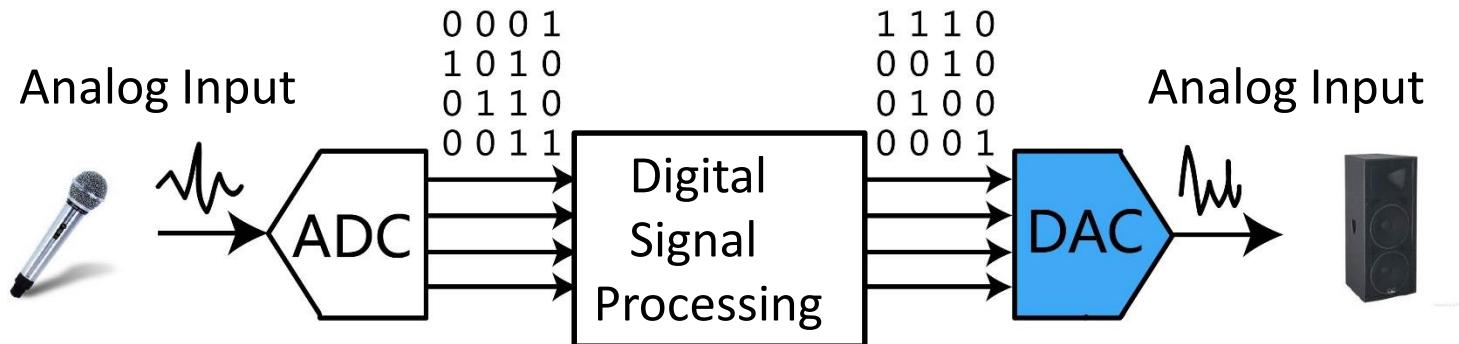
- Research Background • Objective
- Glitches
- Gray-code
- Gray-code Input DAC Architecture and Operation
- Simulation Verification by SPICE
- Conclusion

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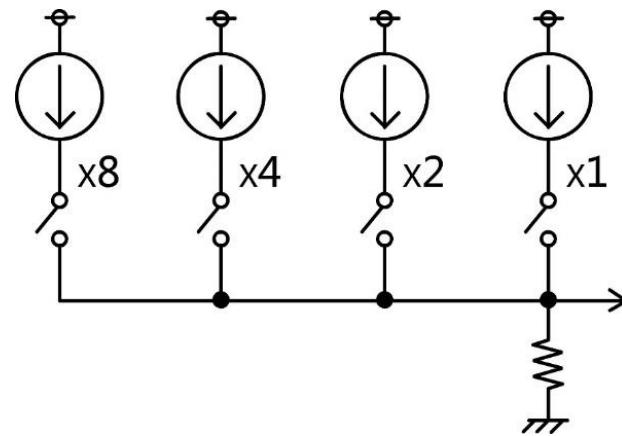
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# Research Background

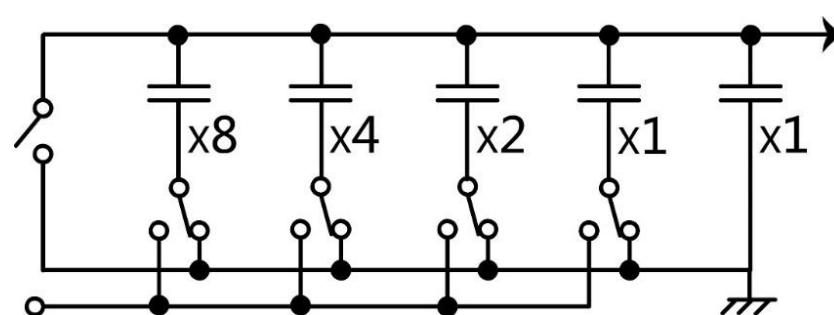


# Research Background

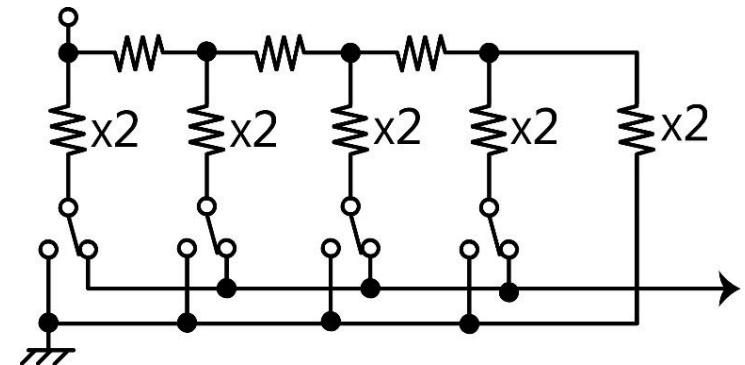
## Basic architecture of DAC



Current Source DAC



Capacitive DAC



Resistance DAC

The switch is driven with a binary code → glitch

# Research Objective

## Objective

- Design Digital-to-Analog Converter (DAC) architectures for clean signal generation

## Approach

- By reducing glitches with Gray-Code input topologies

# OUTLINE

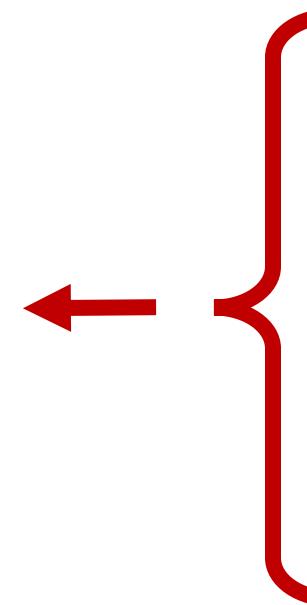
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# What are Glitches

- Voltage spikes
- Reasons for glitches

Decimal numbers	Natural Binary code
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1
10	1 0 1 0
11	1 0 1 1
12	1 1 0 0
13	1 1 0 1
14	1 1 1 0
15	1 1 1 1

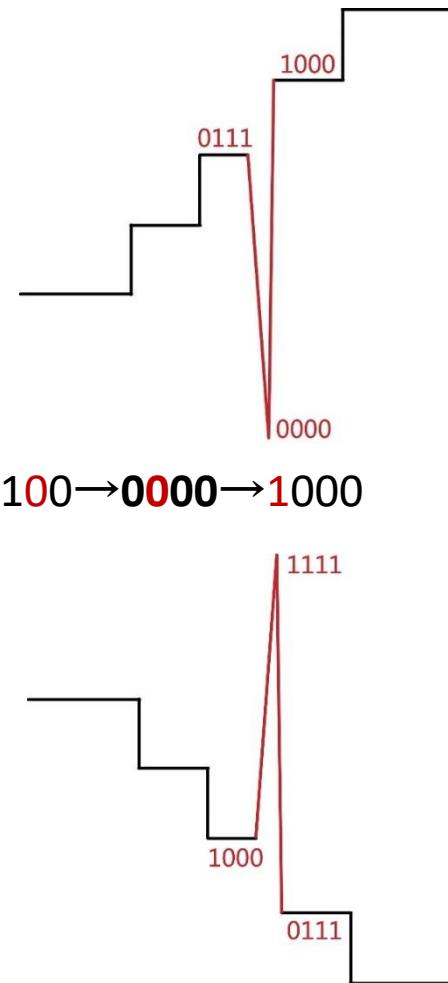


when  
7 → 8

0111 → 0110 → 0100 → 0000 → 1000

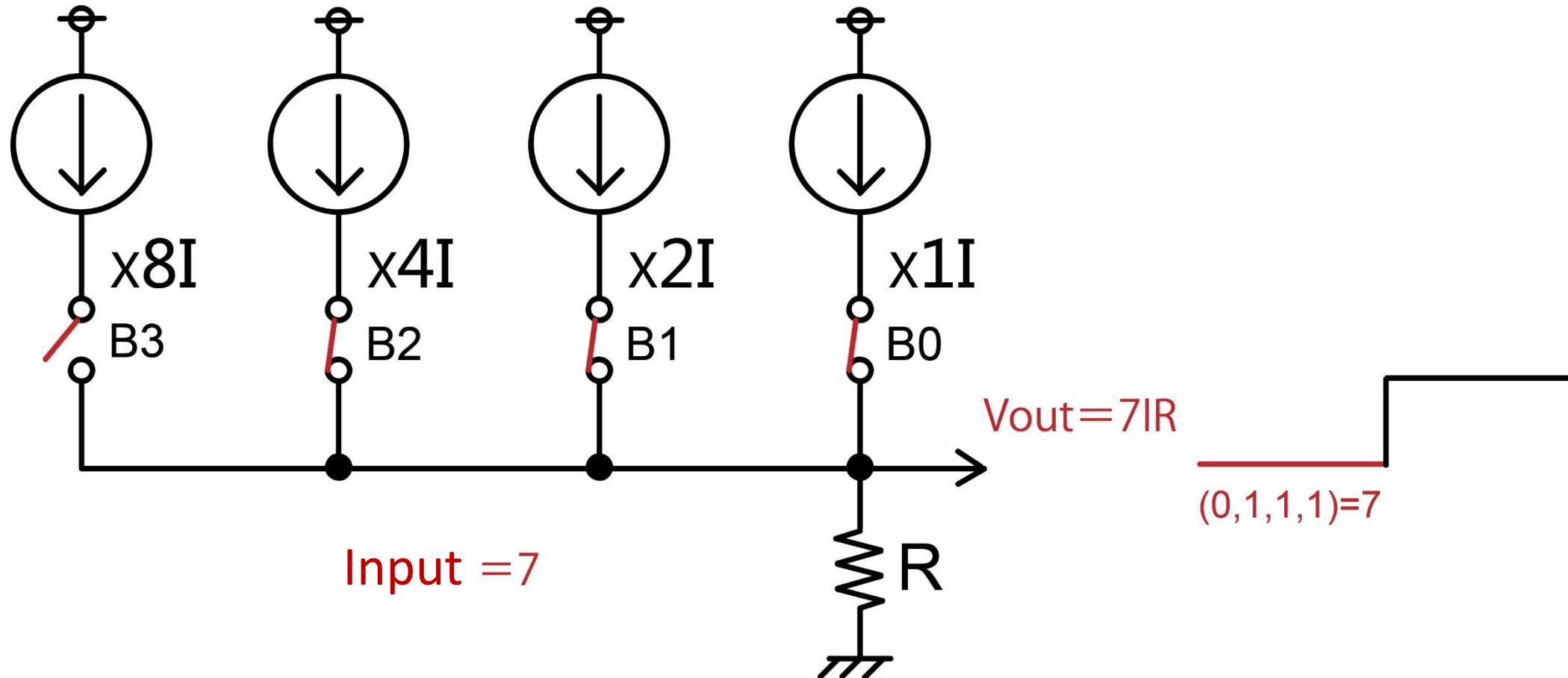
when  
8 → 7

1000 → 1001 → 1011 → 1111 → 0111



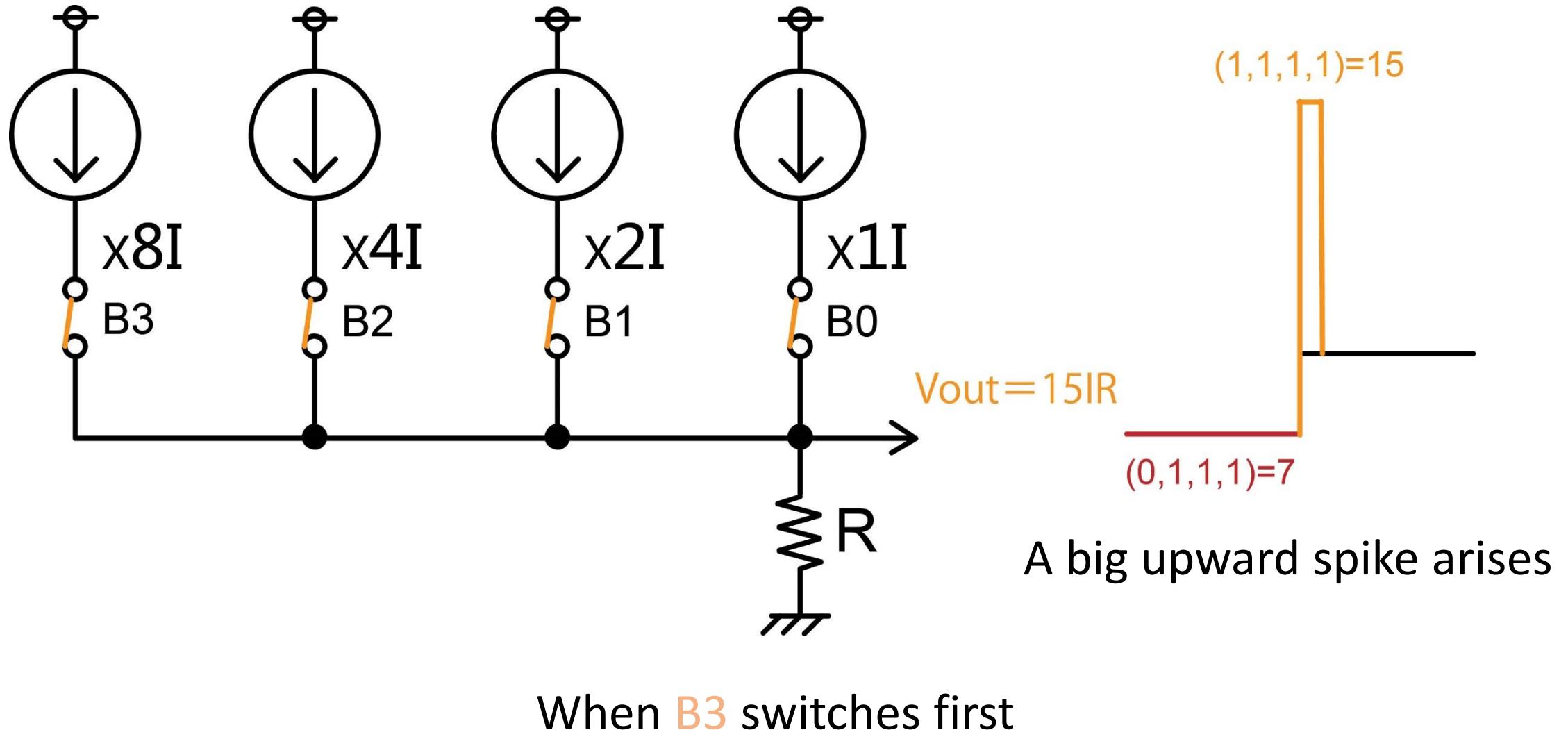
The most significant bit (MSB) changes (near the middle point)

# Generation of Glitch at Switching time

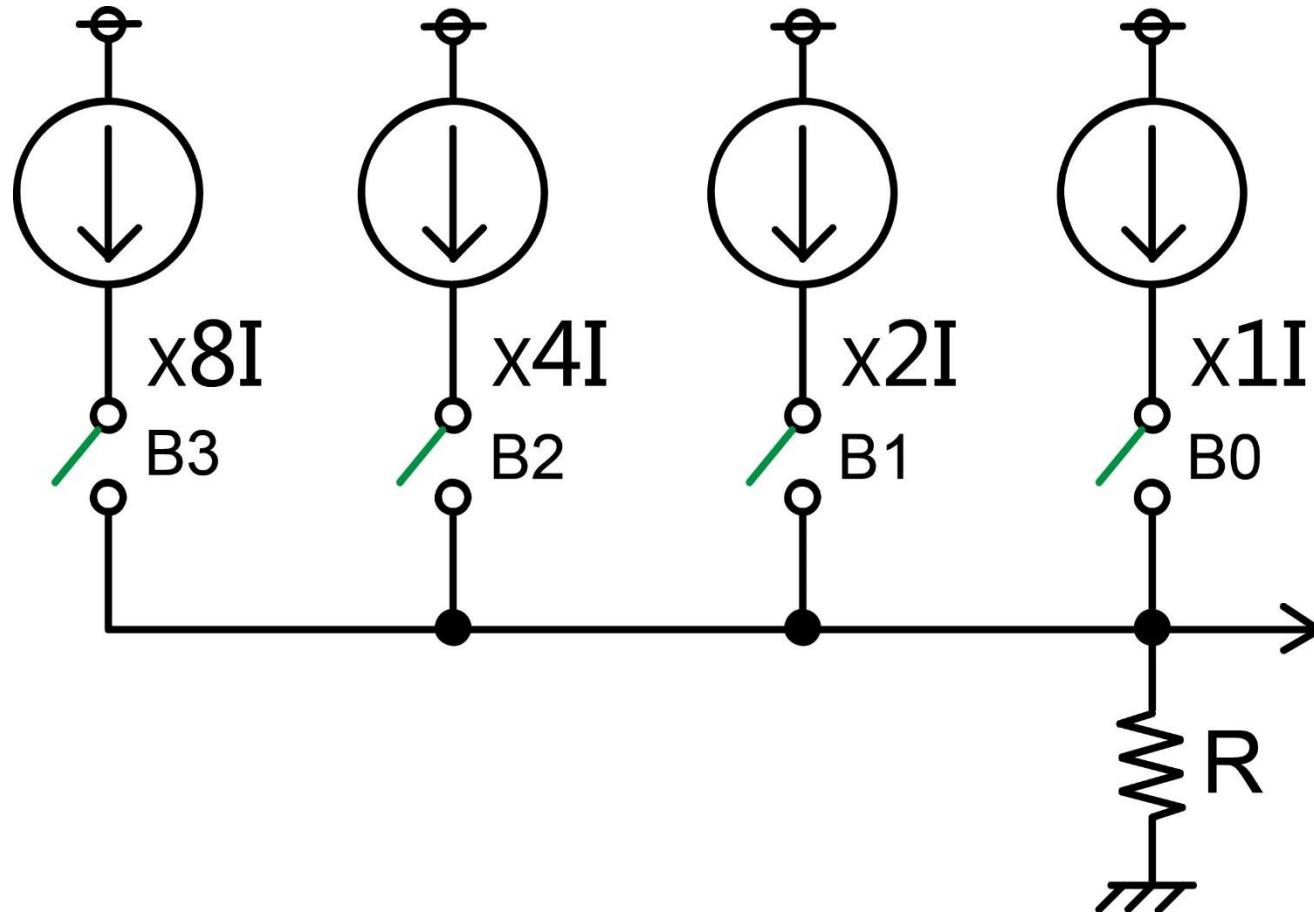


When the input changes  $7 \rightarrow 8$

# Generation of Glitch at Switching time

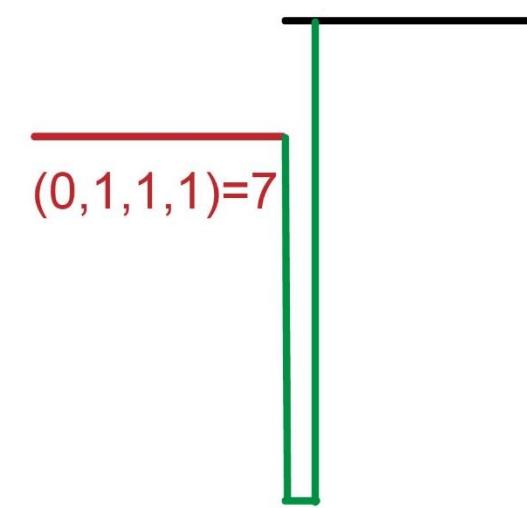


# Generation of Glitch at Switching time

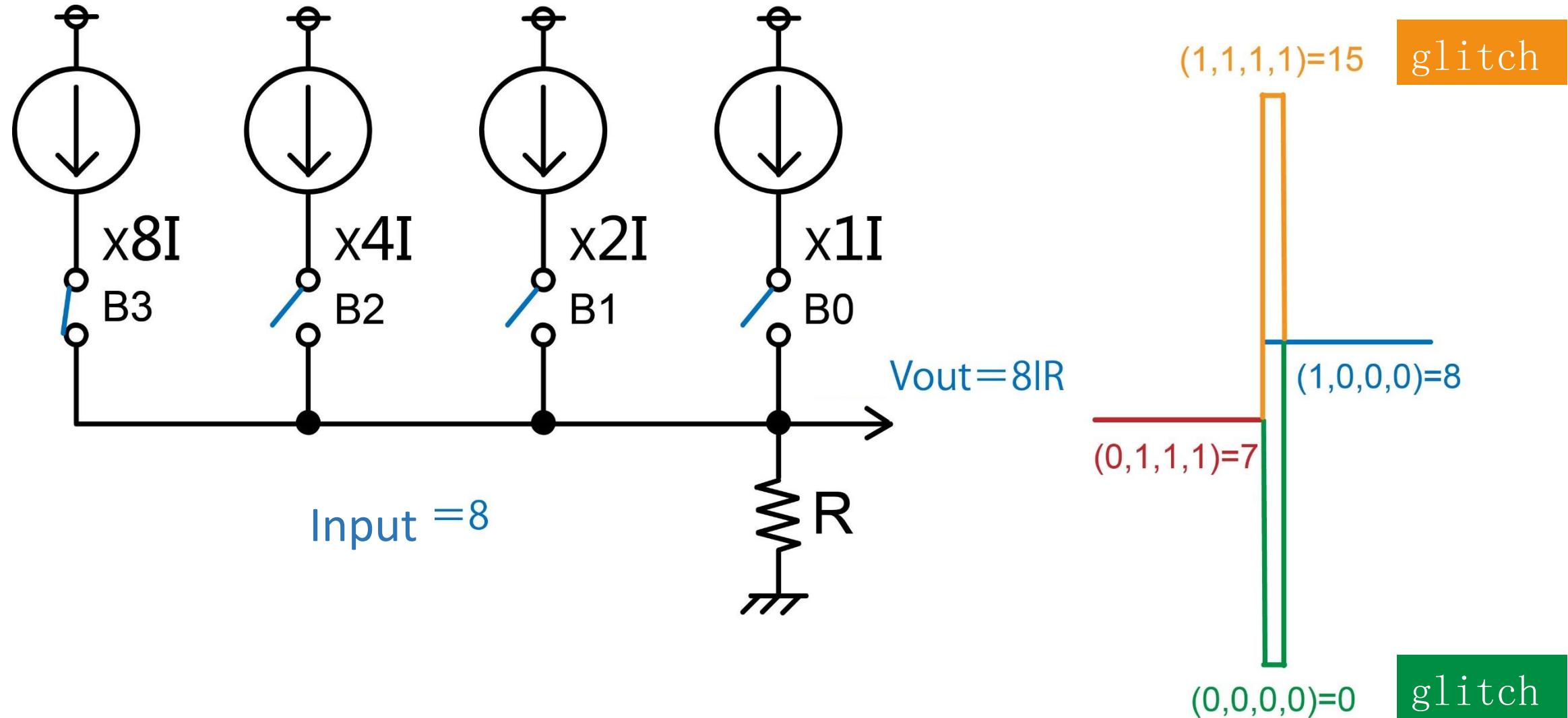


When  $B_3$  switches last

A big downward spike occur



# Generation of Glitch at Switching time



# Glitch Problem and Remedy

## Effects of Glitch

- Serious deterioration of images, videos, sounds



## Remedy

- Using high-order reconstruction filter
- Using track/hold circuitry at the DAC output
- **Using Gray-Code input DAC topologies**

} Extra Space in IC,  
Expensive



# OUTLINE

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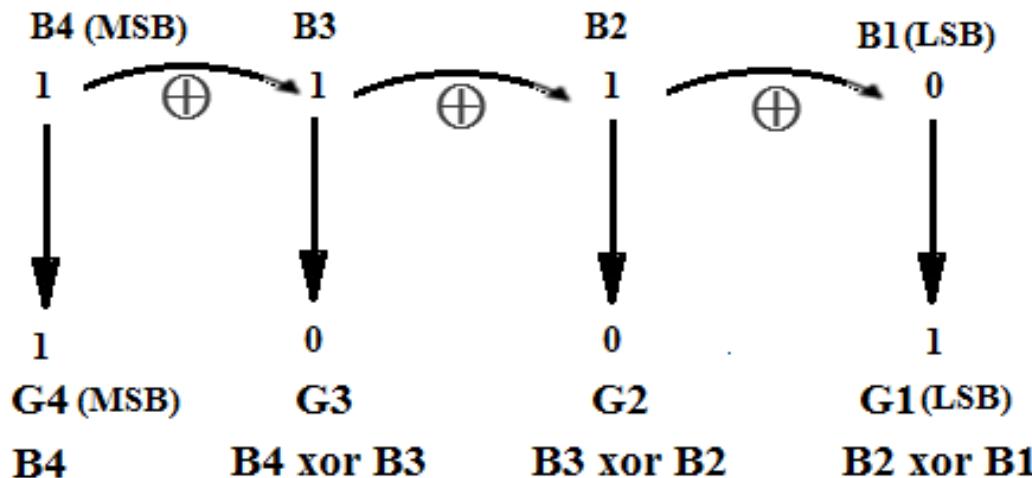
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# Gray-Code

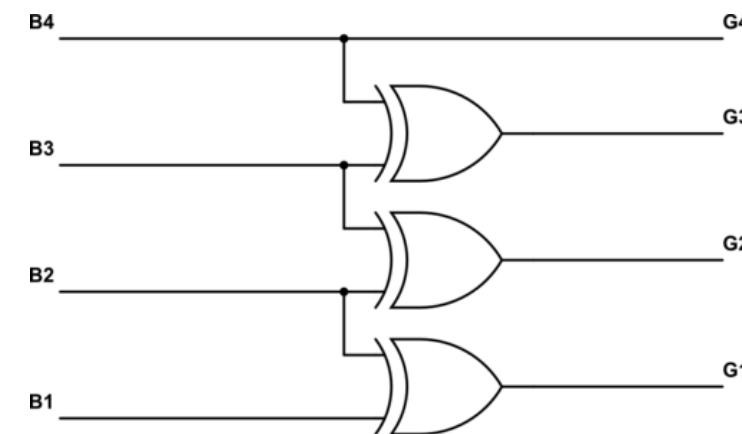
Gray-Code → Alternative representation of binary code

Two adjacent number → Only one bit change

$$(G_n = B_{n+1} \oplus B_n)$$



Binary to Gray code conversion diagram



Binary to Gray code converter

# Gray Code

Compare with **Binary code** and **Gray code**

Decimal numbers	Binary Code	Gray Code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

**Binary code**    Multiple bits change at a time  
                     Trigger more switches  
          Example.  $1 \rightarrow 2 \rightarrow 0001 \rightarrow 0010$     2 bits change  
                      $7 \rightarrow 8 \rightarrow 0111 \rightarrow 1000$     all 4 bits change

**Gray code**    Only one bit changes at a time  
                     Triggers one switch  
          Example.  $1 \rightarrow 2 \rightarrow 0001 \rightarrow 0011$  one bit change  
                      $7 \rightarrow 8 \rightarrow 0100 \rightarrow 1100$     one bit change

**Less glitches**

# OUTLINE

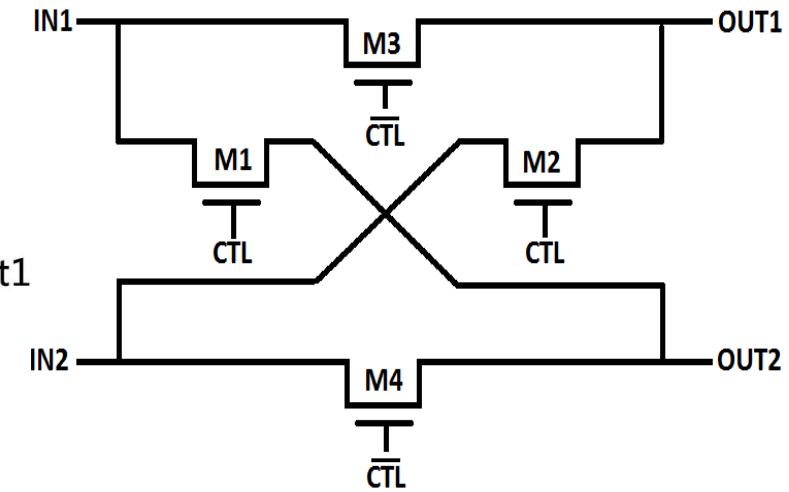
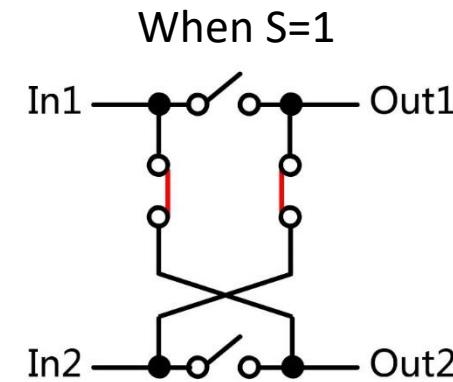
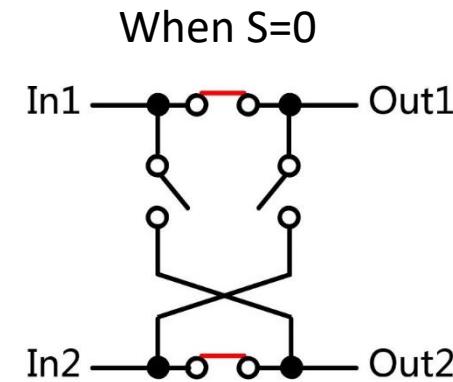
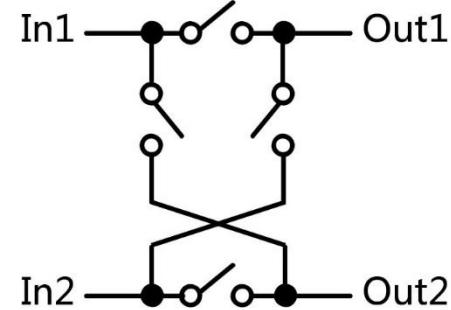
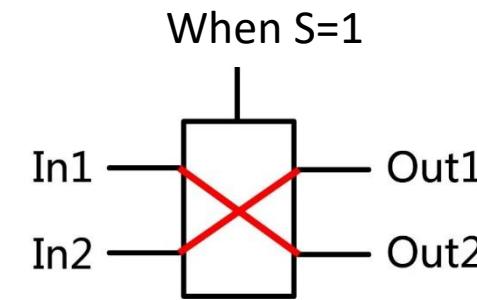
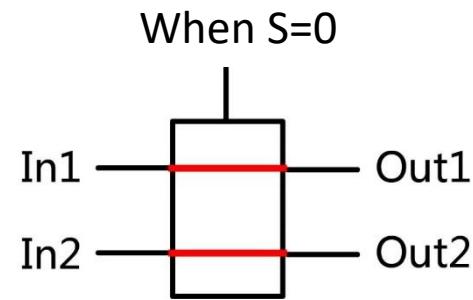
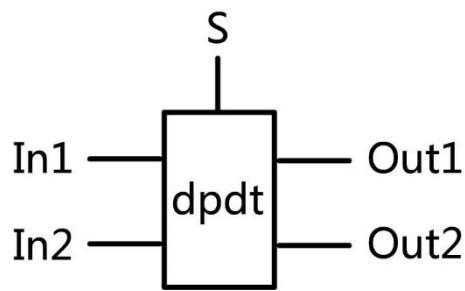
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# Gray-code Input DAC Architecture and Operation

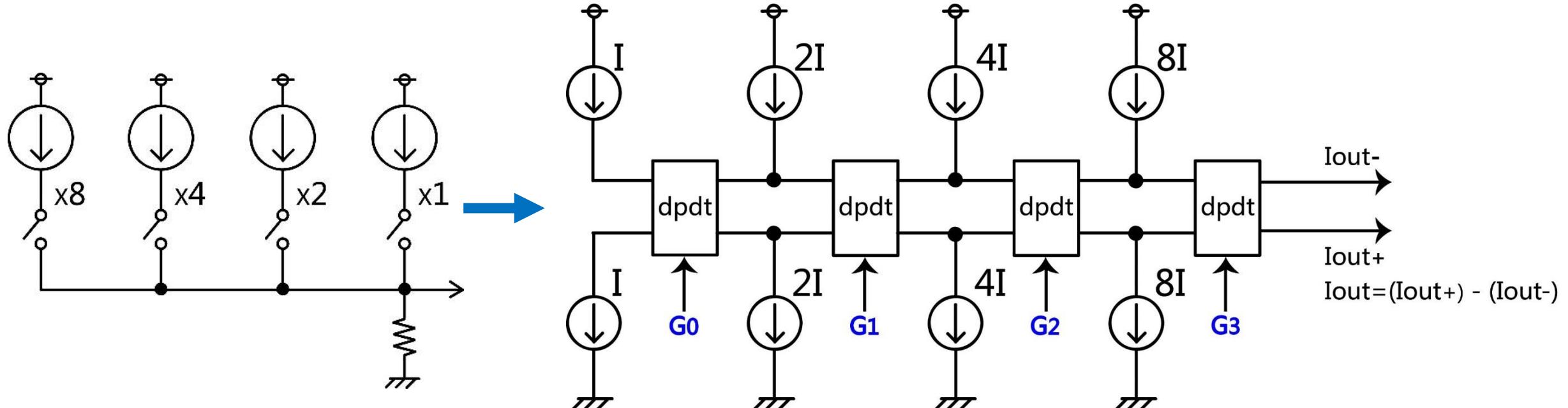
- 1.Current-steering Gray-Code DAC
- 2.Charge-mode Gray-Code DAC
- 3.Voltage-mode Gray-Code DAC

# Current/Voltage Switch Matrix



Switch is DPDT (**Double-Pole Double-Throw**)

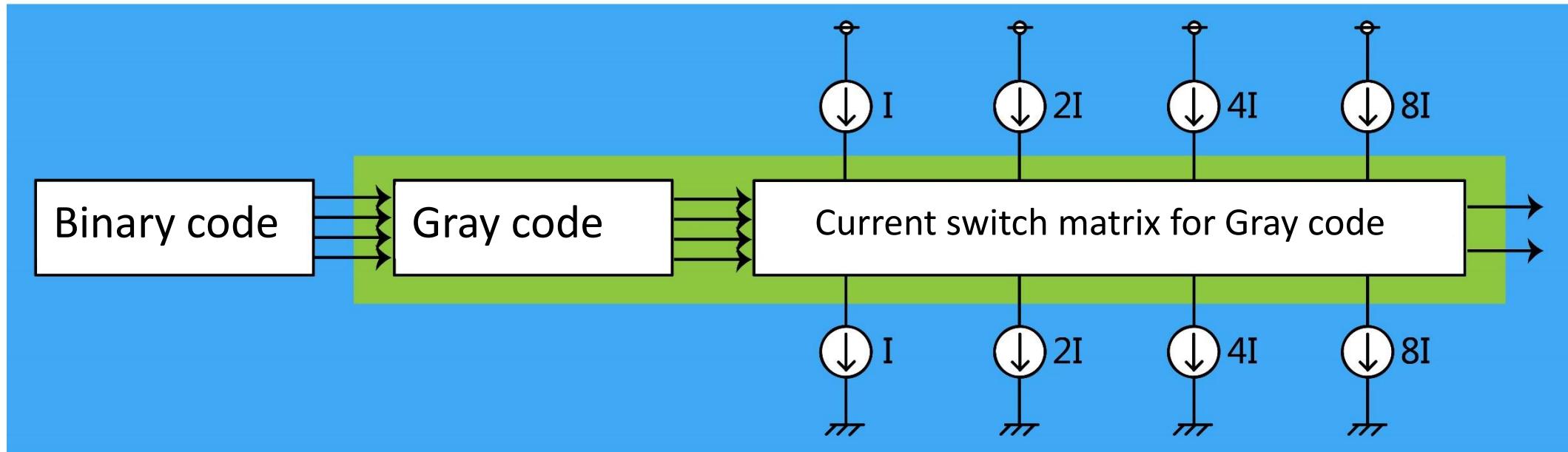
# 1. Current-steering Gray-Code DAC



Conventional Binary-Weighted  
current-steering DAC

Gray-Code input current-steering DAC

# Code Conversion

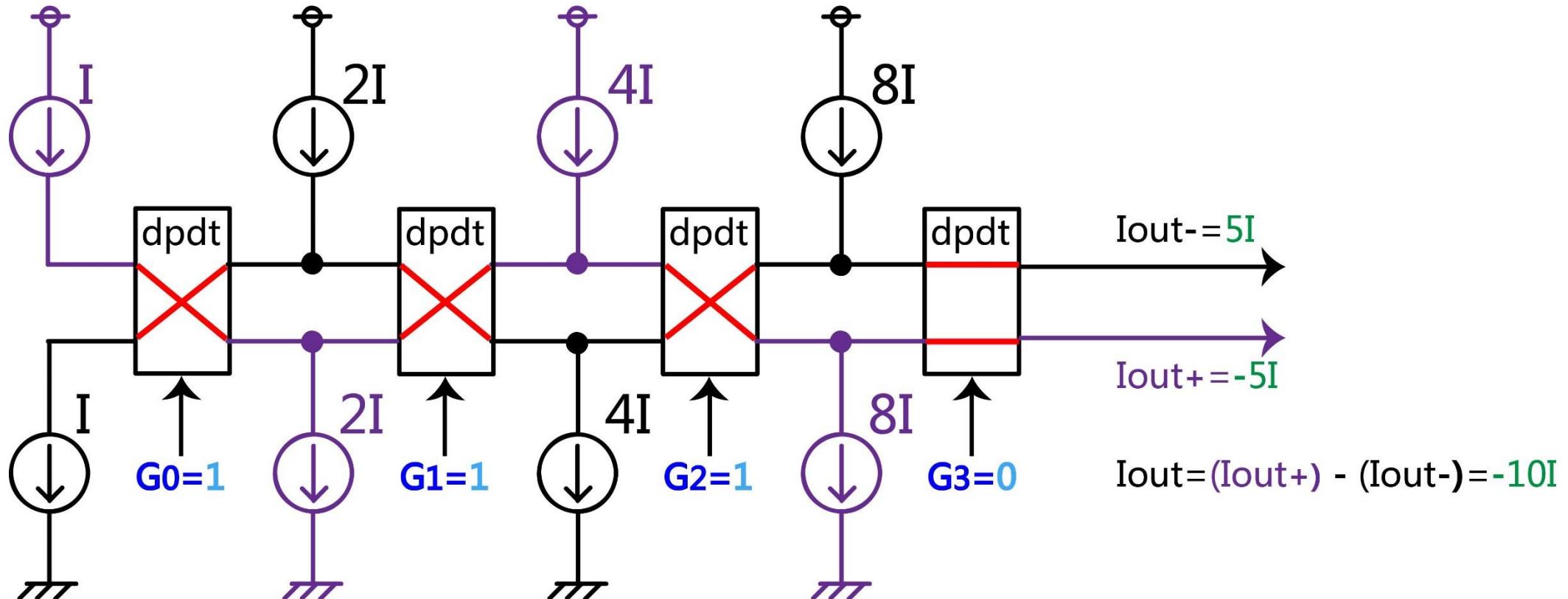


■ Binary code domain ■ Gray code domain

Code domain in Gray-code input current-steering DAC

# A Gray-code input current-steering DAC (data=5)

Data=5

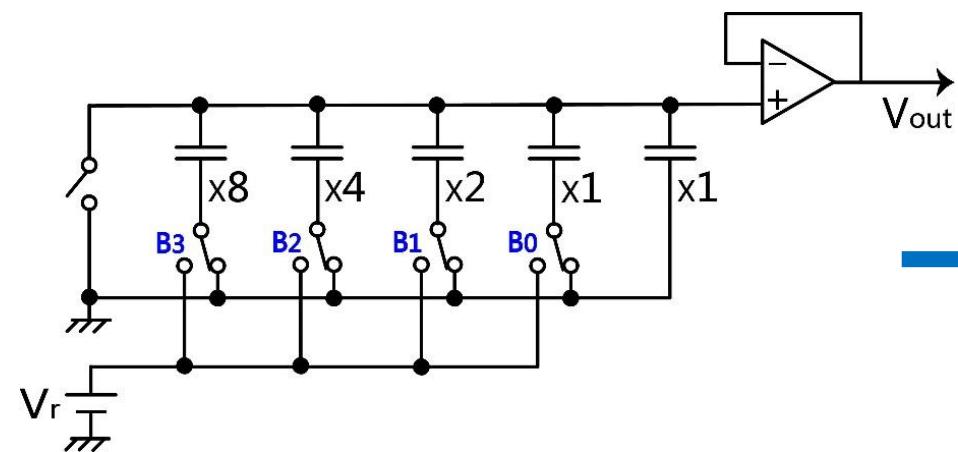


$$I_{out-} = -I + 2I - 4I + 8I = 5I$$

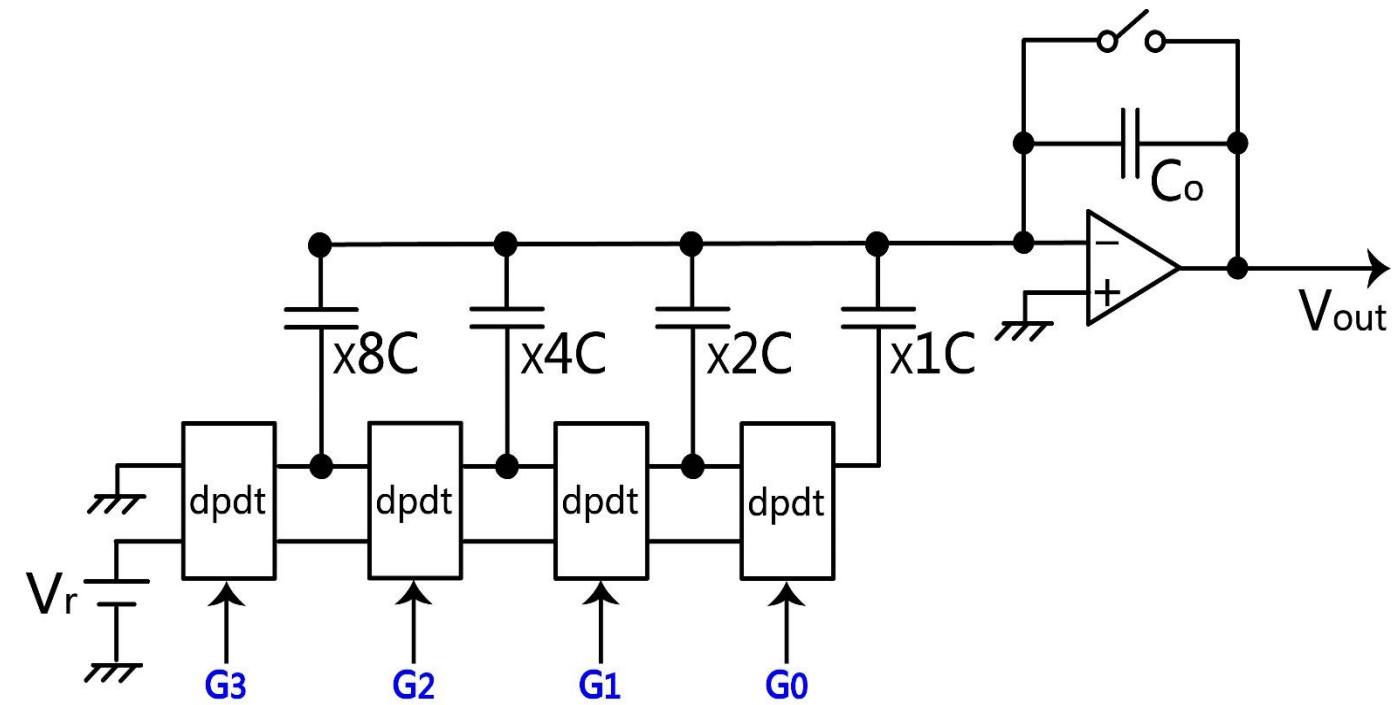
$$I_{out+} = I - 2I + 4I - 8I = -5I$$

$$I_{out} = (I_{out+}) - (I_{out-}) = -10I$$

## 2. Charge-mode Gray-code DAC

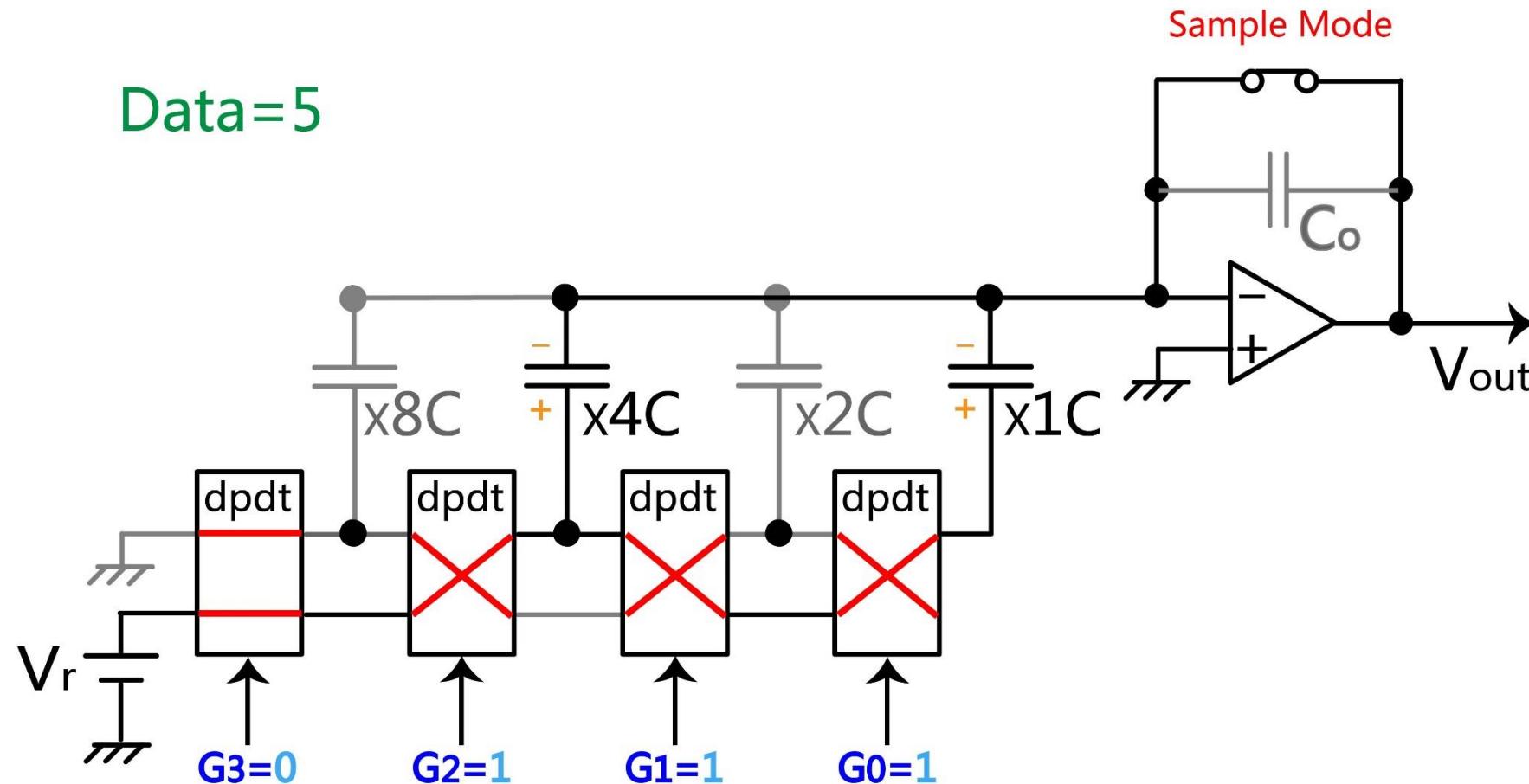


A binary-weighted capacitor DAC

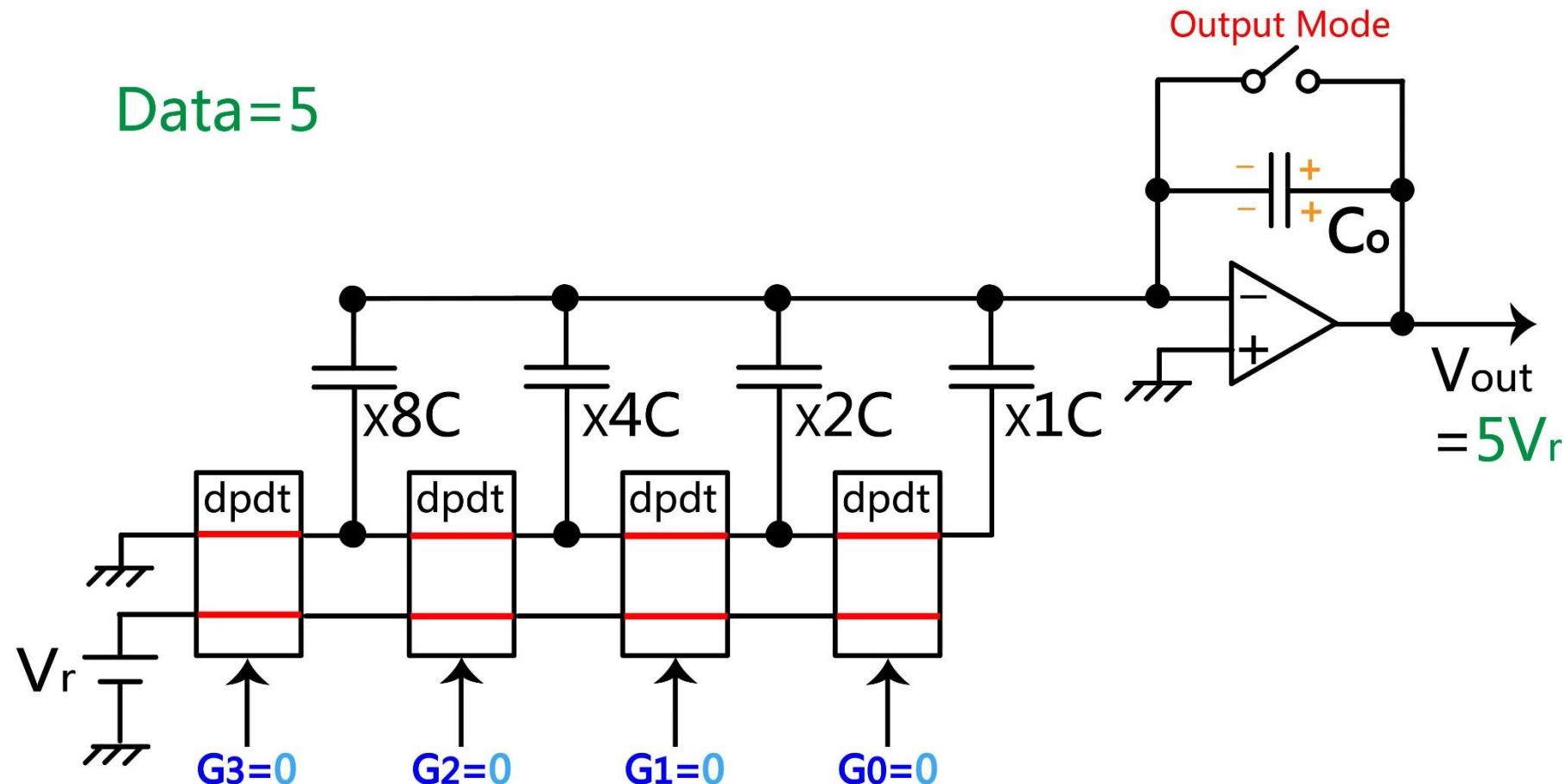


A Gray-code input charge-mode DAC

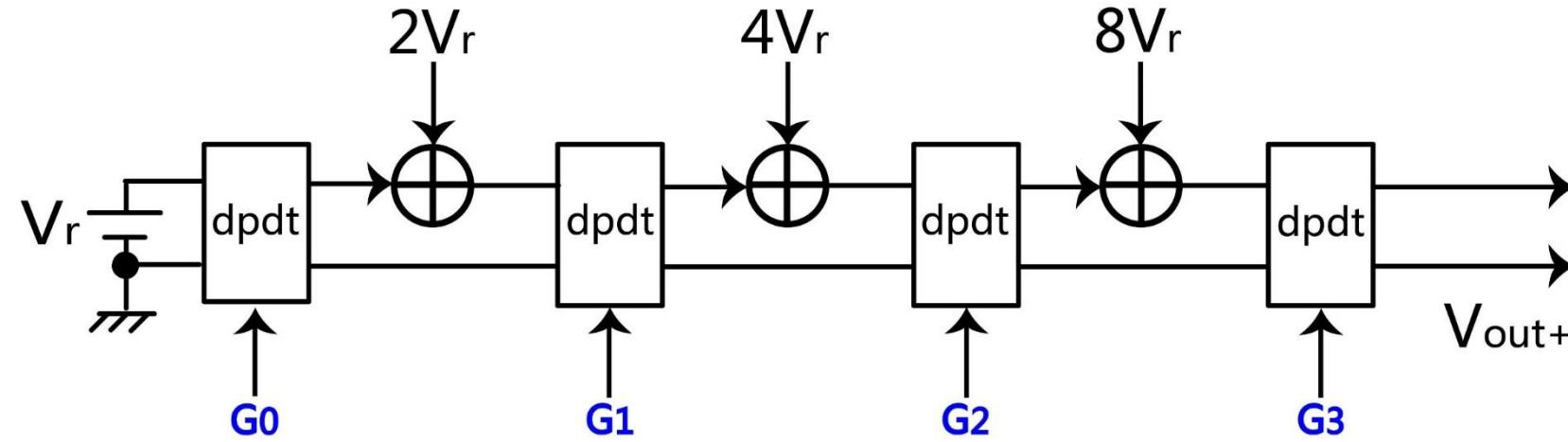
# Sample Mode of a Gray-Code Input Charge-Mode DAC (data=5)



# Sample Mode of a Gray-Code Input Charge-Mode DAC (data=5)

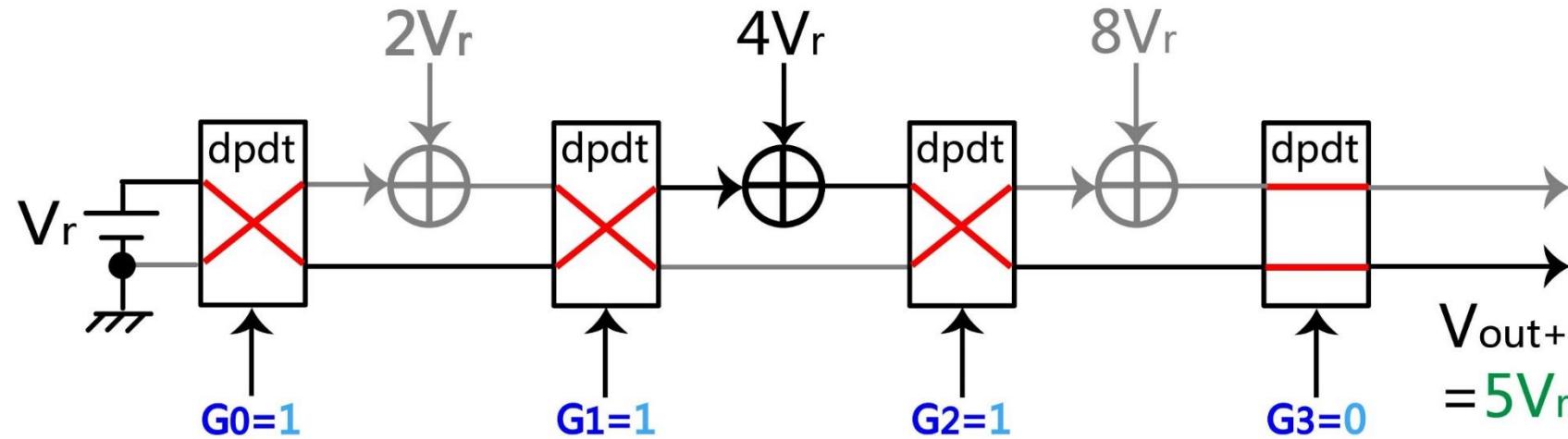


### 3.Voltage-mode Gray-Code DAC



# A Gray-Code Input Voltage-mode DAC (data=5)

Data=5



$$V_{out+} = V_r + 4V_r = 5V_r$$

# OUTLINE

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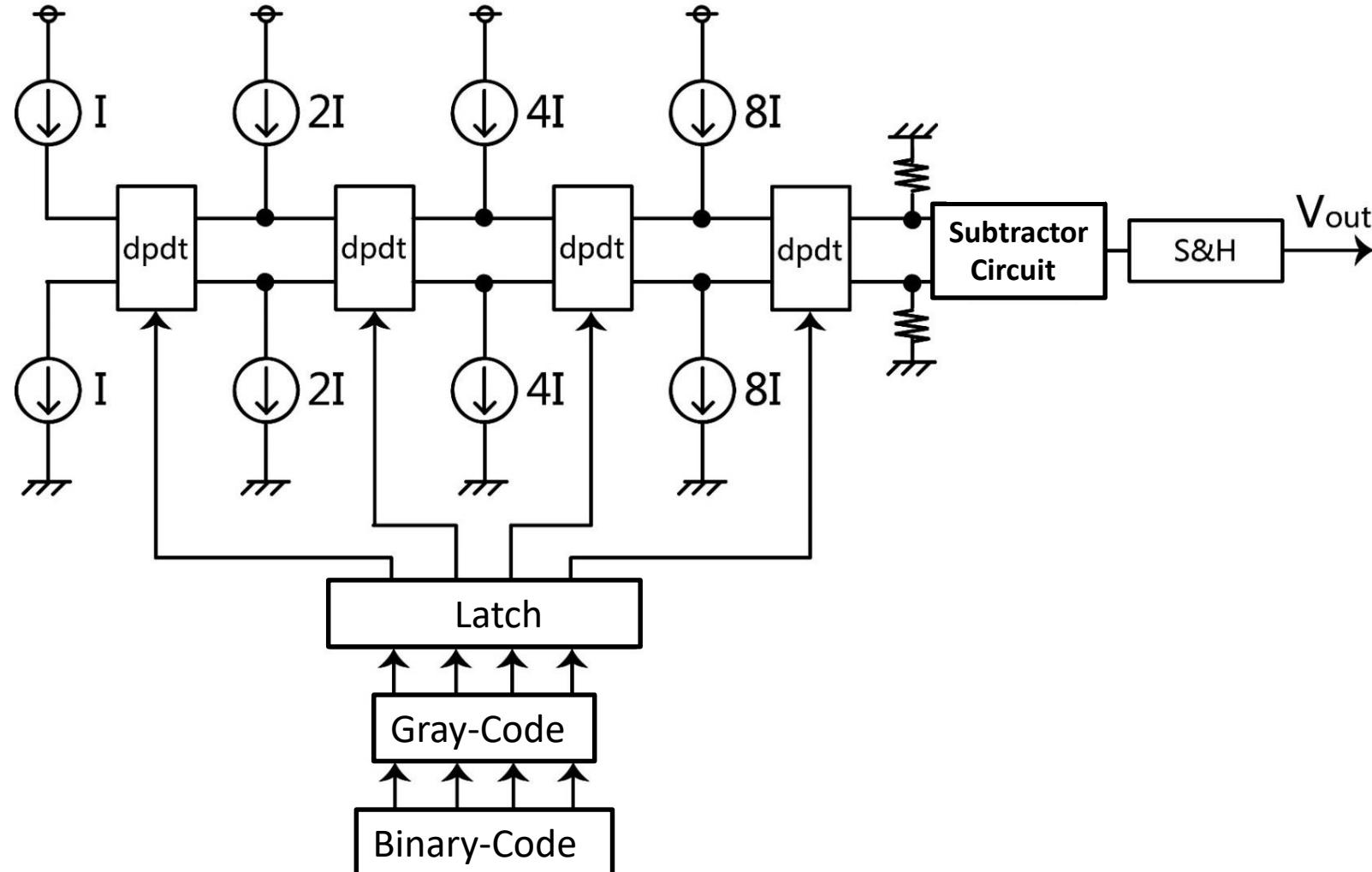
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# Simulation Verification by SPICE

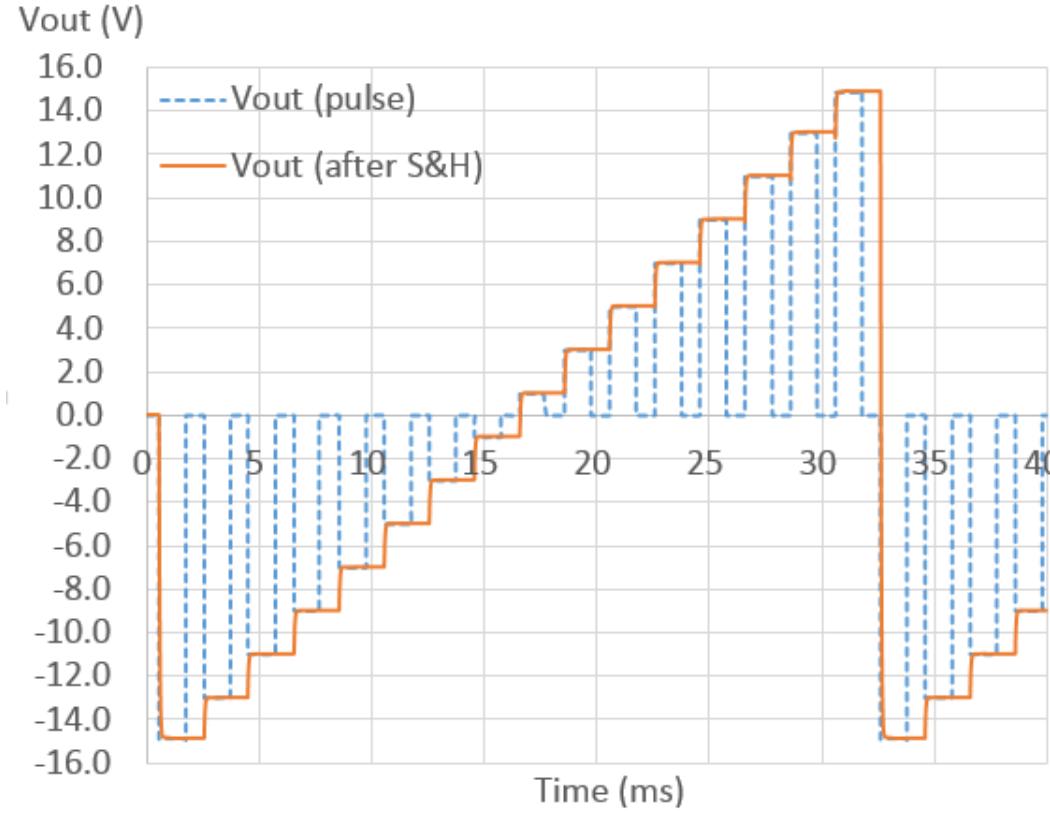
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- 1.Simulation of current-steering Gray-Code DAC
- 2.Simulation of charge-mode Gray-Code DAC
- 3.Simulation of voltage-mode Gray-Code DAC
- 4.Verification of glitch reduction

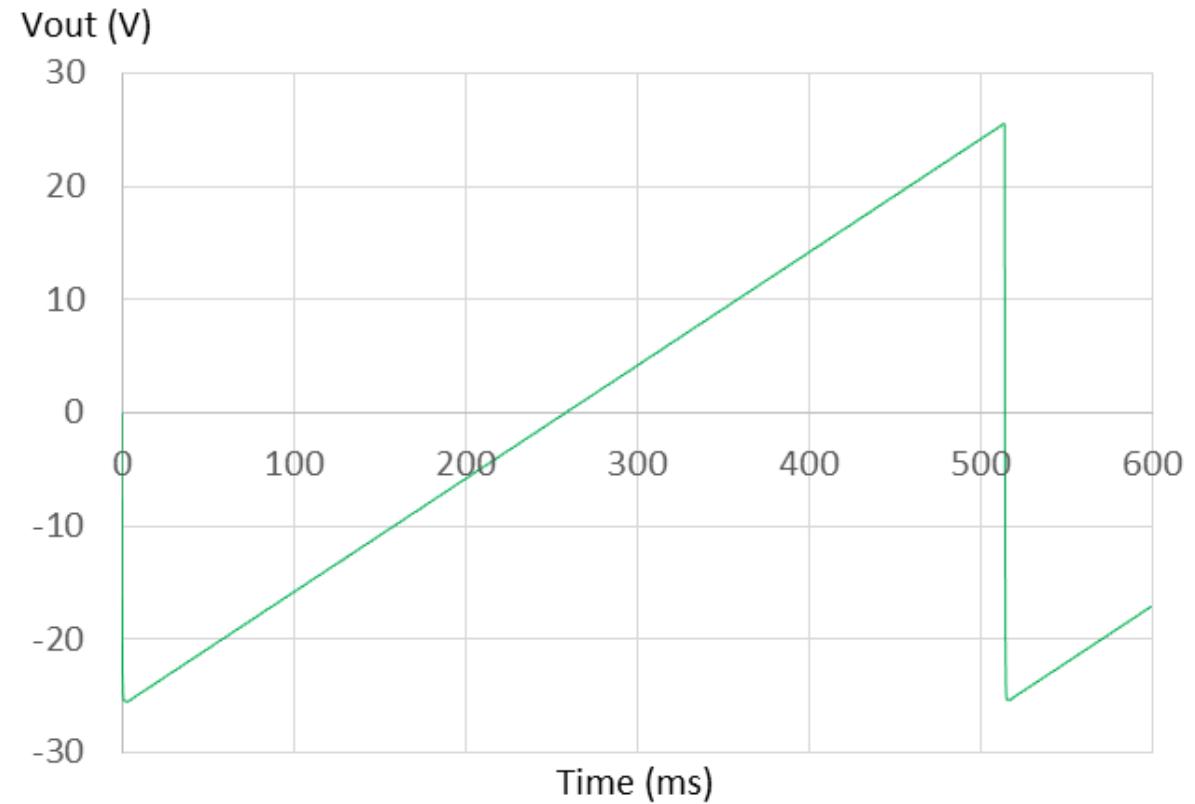
# 1.SPICE Realization of Current-Steering of Gray-Code Input



# 1.Simulation of current-steering Gray-Code DAC

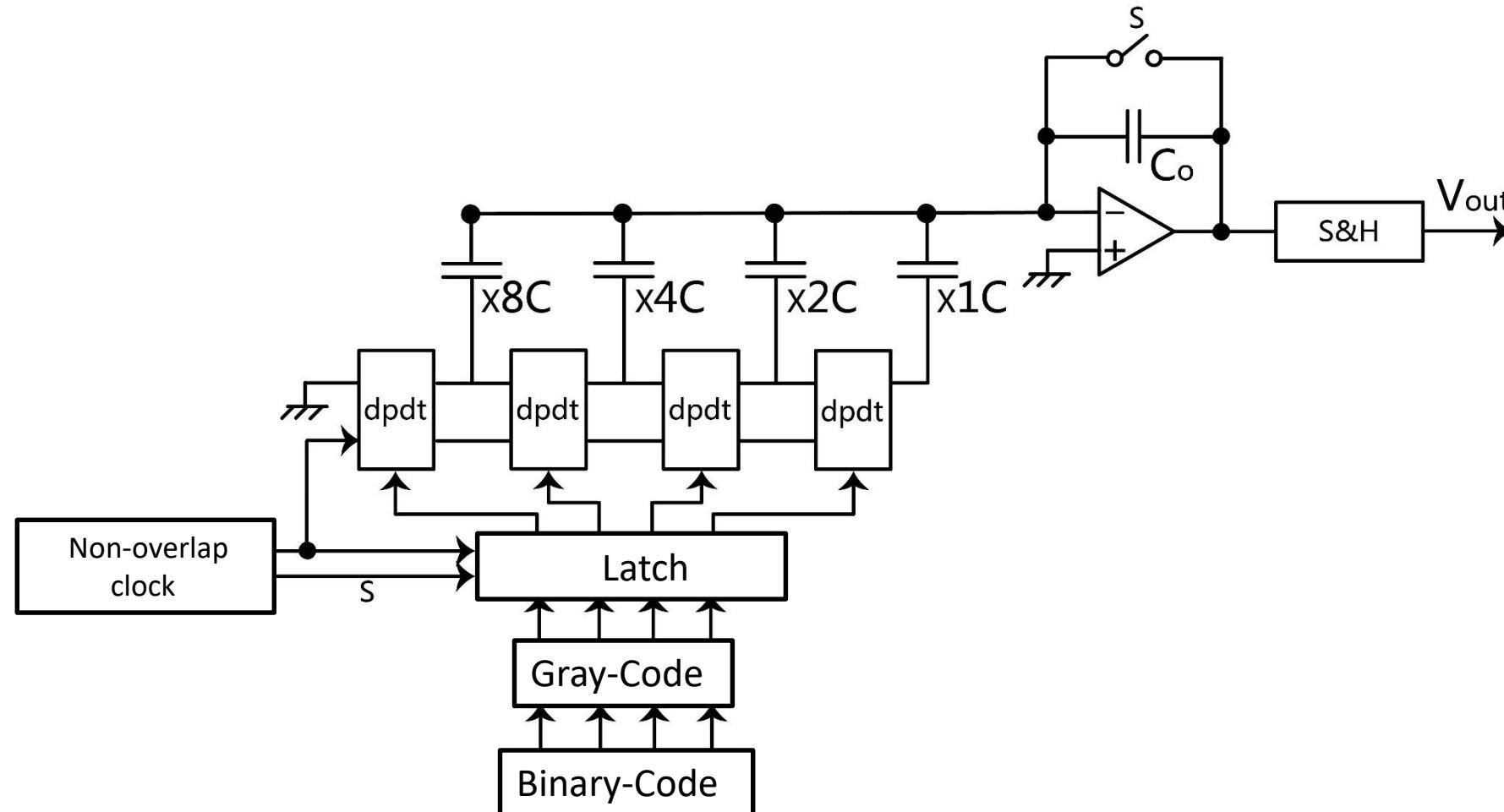


4bit Current-steering DAC

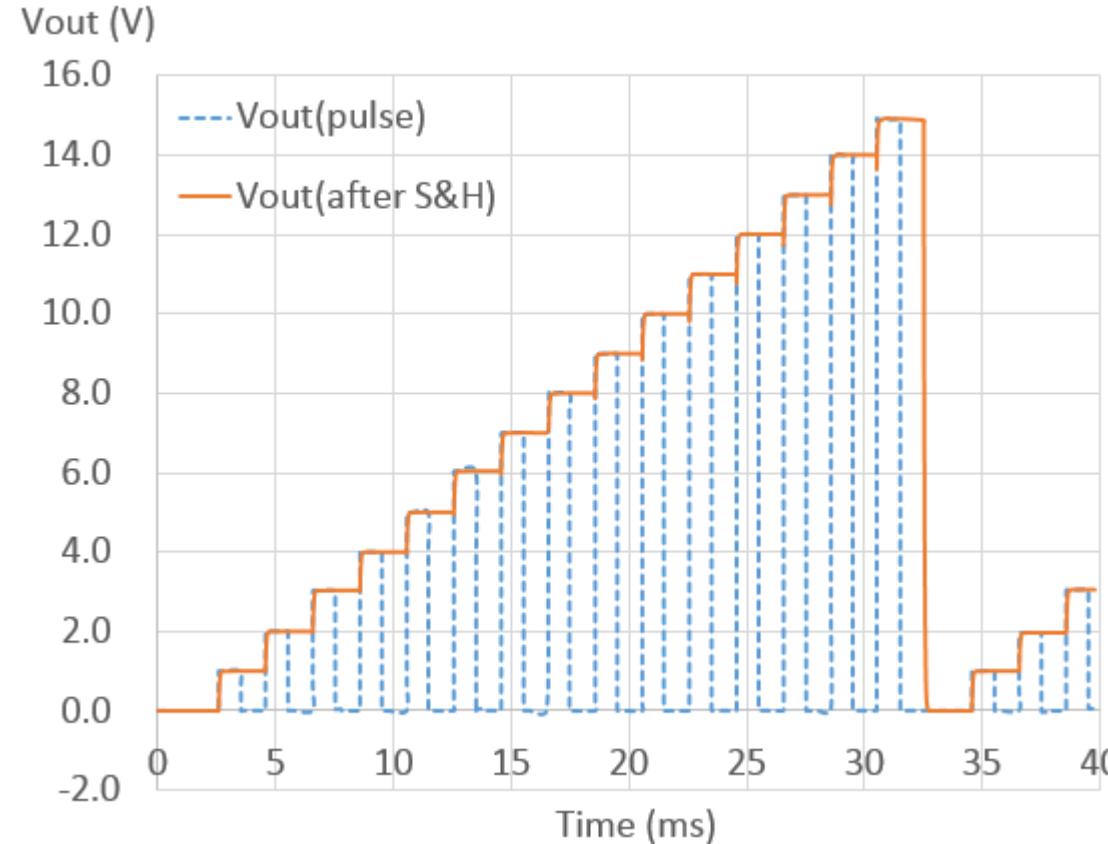


8bit Current-steering DAC

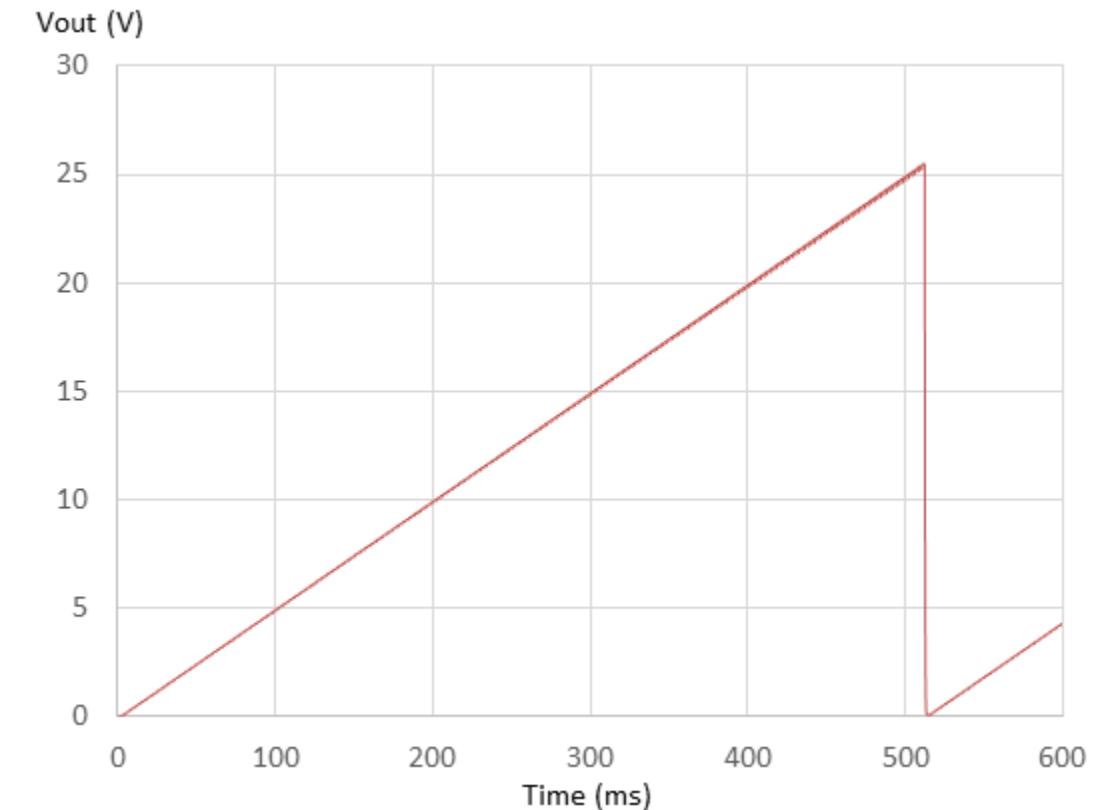
## 2.SPICE Realization of charge-mode of Gray-Code Input



## 2. Simulation of charge-mode Gray-Code DAC

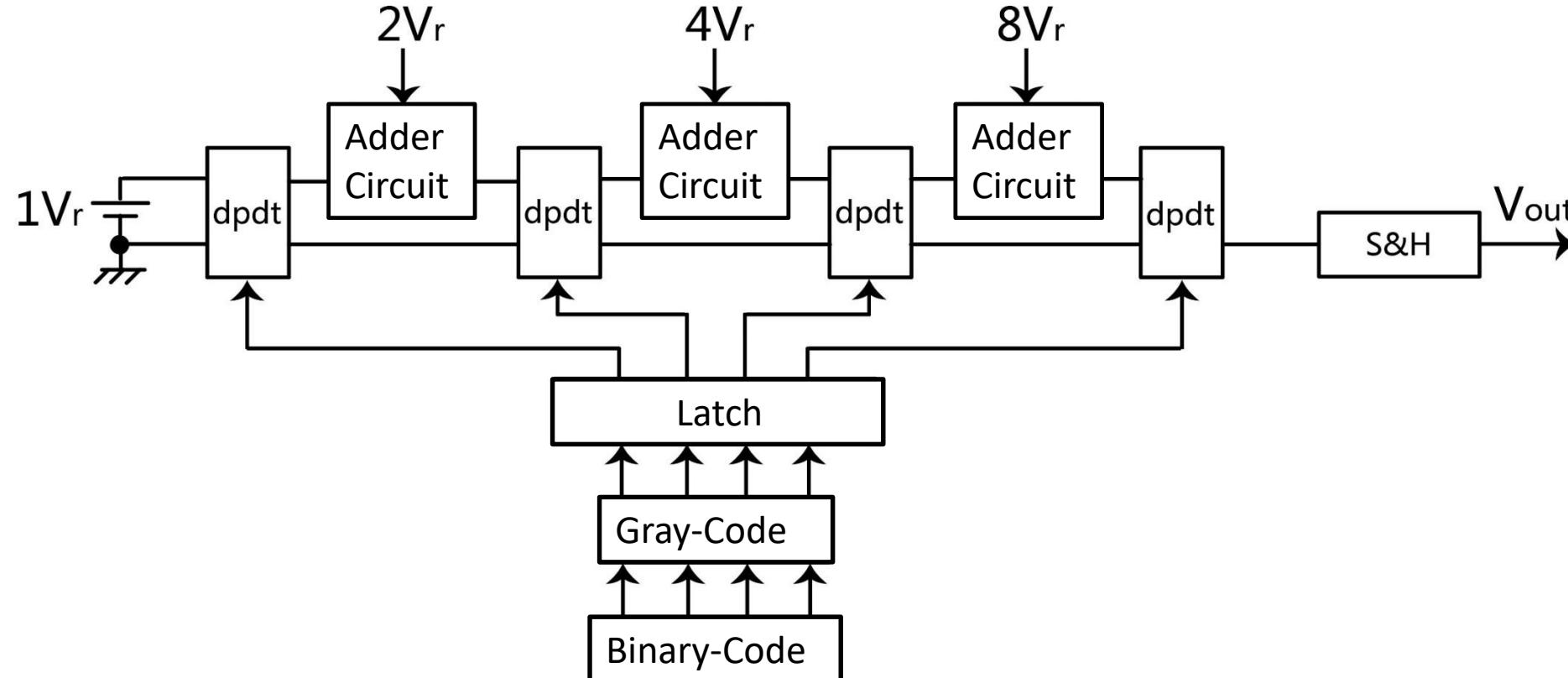


4bit Charge-mode DAC

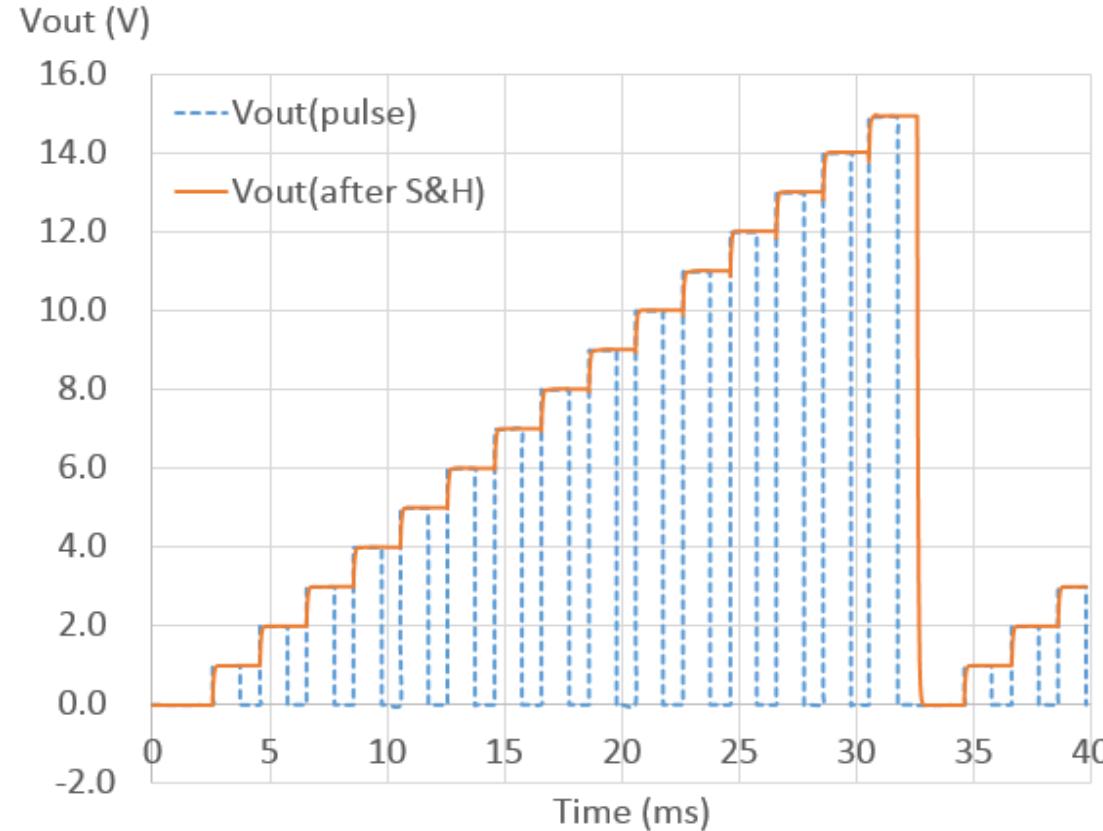


8bit Charge-mode DAC

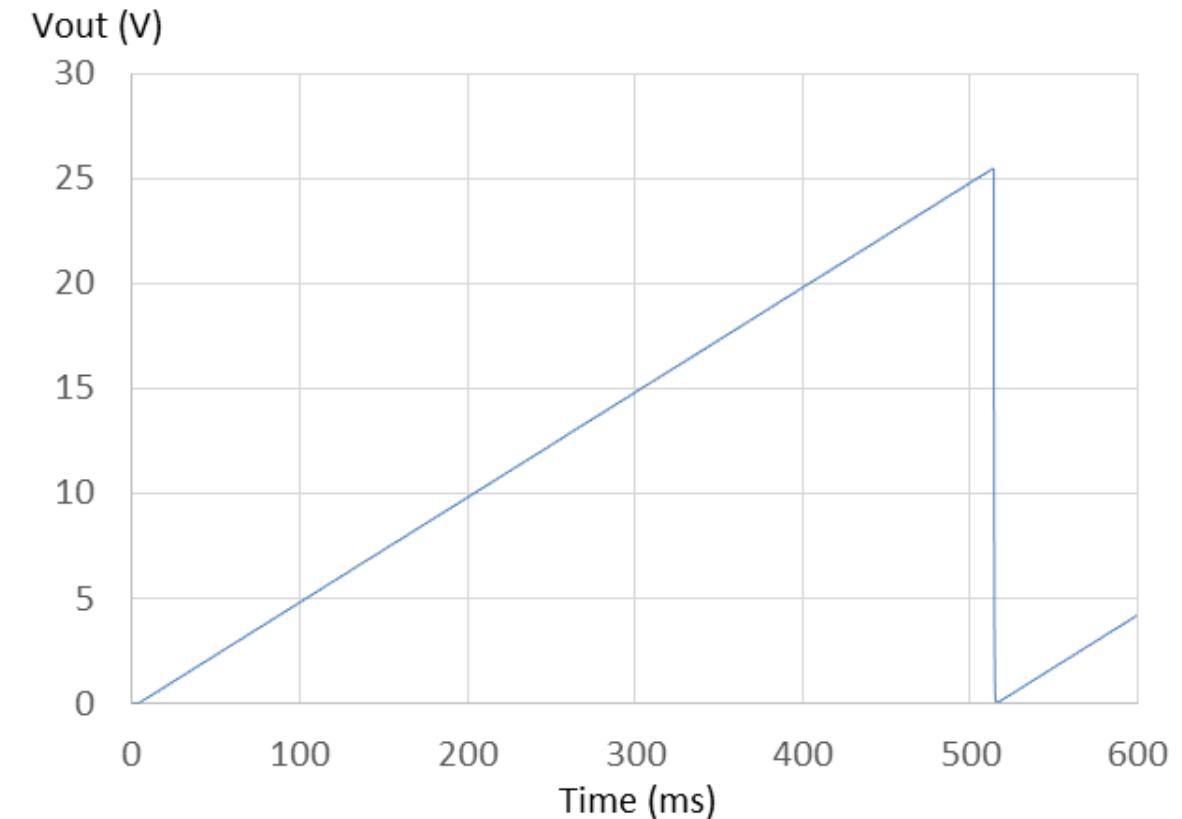
### 3.SPICE Realization of Voltage-mode of Gray-Code Input



### 3. Simulation of Voltage-mode Gray-Code DAC

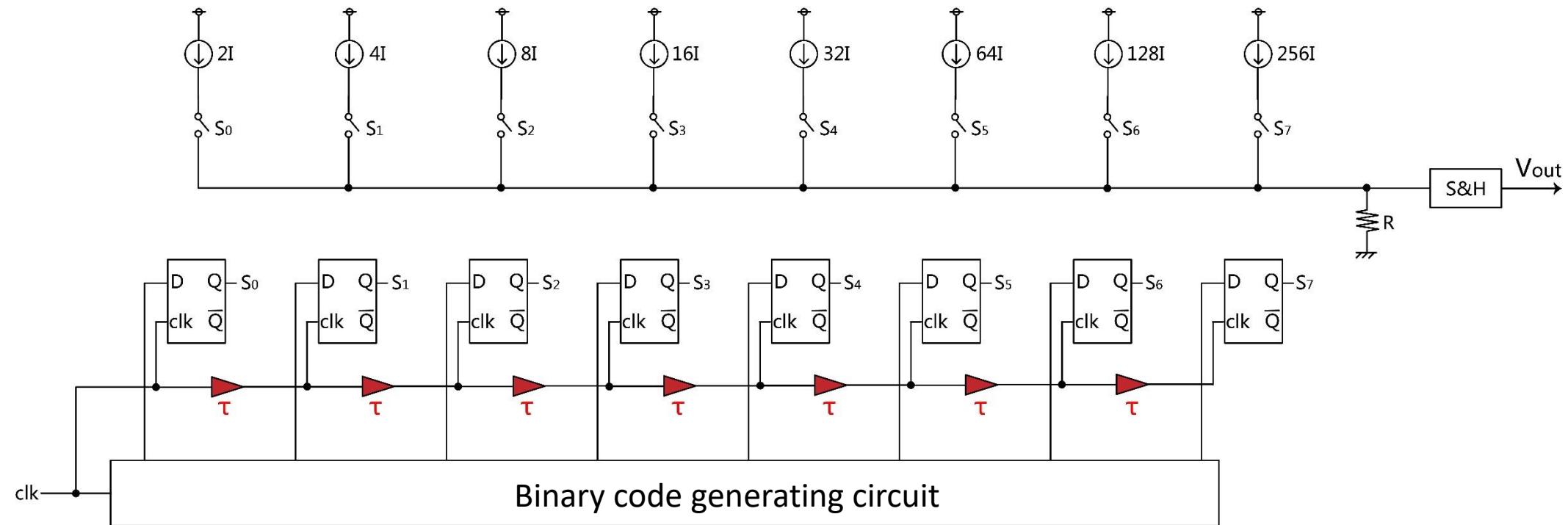


4bit Voltage-mode DAC



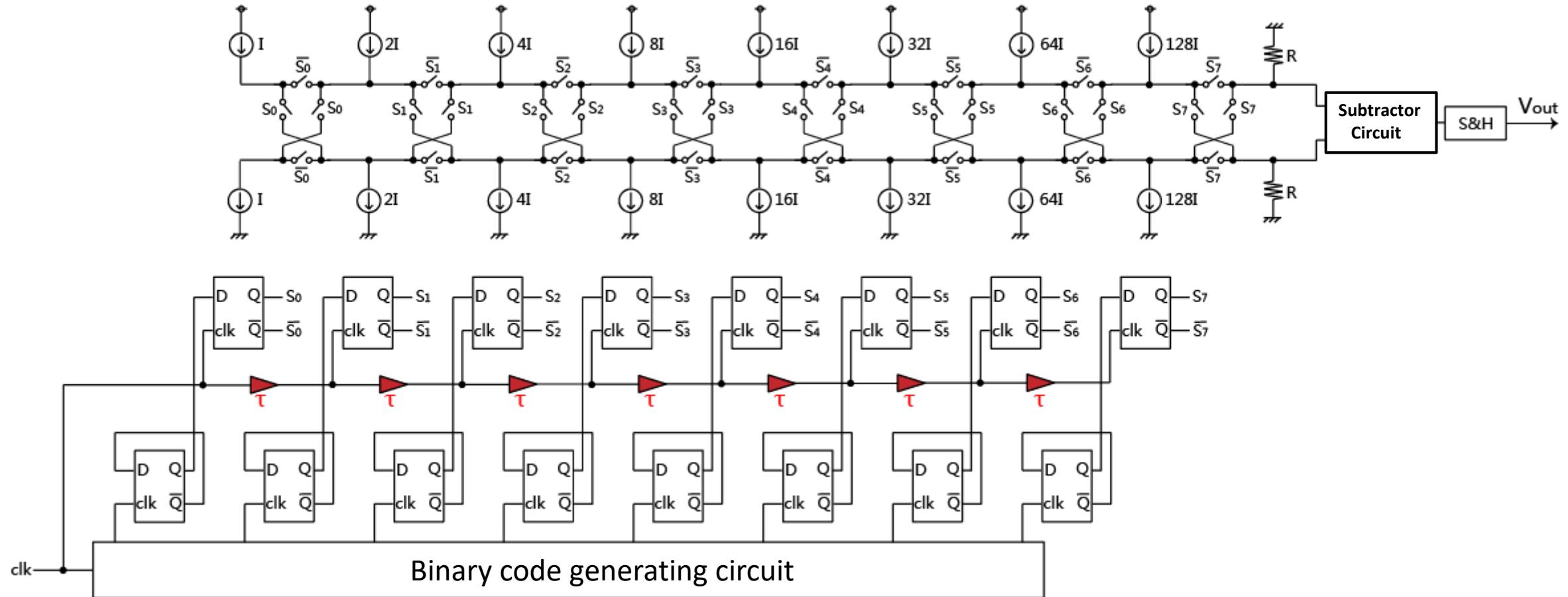
8bit Voltage-mode DAC

# 4.Verification of glitch reduction



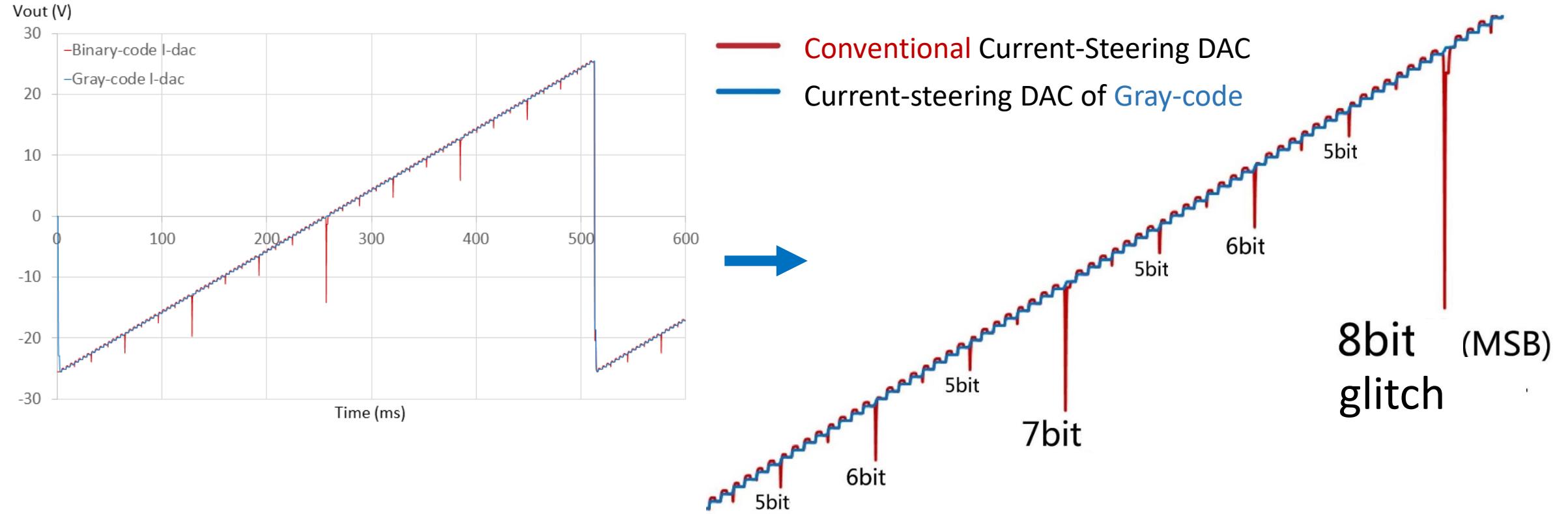
Conventional Current-Steering DAC with switching delay (8bit)

## 4.Verification of glitch reduction



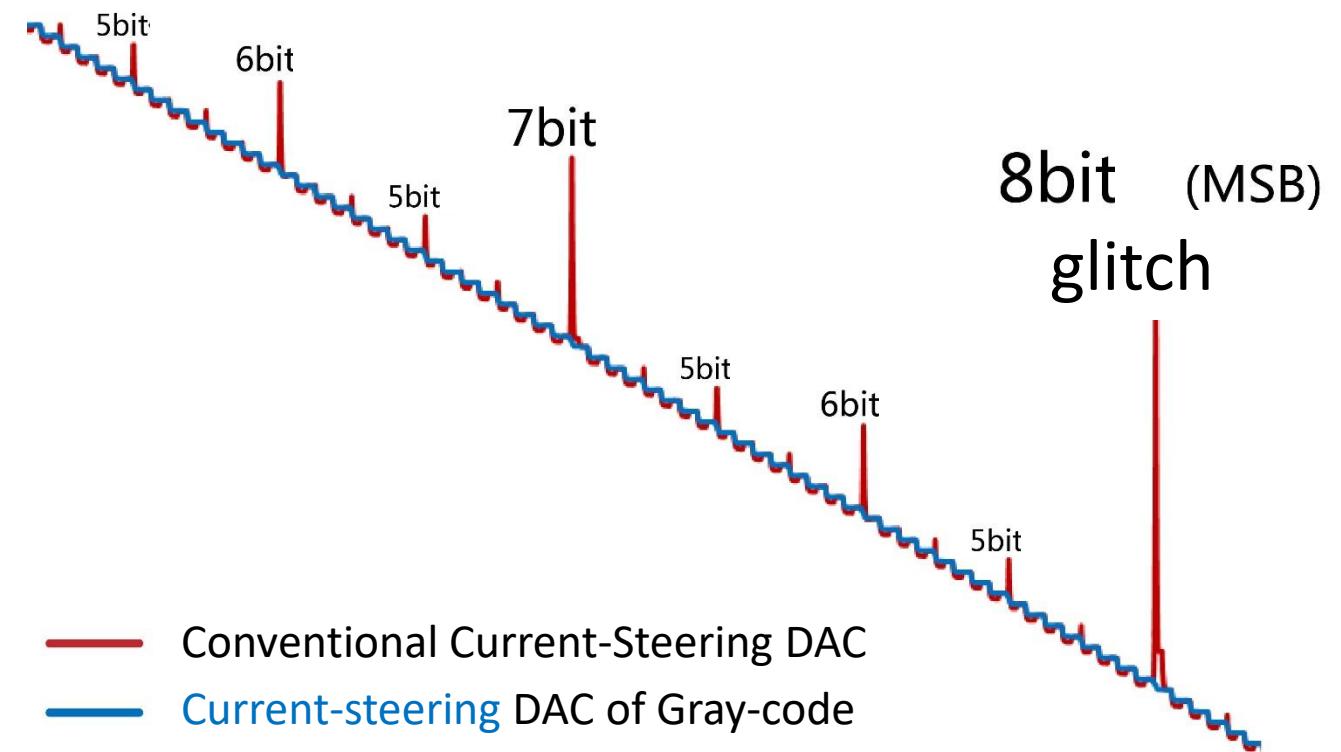
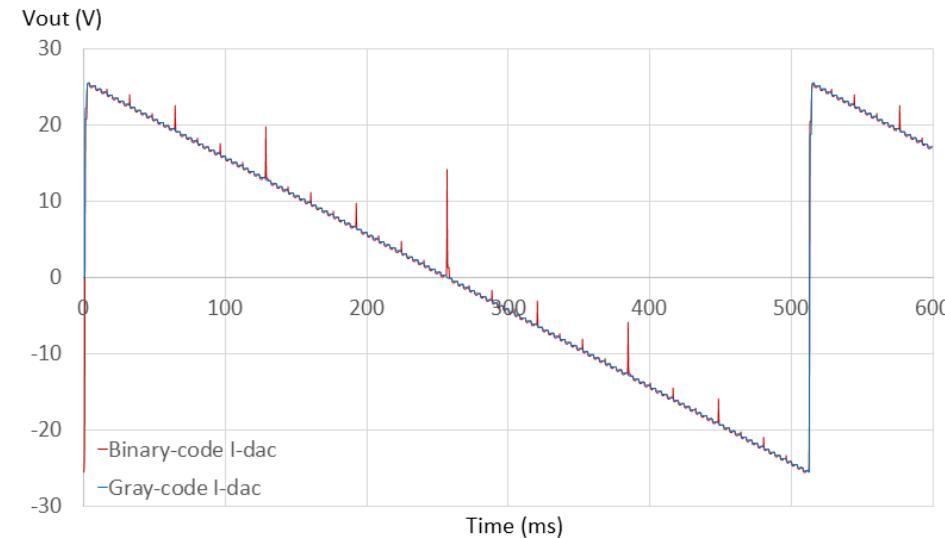
Current-Steering **Gray-code** input DAC with switching delay (8bit)

## 4.Simulation Result (Up Sweeping)



Conventional Current-Steering DAC vs. Current-steering DAC of Gray-code

## 4.Simulation Result (Down Sweeping)

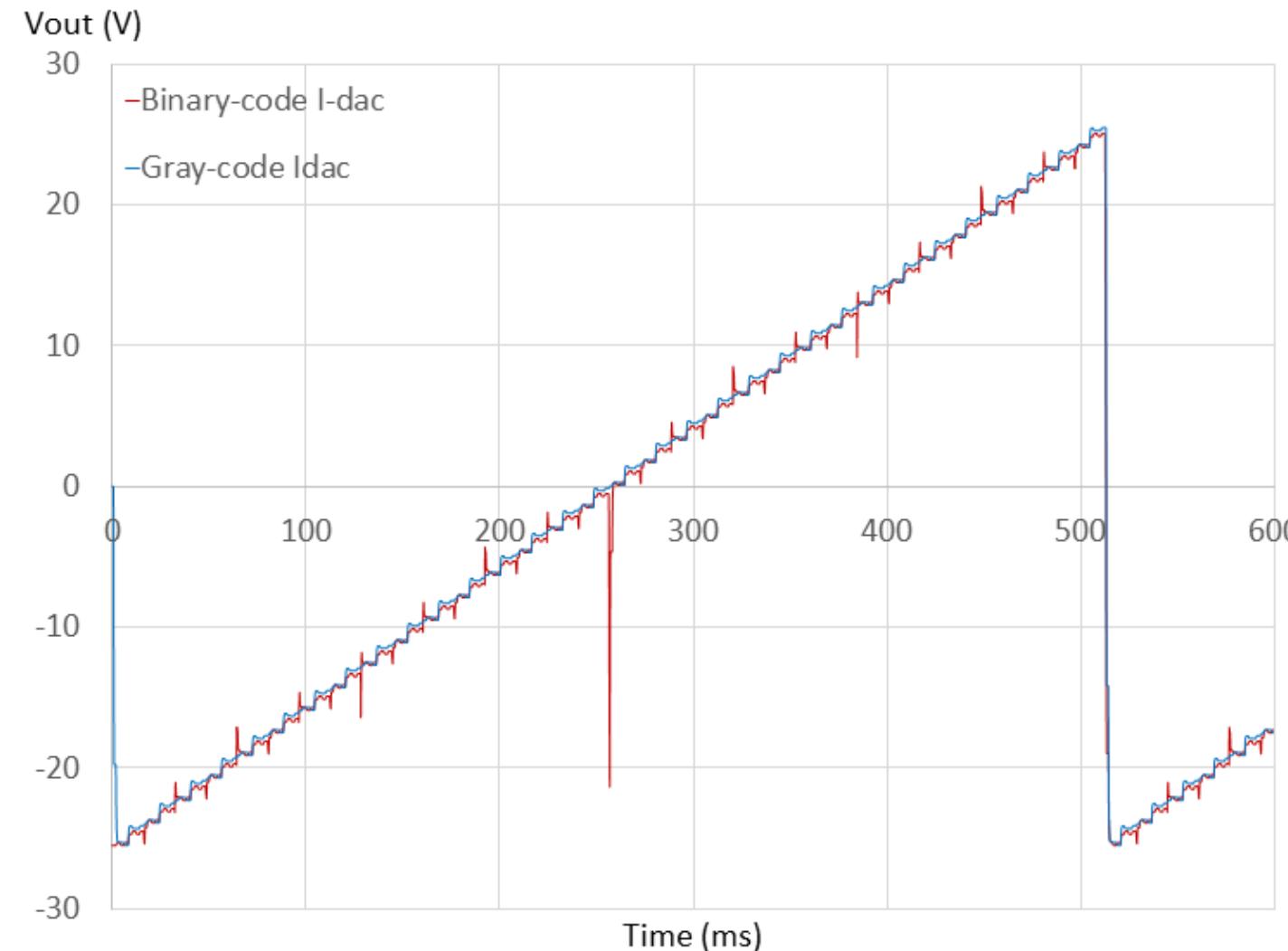


Conventional Current-Steering DAC

vs.

Current-steering DAC of Gray-code

## 4. Simulation Result (Random Switching Delay)



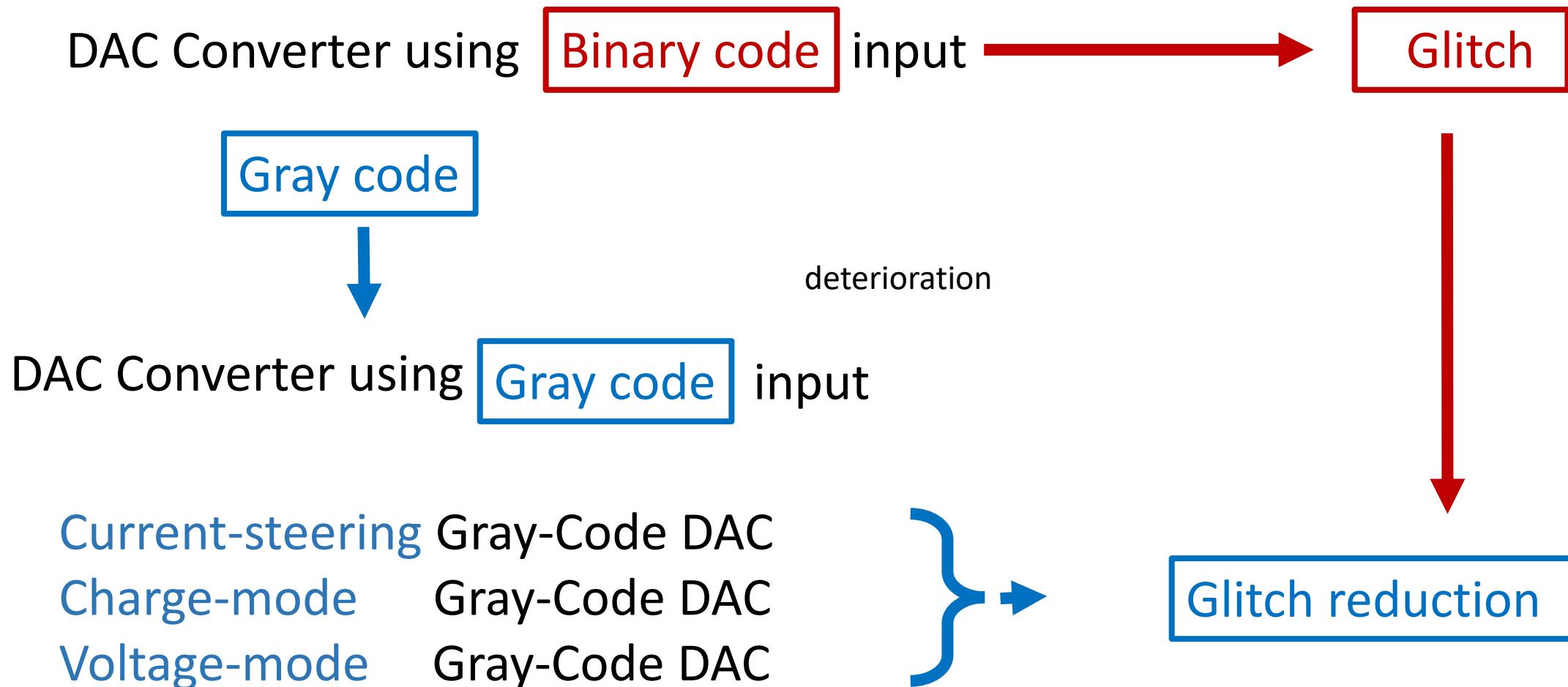
Conventional Current-Steering DAC    vs.    Current-steering DAC of Gray-code

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# Conclusion



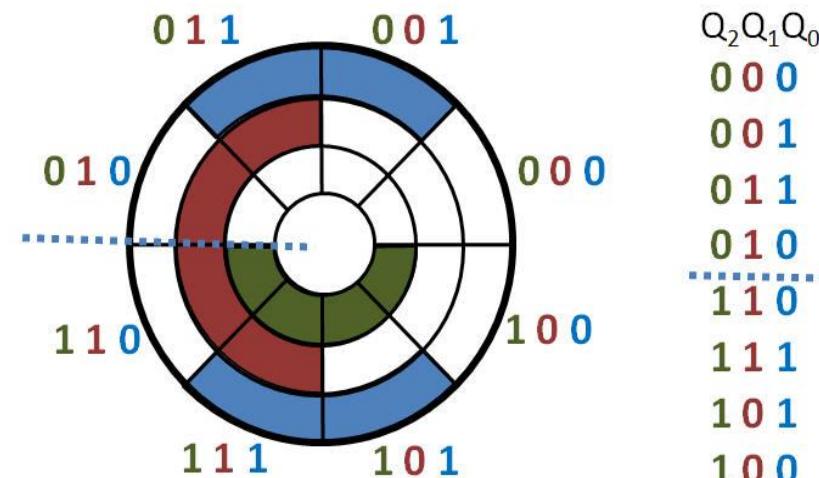
# Final statement

- Coding method can lead to **robust** mixed-signal circuit design.

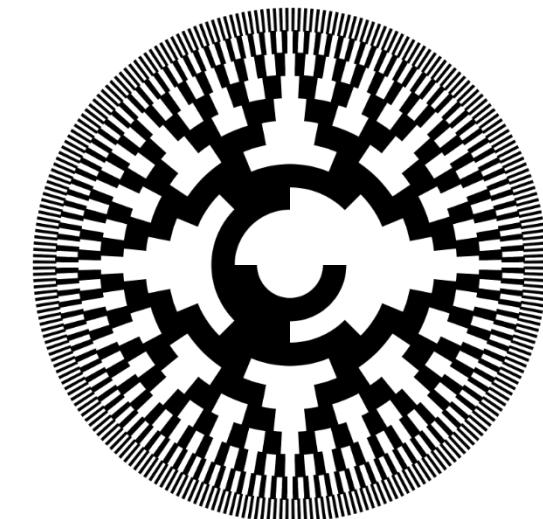
Gray code was invented by Frank Gray at Bell Lab in 1947.



FRANK GRAY and A. L. Johnsruud in television booth. Behind the glass panels at sides and top are the photo-electric cells.



$Q_2 Q_1 Q_0$
0 0 0
0 0 1
0 1 1
0 1 0
1 1 0
1 1 1
1 0 1
1 0 0



# Thank you for listening

谢谢