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ドレイン抵抗劣化の新モデルを用いた LDMOS 信頼性シミュレーションの提案

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A Reliability SPICE Simulation Method
Using a Novel Drain Resistance Degradation Model of LDMOS's

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A complete aging circuit simulation method using a drain resistance degradation model of laterally-diffused MOSFETs (LDMOS's). The drain resistance degradation caused by the hot electron injection (HCI) effect in the drain drift region has been formulated, and then implemented in SPICE. A practical circuit aging simulation procedure has been demonstrated with LDMOS measurements for a simple circuit, effectively.

キーワード：信頼性シミュレーション、ホットキャリア注入、経年回路モデル、LDMOS、コンパクトモデル
(Reliability Simulation, Hot Carrier Injection, Aging Model, LDMOS, Compact Model.)

1. Introduction

Laterally diffused MOS (LDMOS) transistors are widely used in mixed-signal applications where high voltage capability is required. In typical applications these devices are switched between a state with high V_{ds} to low V_{gs} and a state with low V_{ds} to high V_{gs}. During switching, significant degradation induced by hot carrier injection (HCI) may occur [1]. Reliability circuit simulation provides a much more accurate estimation of circuit lifetime. Several approaches [2-5] are reported, however, these are difficult for many circuit designers to follow the procedures because of their resource limitations. Among these approaches, [2] is relatively easy to apply for practical circuit design except that their peak electric field (E_m) calculation method is not described.

We derived the maximum electric field model by solving the Poisson equation using the LDMOS structure, and modified it with semi-empirical equations. Based on the new Em model, a new drain drift region resistance (R_{drift}) degradation model of n-channel LDMOS has been developed and verified with stress measurements. Also, a

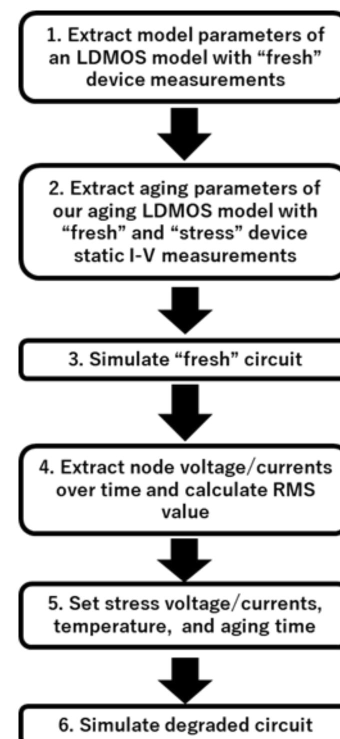

Fig. 1 Schematic illustration of the simulation flow used in circuit reliability simulation.

new procedure to simulate circuit reliability without any loop-back is presented.

As shown in Fig. 1, our aging circuit simulation method is simple and straight-forward. HiSIM-HV model [6] has been applied to simulate n-channel LDMOS devices for "fresh" characteristic. The "stress" device characteristic is simulated by implementing our R_{drift} degradation model since R_{drift} is existing in the HiSIM-HV model as an internal variable. We define a switch parameter to enable/disable the degradation model. Static bias and temperature stress measurements are used for aging model parameter extractions, and RMS voltage biases are calculated from pulsed signals for transient stress simulations.

A fundamental DC-DC converter type test circuit is designed for our LDMOS degradation model verification. The circuit includes minimum number of passive components and one n-channel LDMOS to observe our model behavior.

2. HCI Induced Drain Resistance Degradation Model in the Drift Region

The HCI degradation of n-channel LDMOS is to increase R_{drift} by decreasing carriers in the drift region [2]. The increased amount of R_{drift} correlates with the lateral maximum electric field. R_{drift} degradation model depends on time, which is written in the following equation [2]:

$$\frac{\Delta R_{drift}}{R_{drift}} = A_1 \cdot \ln\left(1+\frac{t}{\tau}\right) + A_2 \cdot \ln\left(1+\frac{t}{\gamma \cdot \tau}\right) \tag{1}$$

where A_1, A_2, and γ γare device specific parameters, t is the stressing time, τ is characteristic time which is a bias and geometry dependent parameter. In Eq. (1), τ is expressed in (2):

$$\tau = \left(\frac{\alpha \cdot W}{I_D}\right)^n \cdot \frac{\phi_b}{E_m\lambda}\ e^{\frac{\phi_b}{E_m\lambda}} \tag{2}$$

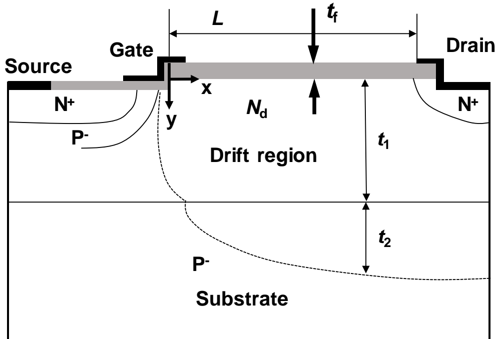

Fig.2 The structure of the n-channel LDMOS to derive the electric field

where α is a device specific empirical fitting parameter,W is the device width, E_m is the magnitude of the maximum electric field, n is a coefficient to be used for recent nano-meter process devices, λ is the mean free path that carriers can travel in this electric field before going through an energy losing scattering event, and ϕ_b is the energy needed for electrons to surmount the Si-SiO_2 energy barrier.

Since the stress bias voltages dependencies of V_{gs} and V_{ds} on the peak electric field should be supported, we developed physically based maximum electric field model equations. We have applied the LDMOS of maximum electric field model which is physically derived by solving the Poisson equation using the LDMOS structure in Fig. 2. The model is written as;

$$E_m \equiv \left|-\frac{\partial \phi_f(0)}{\partial x}\right| = \sqrt{\alpha}\frac{\left(-\frac{\beta}{\alpha}+\phi_0\right)\cosh\left(\sqrt{\alpha}L\right) + \left(V_{ds}+\frac{\beta}{\alpha}\right)}{\sinh\sqrt{\alpha}L} \tag{3}$$

where α and β are described by the following equations.

$$\alpha = \frac{\varepsilon_0}{t_1 t_f \varepsilon_{si}} + \frac{2}{{t_1}^2} \tag{4}$$

and

$$\beta = -\frac{q}{\varepsilon_{si}}\left[N_d + N_{sub}\left(\frac{t_2}{t_1}\right)^2\right] \tag{5}$$

where t_1 is the epi layer thickness with a uniform doping concentration of N_d, t_2 is the substrate depletion layer thickness with doping concentration N_{sub}, t_f is the thickness of the front interface field oxide layer with the dielectric constant of ε_{ox}, x and y measure the horizontal and vertical positions relative to silicon surface, respectively. Note that we define the boundary conditions at the Poisson equation as follows:

$$\phi_f(0) = \phi_0 = 0\ \ , \phi_f(L) = V_{ds} \tag{6}$$

where $\emptyset_f$ is the surface potential. The surface potential $\emptyset_0$ at x = 0 cannot be zero. It is expected to be a function which depends on V_{gs} and V_{ds}. However, if the function is defined as the surface potential, the differential equations cannot be solved, analytically. Therefore, we developed a fitting model of the surface potential that depends on the V_{gs} and V_{ds} at the boundary conditions.

The developed model is shown as;

$$\phi_0 = d_1 \log\left(\frac{V_{ds}}{d_2}\right) - \left[1 - \exp\left(\frac{V_{gs}-V_{th}}{R}\right)\right] \tag{7}$$

where d_1, d_2, and R Rare fitting parameters. The developed model is now dependent on stress voltages.

3. SPICE Implementation

To implement our HCI degradation of R_{drift} equation Eq. (1) into our MDW-SPICE simulator (UCB SPICE compatible simulator on Windows) HiSIM-HV 2.2 [6] source codes are adopted.

Since the drift region resistance has been defined as an instance variable, R_{drift}, it is only allowed to modify the drift resistance in the SPICE model source code. In HiSIM-HV, it is written as;

$$R_{drift} = (R_d + V_{ds} \cdot R_{DVD})\left(1 + \mathbf{RDVG11} - \frac{\mathbf{RDVG11}}{\mathbf{RDVG12}} \cdot V_{gs}\right) \cdot (1 - V_{bs} \cdot \mathbf{RDVB}) \cdot \left(\frac{\mathbf{LDRIFT1} + \mathbf{LDRIFT2}}{\mathbf{DDRIFT} - W_{dep}}\right) \tag{8}$$

where all variables written in bold font are the model parameters to represent gate and drain bias voltage dependencies.

Now the R_{drift} of Eq. (8) is directory degraded by Eq. (1) as shown in Fig. 3.

```
/*** RD degradations ***/
if (model->HSMHV_relmod == 1)  {
   lambda = model->HSMHV_lambda0 * tanh (0.063 / 2.0 / BOLTZEV /
   model->HSMHV_tnom);
   compa = 3.2 / em /lambda;
   stids = 0.0;
   if ((fabs (vgs - model->HSMHV_stvg) <= 1.0e-04) && (fabs(vds -
   model->HSMHV_stvd) <= 1.0e-04)) {
      stids = -here->HSMHV_ids; /* Source base current direction */
   } else {
            stids = 1.0e-16; /* Prevent from zero denominator */
   }
   ttau1 = pow(model->HSMHV_alpha * here->HSMHV_w / stids,
   model->HSMHV_mdeg);
   ttau2 = pow (compa, exp(compa)); /* Check compa value for errors */
   ttau = ttau1 * ttau2;
   rdpart1 = model->HSMHV_a1 * log (1.0 + model->HSMHV_sttime /
   ttau);
   rdpart2 = model->HSMHV_a2 * log (1.0 + model->HSMHV_sttime /
   ttau / model->HSMHV_gamma);
   here->HSMHV_Rd = here->HSMHV_Rd * (1.0 + rdpart1 + rdpart2);
   if (model->HSMHV_info <= -1 ) printf("here->HSMHV_Rd = %e¥n",
   here->HSMHV_Rd);
} /* if (model->HSMHV_relmod == 1) */
```

Fig. 3 R_{drift} degradation SPICE C source code

The Em calculations are shown in Fig. 4.

4. Parameter Extraction and Circuit Simulation

We prepared an LDMOS whose gate oxide thickness, channel length, and channel width are 11.5 nm, 0.4 μm, and 500 μm, respectively, and then measured fresh and stressed I_{ds}-V_{gs}, I_{ds}-V_{ds} characteristics Continuous gate and drain voltage stress has been supplied for 31,620 seconds at the temperature of 393 K. During the stressing process, the I-V measurements were performed, periodically as shown in Fig. 6.

HiSIM model parameters are extracted with fresh DC I-V measurements. Next, degradation parameters of our model are extracted with stressed and fresh DC I-V and I_{dmax} - time measurements in Fig. 6. The extracted degradation model parameters are listed in Fig. 5. The degradation simulations as shown in these figures are accurate enough to estimate n-channel LDMOS characteristics.

For a circuit verification, we organized a simple DC-DC converter as shown in Fig. 7. After the fresh simulation, the pulsed stress gate voltage of the n-channel LDMOS is monitored, and then calculate it to RMS value which is set to the stress gate voltage. The constant drain voltage of the n-channel LDMOS can be the stress drain voltage. After setting these two stress voltages, the stress simulation has been performed with the degradation model parameter is activated. The final stressed and fresh simulation results are shown in Fig. 8. The output voltage degradation is simulated, successfully.

```
/*** Em calculations ***/
salpha = EPS0 / model->HSMHV_tdep1 / model->HSMHV_trsf / EPSSI
+ 2.0 / model->HSMHV_tdep1 / model->HSMHV_tdep1;
sbeta = -Charge_q / EPSSI * (model->HSMHV_ndepm + model-
>HSMHV_nsubc * (model->HSMHV_tdep2*model->HSMHV_tdep2 /
model->HSMHV_tdep1 / model->HSMHV_tdep1));
phi0 = model->HSMHV_d1 * log((vds+1) / model->HSMHV_d2) -
model->HSMHV_vdeg * (1 - model->HSMHV_d3*exp(model-
>HSMHV_stvg - Vth0 / model->HSMHV_drr));
em = sqrt(salpha) *((-sbeta / salpha + phi0) * cosh(sqrt(salpha) * here-
>HSMHV_lgate) + model->HSMHV_stvd + sbeta / salpha) /
sinh(sqrt(salpha) * here->HSMHV_lgate);
```

Fig. 4 SPICE C Source code of Em calculations

+ RELMOD = 1
+ D1 = 11.67
+ D2 = 4.718e-06
+ D3 = 0.82
+ DRR = 11.7
+ TDEP1 = 4e-06
+ TRSF = 1.0e-08
+ TDEP2 = 1.0e-06
+ VDEG = 1.0
+ A1 = 1.0e-02
+ A2 = 1.0e-01
+ LAMBDA0 = 4.5e-06
+ ALPHA = 164.8E-06
+ MDEG = 0.7328
+ STTIME = 6.0E9
+ STVG = 1.0
+ STVD = 20.0
+ GAMMA = 889.2E-06

Fig. 5 Extracted degradation model parameters

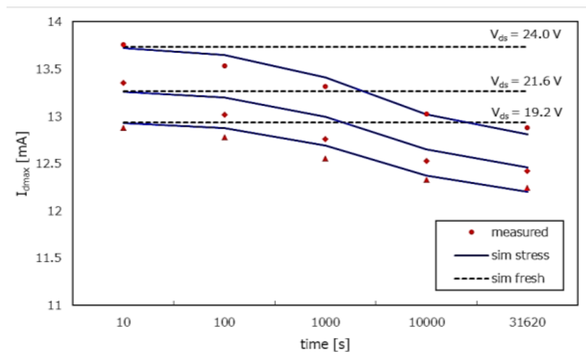

Fig. 6 Fresh and stressed I_{dmax} vs. stressed time characteristics of the n-channel LDMOS. Where I_{dmax} is the drain current at V_{gs} = 6V.

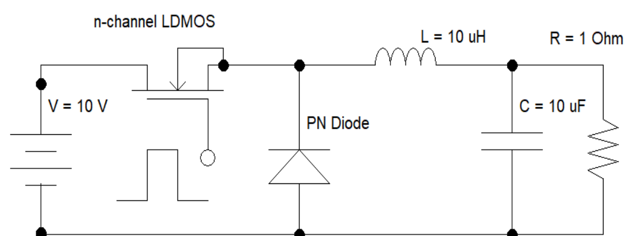

Fig. 7 The equivalent test circuit of the fundamental DC-DC converter. A pulsed bias is supplied at the gate of the n-channel LDMOS device. The pulse period, rise time, fall time, delay time, width, and amplitude are 4.5 μs, 1 ns, 1 ns, 1ns, 2 μm, and 15 volts, respectively.

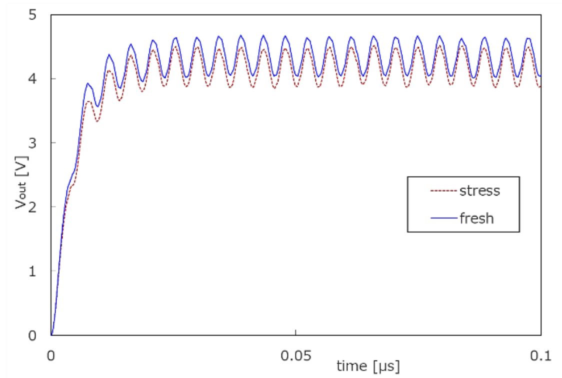

Fig. 8 Fresh and stressed V_{out} simulation waveforms of the test circuit (in Fig. 4).

5. Conclusions

A new drain drift region resistance (R_{drift}) degradation model of n-channel LDMOS has been developed and verified with stress measurements. We derived the maximum electric field model by solving the Poisson equation using the LDMOS structure, and modified it with semi-empirical equations. The degradation model parameters of the model were extracted with n-channel LDMOS measurements, accurately.

Also, a new procedure to simulate circuit reliability without any loop-back is presented. Using the new model and the procedure, an aging simulation of a fundamental DC-DC converter was presented.

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