Limit Cycle Suppression Technique
Using Random Signal
In Delta-Sigma DA Modulator

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Research Objective

Objective

• Development of high linear & high resolution ΔΣ DAC

Studies

• Limit cycle suppression using random signal at quantizer input.
Outline

• Research Background
• Proposed Circuit
• Simulation Configuration & Results
• Conclusion
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**ΔΣ DA Converter**

- **Digital input**
- **Integrator**
- **Quantizer**
- **ΔΣ Modulator**
- **Feedback**
- **Digital output**

**Analog output**

**High linear**

**High resolution**

**Usage**

- Measurement
- Audio system
- Satellite communication

**△ΣΔDA Converter**
Modulator type

(1) low-pass (LP) type

(2) high-pass (HP) type

(3) band-pass (BP) type

(4) multi-BP type I

(5) multi-BP type II

Modulator output power spectrum

Noise power
Merits & Demerits of $\Delta \Sigma$ DAC

**Merit**

- Mostly digital circuit
- High linear & high resolution for low frequency signal generation

**Demerit**

- Limit cycle problem for small input

※ Due to modulator nonlinearity by quantizer
Limit Cycle Problem

Digital input $\rightarrow \Sigma \rightarrow$ Modulator output $\rightarrow 1$ bit DAC $\rightarrow$ Analog output

Removal of analog signal by LPF sharply $\Rightarrow$ difficult

Analog output $=$ Signal $+$ Limit cycle (Noise)

Objective
- Limit cycle suppression
- Relax LPF requirement
Our Studies

Digital input

+ Random signal

\[ \text{Limit cycle reduction with random signal at quantizer input} \]

Analog output

1bit DAC

Analog LPF

Limit cycle

Stair

Smoothness!
Other Dither Method

Adding random signal to digital input

Random signal

Digital input

Drawbacks

- Input range sacrifice
- Random signal has to be out of signal band
difficult to generate
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Proposed Method

< Features >

① NOT sacrifice input range
② NOT affect signal band, thanks to noise-shaping
③ Easily generate random signal.
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In 10-bit case

Random signal:
-1.0~+1.0, -2.0~+2.0, -3.0~+3.0

Digital signal
DC: -1.0~+1.0

Random signal

Digital dither signal

Controlled by number of 1’s

Modulator output
「0」 or 「1」
Modulator Operation with Random Signal

- Without random signal
- With random signal

DC Input → \(\sum\) → \(\oplus\) → \(\sum\) → \(\oplus\) → Output

Time domain

\[1 \ 0 \ 0 \ 0 \ 1 \ 0 \ 0 \ 0 \ 1 \ 0 \ 0 \ 0 \]

Period

Order of '0' and '1' \(\Rightarrow\) different
Total numbers of 1's \(\Rightarrow\) the same

Frequency domain

DC signal power \(\Rightarrow\) the same

Linear

Noise

Diffusion
Simulation Results

Random signal: -2.0 ~ +2.0

DC Input = 0.1

Without dither

Proposed
SFDR (Spurious Free Dynamic Range)

10-bit first-order
LP case
DC = 0.1

\[
SFDR = \frac{\text{Signal Power}}{\text{Maximum Harmonics Power}}
\]

\[SFDR = 5.39 \text{ dB} < 15.59 \text{ dB}\]

Without dither

Proposed
Linearity is confirmed with simulation result.

Ideal result can be obtained with random signal between -2.0 ~ +2.0
10-bit first-order LP case

SFDR Comparison

“precision 3” → 1.782
“precision 4” → 1.7824
“precision 5” → 1.78245

SFDR (dB)

DC Input (Full scale -1~+1)

-1 -0.5 0 0.5 1
-1 -0.5 0 0.5 1

-1 -0.8 -0.6 -0.4 -0.2 0 0.2 0.4 0.6 0.8 1

-1 -0.8 -0.6 -0.4 -0.2 0 0.2 0.4 0.6 0.8 1

SFDR (dB)

DC Input (Full scale -1~+1)

-1 -0.5 0 0.5 1
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-1 -0.8 -0.6 -0.4 -0.2 0 0.2 0.4 0.6 0.8 1

-1 -0.8 -0.6 -0.4 -0.2 0 0.2 0.4 0.6 0.8 1

SFDR much improved
14-bit second-order BP case

Simulation Results

2–band BP modulator

Red → Spectrum with random signal.

Black → Spectrum without random signal.

4–band BP modulator
Second-order BP case

SFDR Comparison

Red line ➔ without random signal.
Blue line ➔ with random signal.

- **16-bit**
  - DC Input (Full scale -1~+1)
  - Red line: without random signal.
  - Blue line: with random signal.

- **14-bit**
  - DC Input (Full scale -1~+1)
  - Red line: without random signal.
  - Blue line: with random signal.

- **18-bit**
  - DC Input (Full scale -1~+1)
  - Red line: without random signal.
  - Blue line: with random signal.
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Conclusion

\(< \Delta \Sigma \text{ DA modulator } >\)

**Conventional:** Limit cycle problem for small input

**Proposed:** Using random signal at quantizer input

- Limit cycle reduced
- SFDR much improved
- Overall linearity of \( \Delta \Sigma \) DA modulator maintained.
- Above statements valid for all LP, HP, BP, multi-BP type modulators.
Thanks for listening!