Integral-type Time-to-Digital Converter

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Motivation

TDC Architectures with NO delay lines

• for higher time resolution

• to avoid PVT variations of delay lines:
  – Process
  – Voltage
  – Temperature

Conventional TDC
Outline

• Introduction
• Proposed TDC Architecture and Operation
• Highly Efficient Data Acquisition Condition
• Jitter Effects
• Summary
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Time-to-Digital Converter (TDC):
measures timing difference between two input signals as a digital code
## Comparison

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Conventional TDC</th>
<th>Proposed TDC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay Line</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>PVT Variation</td>
<td>Large</td>
<td>Small</td>
</tr>
<tr>
<td>Self Calibration</td>
<td>Required</td>
<td>Not Required</td>
</tr>
<tr>
<td>Time Resolution</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Measuring Time</td>
<td>Short</td>
<td>Long</td>
</tr>
<tr>
<td>Analog Circuit</td>
<td>NO</td>
<td>YES</td>
</tr>
</tbody>
</table>
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Probabilistic Measurement

Random dots  (Monte Carlo Method)

\[
\frac{N_1}{N_2} \quad \rightarrow \quad \frac{S_1}{S_2}
\]
Proposed TDC Principle (1/3)

Sampling a square wave with **input time difference** $\tau$ / **reference period** $T$ duty cycle

$$\lim_{L \to \infty} \frac{K}{L} = \frac{\tau}{T}$$
Square wave duty cycle depends on input time difference $\tau$
Proposed TDC Principle (3/3)

Acquiring more data improves time resolution
Proposed TDC Architecture

\[
\sin(\omega t + 2\pi/3) + \sin(\omega t + 4\pi/3)
\]

\[
\sin(\omega t) + 2\pi/3 + \sin(\omega t) + 2\pi/3
\]
Output starts to oscillate at **rising edge timing of input** from phase 0

[1] M. Nelson (Tektronics)
Oscilloscope-Trigger Circuit (2/2)

Track mode:

\[ V_{out} = \sin(\omega t + 4\pi/3) \{ \sin \omega t - \sin(\omega t + 2\pi/3) \} + \sin \omega t \{ \sin(\omega t + 2\pi/3) + \sin(\omega t + 4\pi/3) \} + \sin(\omega t + 2\pi/3) \{ \sin(\omega t + 2\pi/3) + \sin(\omega t + 4\pi/3) \} = 0 \]

Hold mode:

\[ V_{out} = \sin(\omega t + 4\pi/3) \{ \sin \omega t_0 - \sin(\omega t_0 + 2\pi/3) \} + \sin \omega t \{ \sin(\omega t_0 + 2\pi/3) + \sin(\omega t_0 + 4\pi/3) \} + \sin(\omega t + 2\pi/3) \{ \sin(\omega t_0 + 2\pi/3) + \sin(\omega t_0 + 4\pi/3) \} = \left( \frac{3\sqrt{3}}{2} \right) \sin(\omega (t - t_0)) \]
Proposed TDC Operation (1/3)

STEP1: Holding the input time difference $\tau$ as phase difference

\[
T = \frac{2\pi}{\omega}
\]

\[
\sin \omega(t - t_0)
\]

\[
\sin \omega((t - t_0) - \tau)
\]
Proposed TDC Operation (2/3)

STEP2: Making the square wave with $\tau / T$ duty cycle
STEP3: Counting the ratio of the sampling points

\[
\tau = \frac{\text{Count I}}{\text{Count II}} T
\]

Proposed TDC Operation (3/3)
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Equivalent-Time Sampling

Measured Wave

Sampling Clock

Reconstructed Waveform

Higher time resolution than sampling clock period
Sampling points must be dispersed uniformly
Data Acquisition Condition

Repetitive Wave

Sampling Clock

\[ T_{\text{CLK}} = ? \times T_{\text{sig}} \]
Waveform Missing Condition

\[ f_{CLK} \gg f_{sin} \quad f_{CLK} \approx \frac{1}{\alpha} f_{sin} \quad (\alpha = 1, \frac{1}{2}, \frac{1}{3}, \frac{2}{3}, \ldots, \frac{1}{6}, \ldots) \quad f_{CLK} \approx f_{sin} \]

Sampling points move little  \(\rightarrow\) Requires long time
Highly Efficient Condition

\[ f_{CLK} = \varphi \times f_{sig} \]

\( \varphi \) : Golden ratio ( \( = 1.6180339887 \ldots \) )

Sampling points are dispersed uniformly through measurement
Golden Ratio Sampling

All sections are divided by golden ratio

Max / Min distances = $\phi$ or $\phi^2$ const.
Max & Min distances between neighbor points vs. Total Number of Data

Max & Min distances decreases $\times 1/\Phi$ every Fibonacci numbers

$\Rightarrow$ Time resolution improves about $1 / \text{Total Number of data}$
Proposed TDC Data Acquisition

\[
sin \omega t \quad sin(\omega t + 2\pi/3) \quad sin(\omega t + 4\pi/3)
\]

CLK

START

STOP

\[
\frac{T}{\varphi (Golden\ ratio)}
\]

\[
T
\]

\[
\tau
\]

Unknown Time

Controllable Frequency

Reference Period

\[
tau
\]

EN

Counter I

To CPU

EN

Counter II

To CPU

input

output

input

CLK

CLK

input

output

input

output
Simulation Result

Acquiring more data improves time resolution

\[ n = 64 \]

\[ RMS = 4.6550275 \text{ [LSB]} \]

Approximate Curve

\[ y = 192.67429 \times ^{-0.9201173} \]
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Jitter Effects

The figure illustrates a circuit diagram with triggers and counters, labeled as follows:

- **CLK**: Clock input
- **START** and **STOP**: Control signals
- **Trigger** blocks with inputs as sin(\(\omega t\)) and sin(\(\omega t + 2\pi/3\))
- **Counter I** and **Counter II**: Output signals to CPU

The equations for the signals are:

\[ \sin(\omega t) + \sin(\omega t + 2\pi/3) + \sin(\omega t + 4\pi/3) \]

The jitter of \(w1\) & \(w2\) affects the period and duty of \(D1 \cdot \overline{D2}\).

The period \(T\) is shown as the time between consecutive ticks of the \(D1 \cdot \overline{D2}\) signal.

Jitter in \(w1\) and \(w2\) impacts the consistency of the \(D1 \cdot \overline{D2}\) output, indicating a potential issue with synchronization or timing accuracy in the system.
Maximum Error vs. Total Number of Data

- Red: No Jitter
- Green: Random Jitter
- Blue: Accumulated Jitter
Simulation Result (2/2)

Maximum Error vs. Total Number of Data

![Graph showing maximum error vs. total number of data with lines for No Jitter, Common Accumulated Jitter, and Differential Accumulated Jitter.](image)
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- Proposed integral-type TDC:
  - fine time resolution
  - no need for calibration

- Highly Efficient Data Acquisition Condition:
  - Sampling clock frequency / measured signal frequency = Golden ratio

- Robust for jitter
Appendix
Deterministic Measurement

\[ T_{CLK} = \frac{Q}{P} \times T_{sig} \quad (P, Q: \text{integers and relatively prime}) \]

**Q**: Phase distance for each sampling

**P**: Maximum number of total measurable sampling points
Golden Ratio

\[ \varphi \equiv \frac{a + b}{a} = \frac{a}{b} \]

\[ \varphi = \frac{1 + \sqrt{5}}{2} = 1.6180339887 \ldots \]
Fibonacci Number

\[ F_0 = 0 \]
\[ F_1 = 1 \]
\[ F_{n+2} = F_n + F_{n+1} \]

0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, \ldots

\[ \lim_{n \to \infty} \frac{F_n}{F_{n-1}} = 1.6180339887 \ldots = \varphi \]