ICSICT-2018
2018 IEEE 14th International Conference on Solid-State and Integrated Circuit Technology

Silicon Verification of Improved Nagata Current Mirrors

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ASO Inc.
Gunma University

Outline

- Research Background
- Nagata current mirror circuit
- Improved circuit
- Design guideline
- Design & implementation
- Measurement
- Evaluation
- Conclusion

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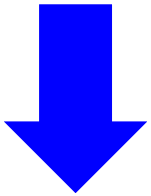
Research Background

Most analog ICs require

Reference current / voltage source



Stable against PVT variation

P : Process
V : Supply voltage
T : Temperature

Nagata current mirror

- ✔ Simple
- ✔ Constant current for voltage variations
- ✔ Widely used in analog ICs

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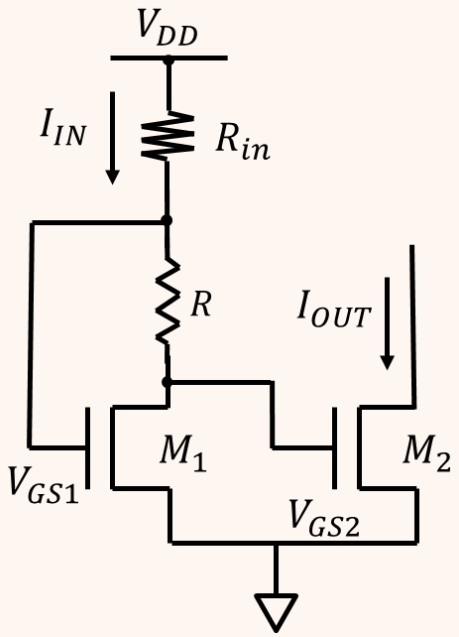
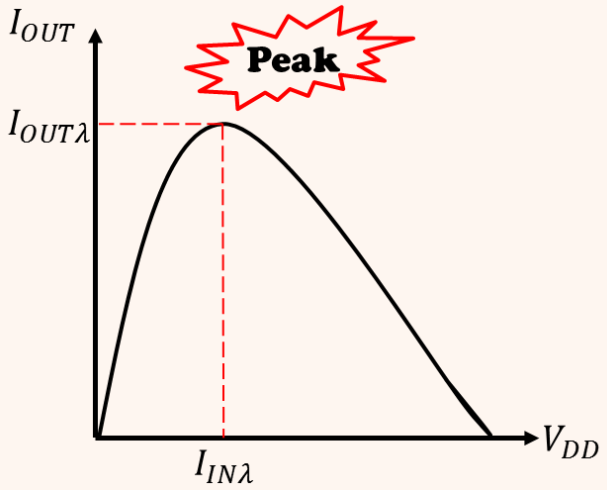
Original Nagata Current Mirror



MOS Nagata
Current Mirror Circuit



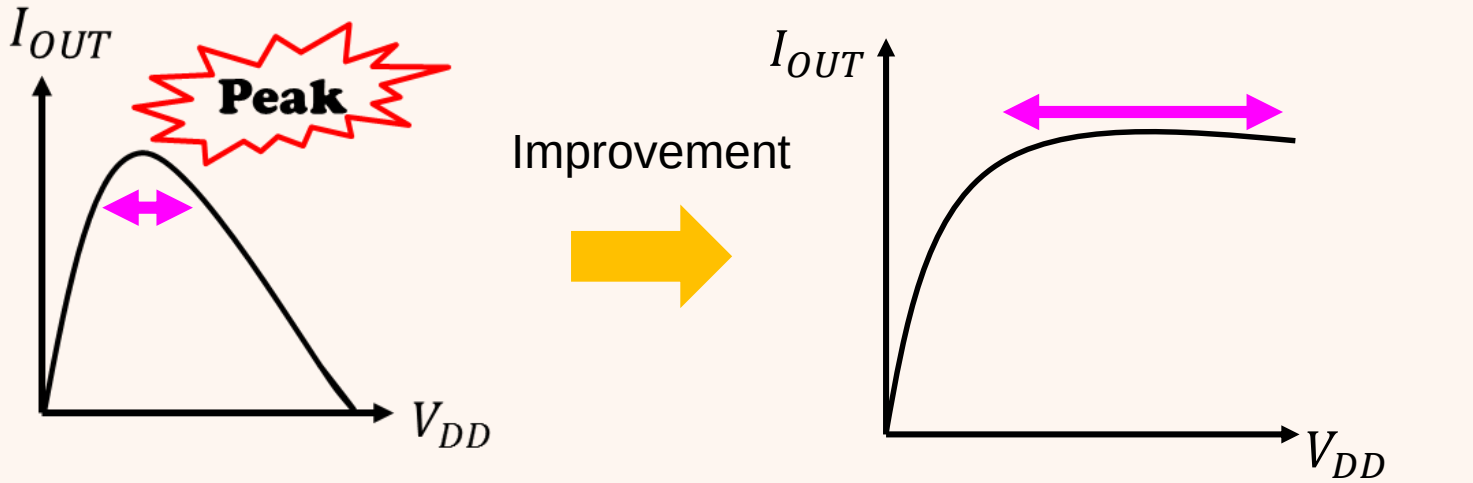
Peaking current
characteristics

$$I_{IN\lambda} = \frac{1}{4R^2K_1(1+\lambda V_{DS1})} \cdot I_{OUT\lambda} = \frac{(W/L)_2}{4(W/L)_1} \cdot I_{IN}(1+\lambda V_{DS2})$$

Reserch Objective

Improved point

Peak vicinity is narrow ➡ Wider



Peaking current characteristics

Peaking current characteristics of improved circuit

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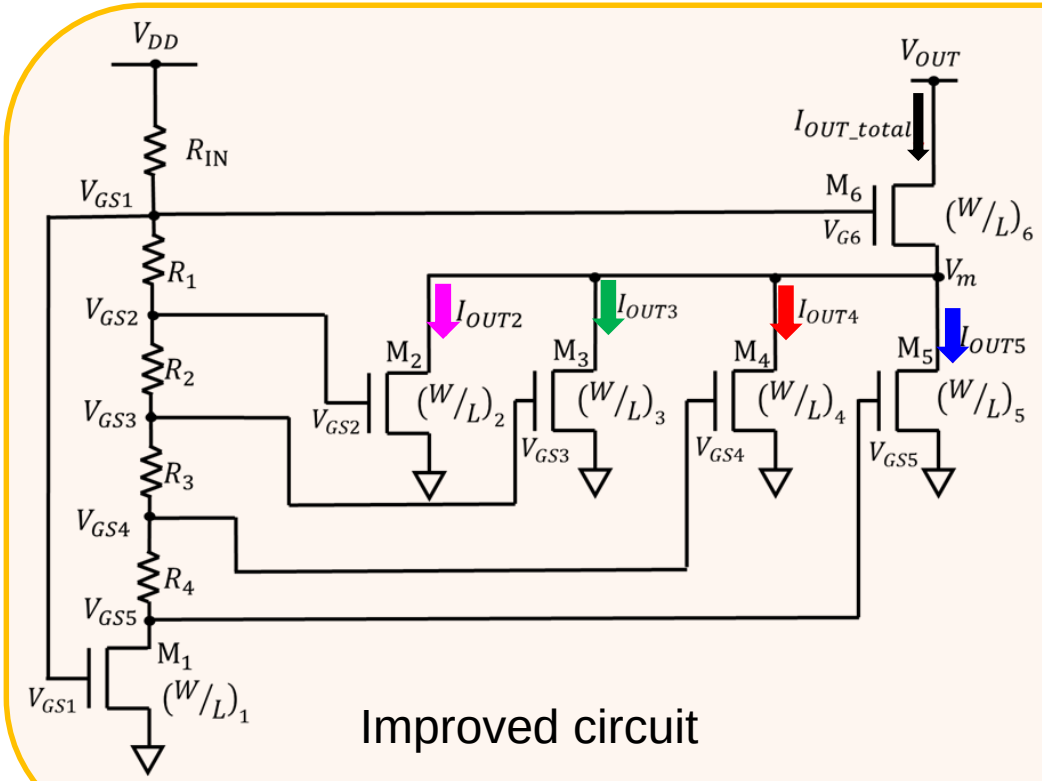
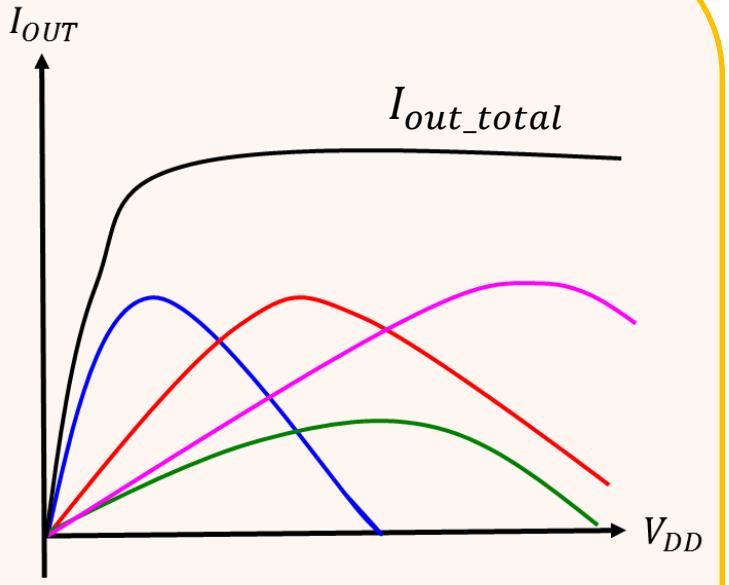
Overview of Improved Circuit



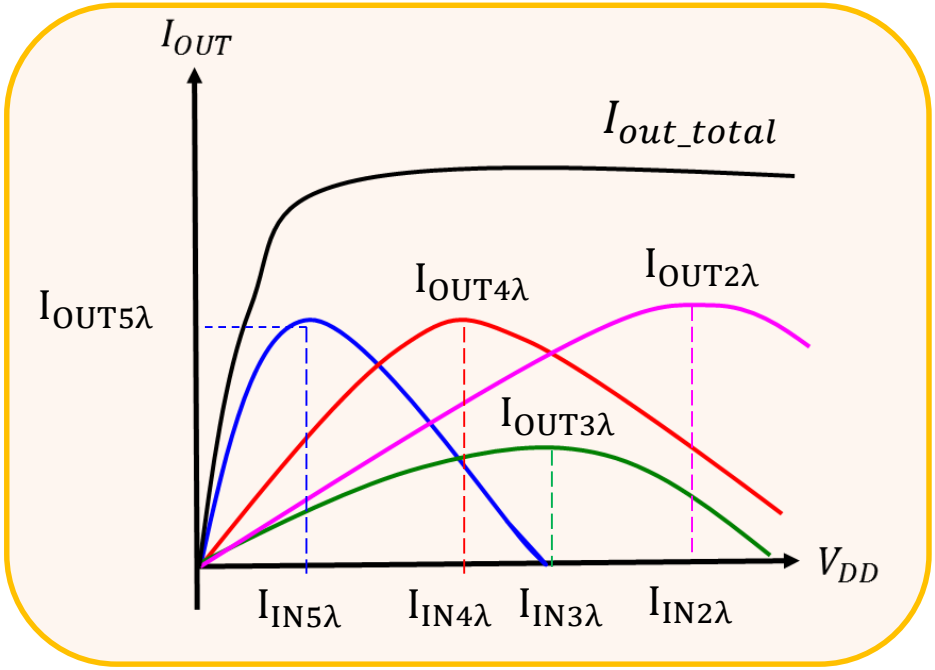
Improved circuit



Peaking current characteristics of improved circuit

- ✔ Simple design
- ✔ Using multiple current mirror circuit
- ✔ Different current peaks

Theoretical Formula



Current equation of improved circuit

$$I_{INn\lambda} = \frac{1}{4R'^{2}_{n-1}K_1(1+\lambda V_{DS1})}$$

$$I_{OUTn\lambda} = \frac{(W/L)_n}{(W/L)_1} I_{INn\lambda}(1+\lambda V_{DSn})$$

$$(n = 2,3,4,5 \quad R'_{n-1} = R_1 + R_2 + \cdots + R_{n-1})$$

Condition for saturation region expression

$$R'_{n-1} < \frac{V_{TH}}{I_{IN}}$$

$$V_{OUT} > V_{DD} - R\,I_{IN} - V_{TH}$$

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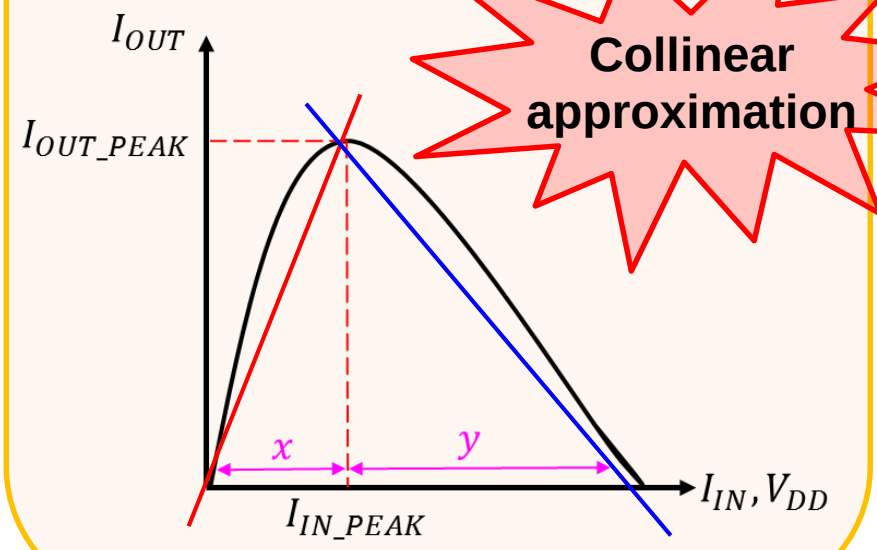
Analysis of Peak Characteristics

Attention peak characteristics



Collinear approximation

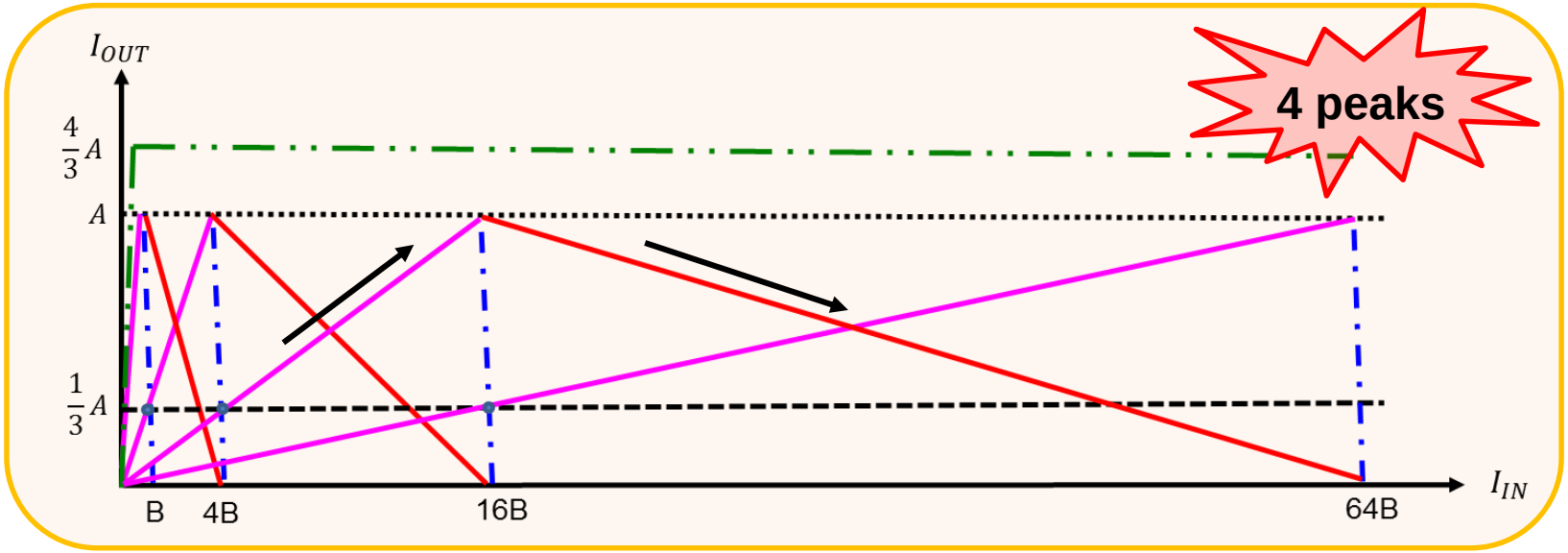
- $x = 0 \sim I_{IN\_PEAK} = \frac{1}{4R^2K_1}$
- $y = I_{IN\_PEAK} \sim I'_{IN} = I'_{IN} - x = \frac{1}{R^2K_1} - \frac{1}{4R^2K_1} = 3x$

$x : y = 1 : 3$

Establish design guideline using this ratio

Overview of Design Guideline

Current decrease ↘ = increase ↗



Design process

- ✔ Determine $I_{OUT} = A$
- ✔ Determine I_{IN} of each peak
  - ➡ Using the ratio ($x : y = 1 : 3$)
- ✔ Derive R, R_{IN}, L , W from theoretical formula

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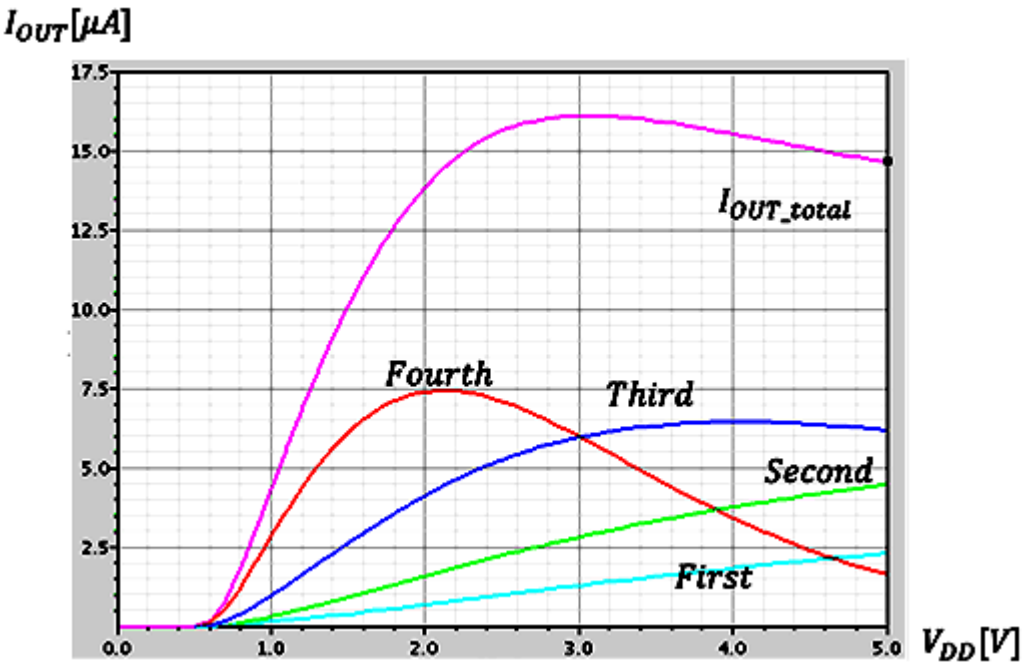
Parameters by Theoretical Equation

Parameters

$W_1[\mu m]$	1.5
$W_2[\mu m]$	0.42
$W_3[\mu m]$	1.7
$W_4[\mu m]$	6.8
$W_5[\mu m]$	27.1
$W_6[\mu m]$	27.1

$R_1[k\Omega]$	3.3
$R_2[k\Omega]$	3.3
$R_3[k\Omega]$	6.5
$R_4[k\Omega]$	13.2
$R_{IN}[k\Omega]$	400

$L = 0.35[\mu m]$ in all cases



SPICE simulation result

Error by linear approximation and MOS model

→ Fine adjustment

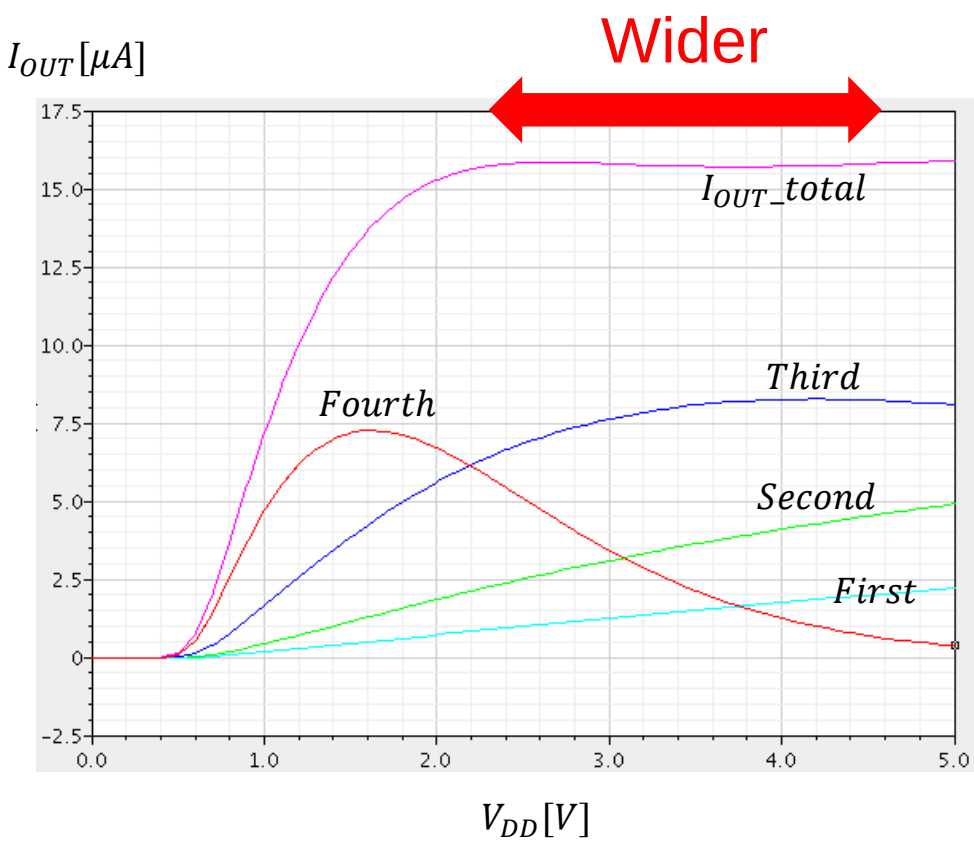
Adjusted Parameters

Adjusted parameters

$W_1[\mu m]$	1.5
$W_2[\mu m]$	0.42
$W_3[\mu m]$	1.7
$W_4[\mu m]$	6.8
$W_5[\mu m]$	25.5
$W_6[\mu m]$	25.5

$R_1[k\Omega]$	3.2
$R_2[k\Omega]$	3.2
$R_3[k\Omega]$	6.4
$R_4[k\Omega]$	22.4
$R_{IN}[k\Omega]$	400

$L = 0.35[\mu m]$ in all cases



SPICE simulation result

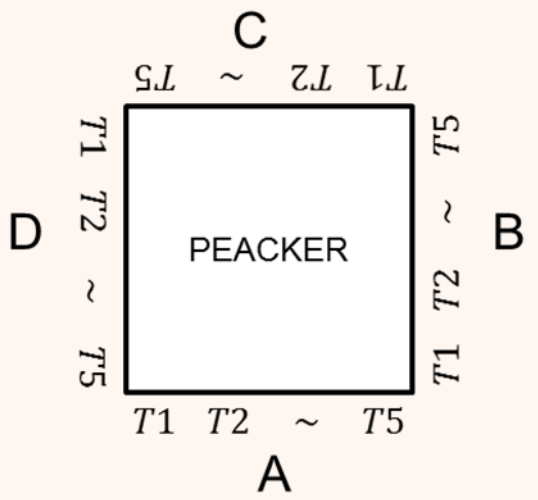
Fabricated Chip

Fabricated circuit parameters TSMC $0.35\mu m$ CMOS

Circuit Type	T1	T2	T3	T4	T5
# of peaks	4	4	4	3	4
(W/L)	$(W/L)_{T1}$	$1.5 \times (W/L)_{T1}$	$2 \times (W/L)_{T1}$	$(W/L)_{T4}$	$(W/L)_{T5}$
R	R'_{n-1T1}	R'_{n-1T1}	R'_{n-1T1}	R'_{n-1T4}	R'_{n-1T5}

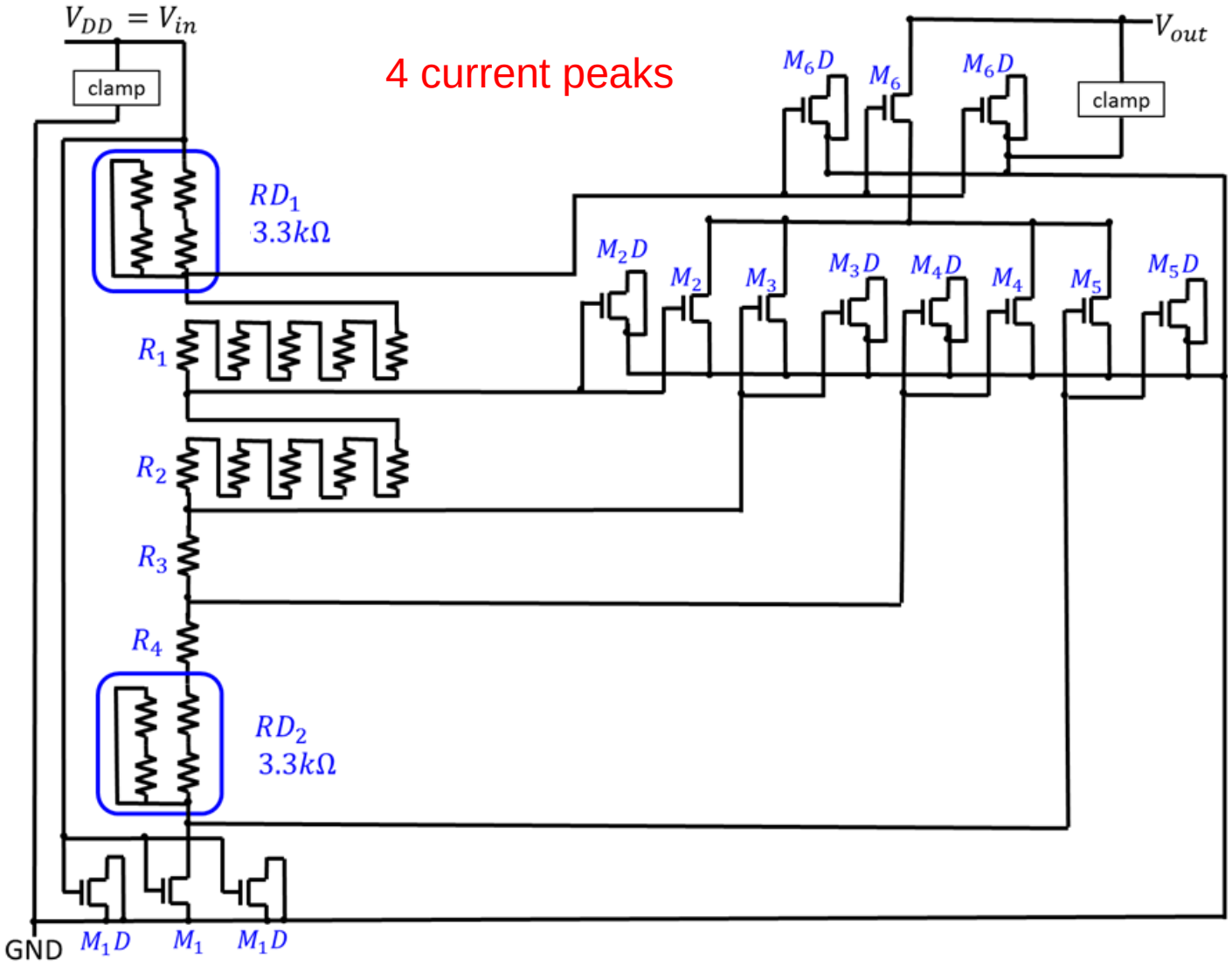
- ✔ 5 chips (#1,…,#5)
- ✔ 4 sets (A,…,D) per one chip
- ✔ 5 circuit (T1,…,T5) per one side

20 samples per circuit type
4 (A,…,D) x 5(#1,…,#5)



Fabricated chip

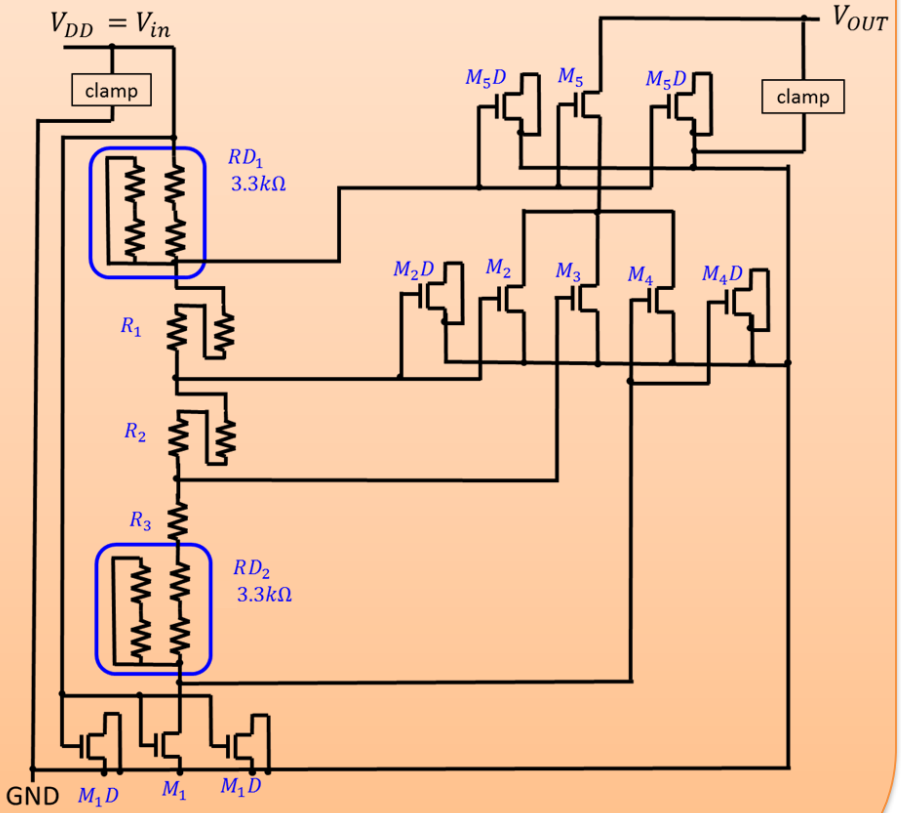
Circuit Diagram of T1/T2/T3



Circuit Diagram of T4 & T5

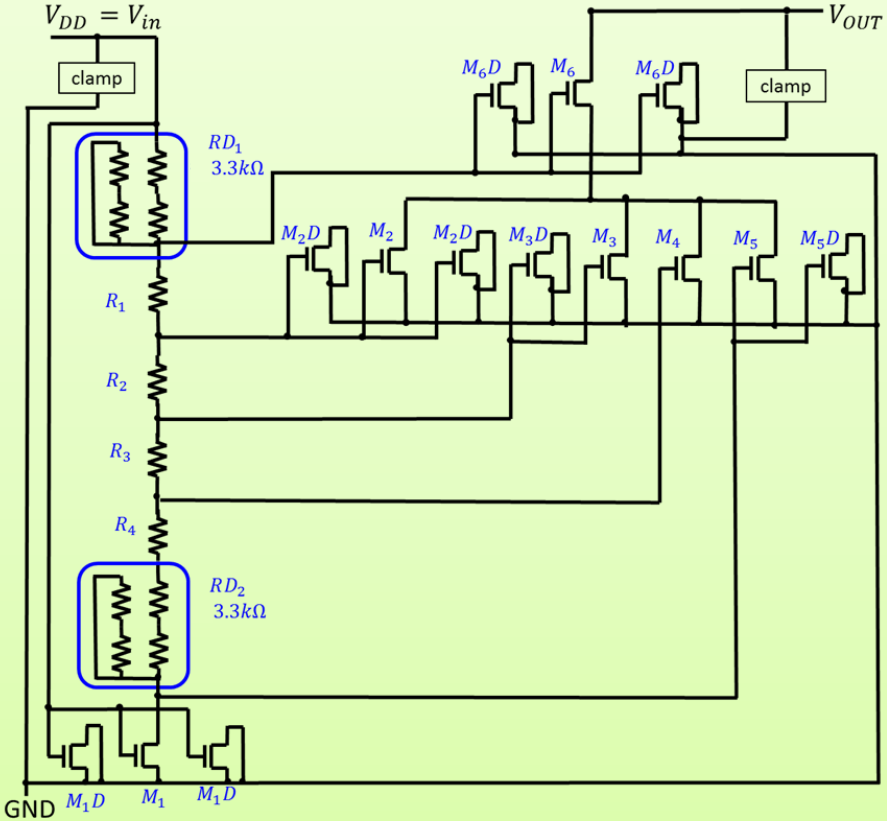
T4

3 current peaks



T5

5 current peaks



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Measurement Method

- ✔ Output voltage $V_{OUT} = 1V, 2V, 3V$
- ✔ Input voltage $V_{IN} = 0 \sim 5.0\ V$

→ Measured the total output current I_{OUT}

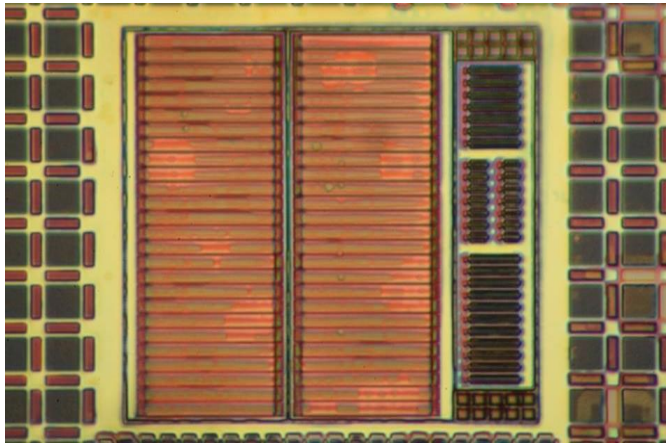
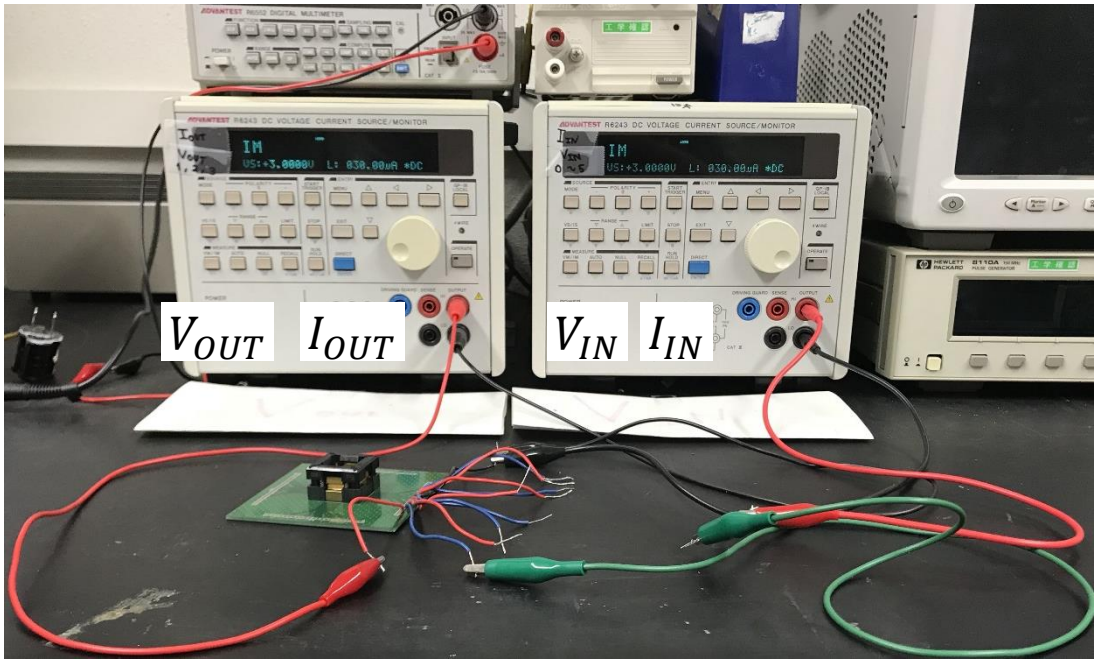
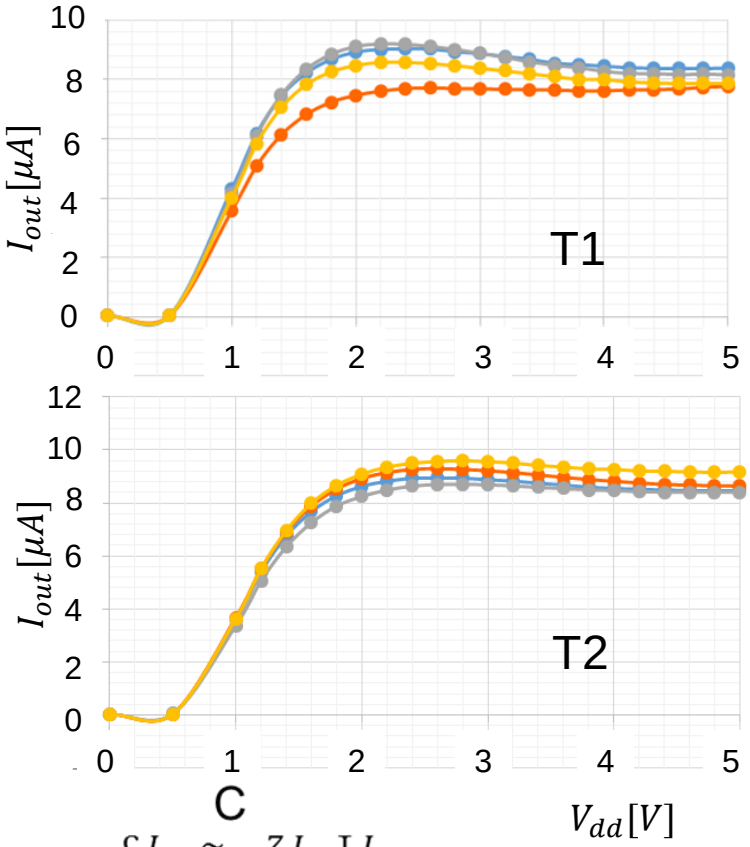


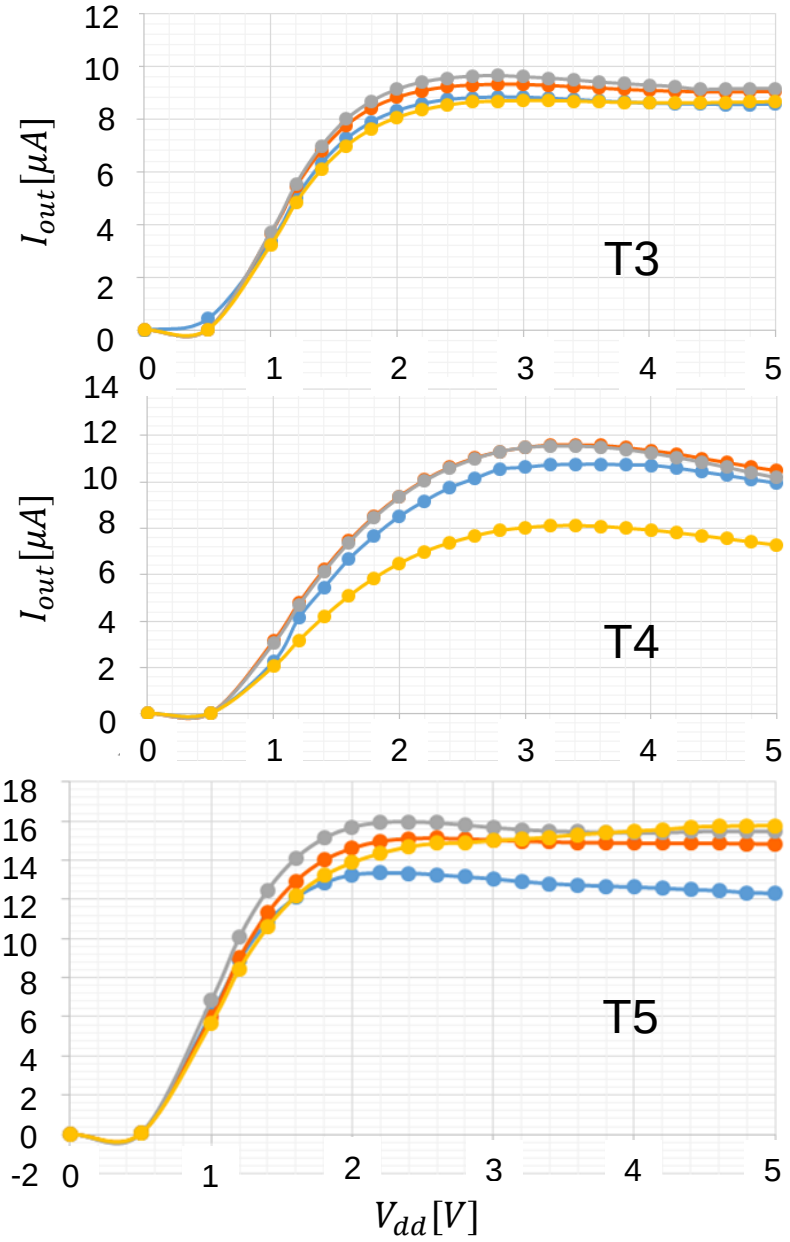
Photo of prototype chip

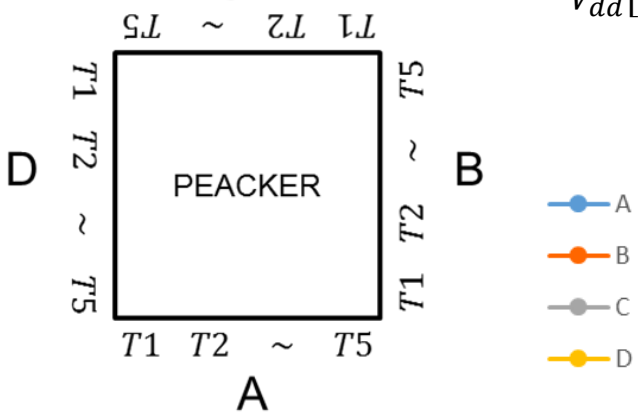


Measurement environment

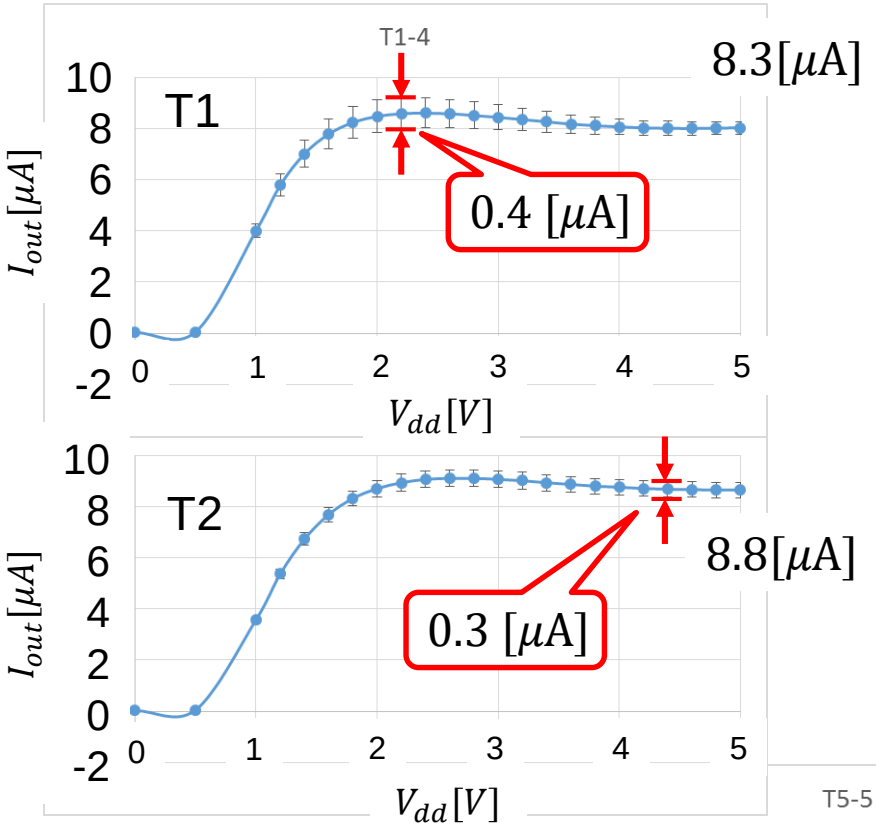
I_{OUT} Measurement Results (#1) $V_{OUT} = 3V$

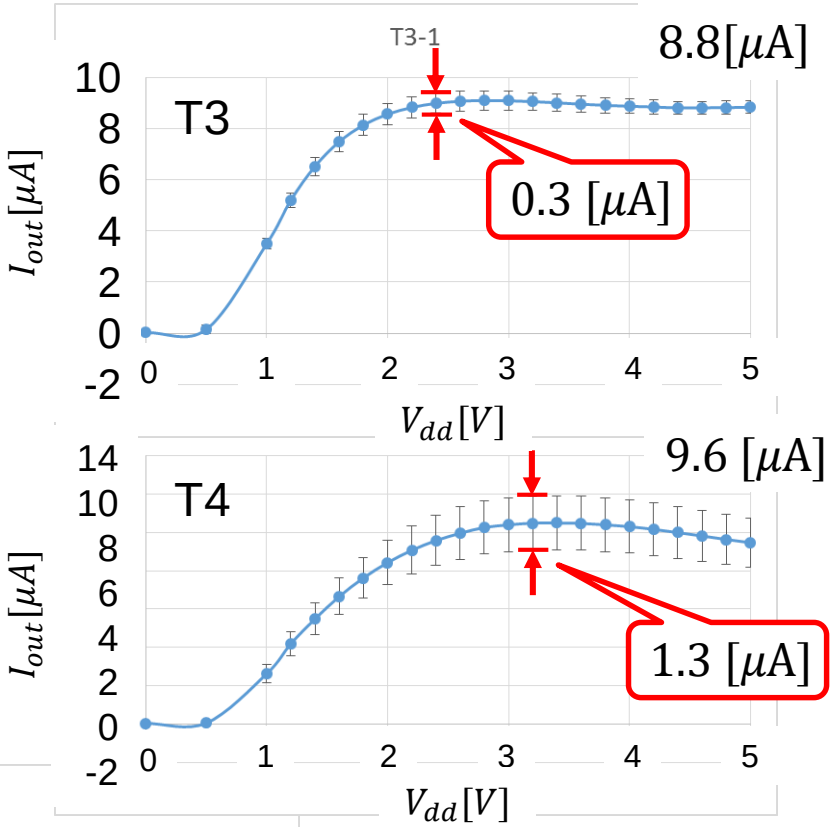


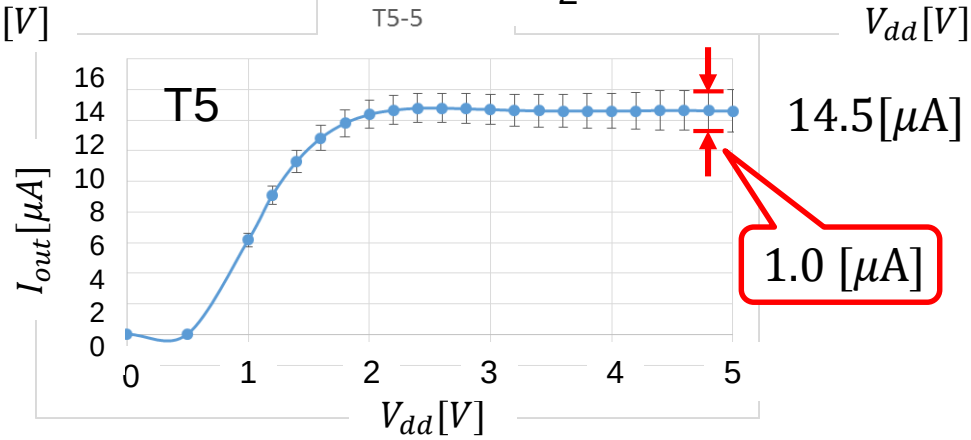




Standard Deviation of I_{OUT} (#1)

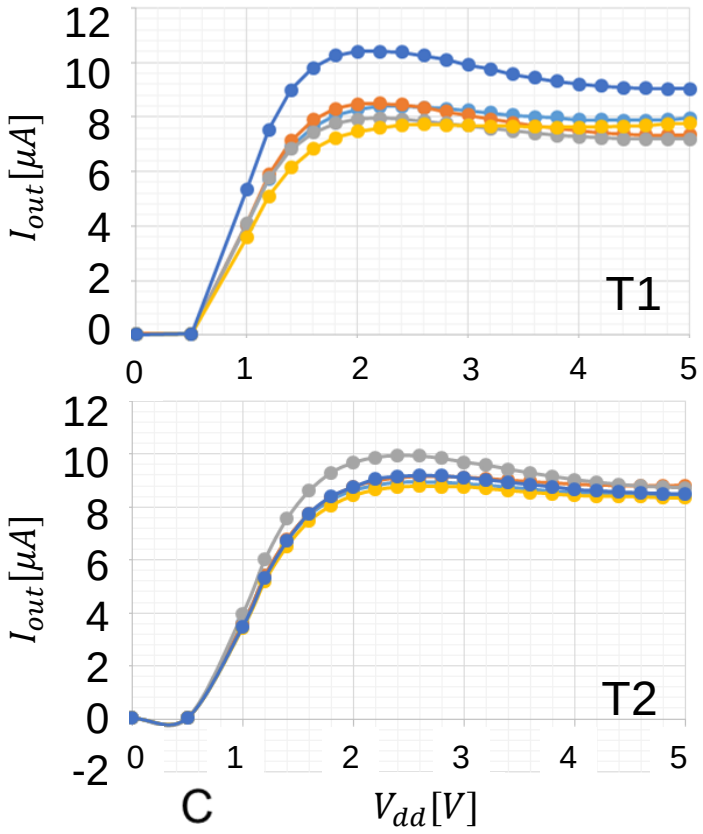


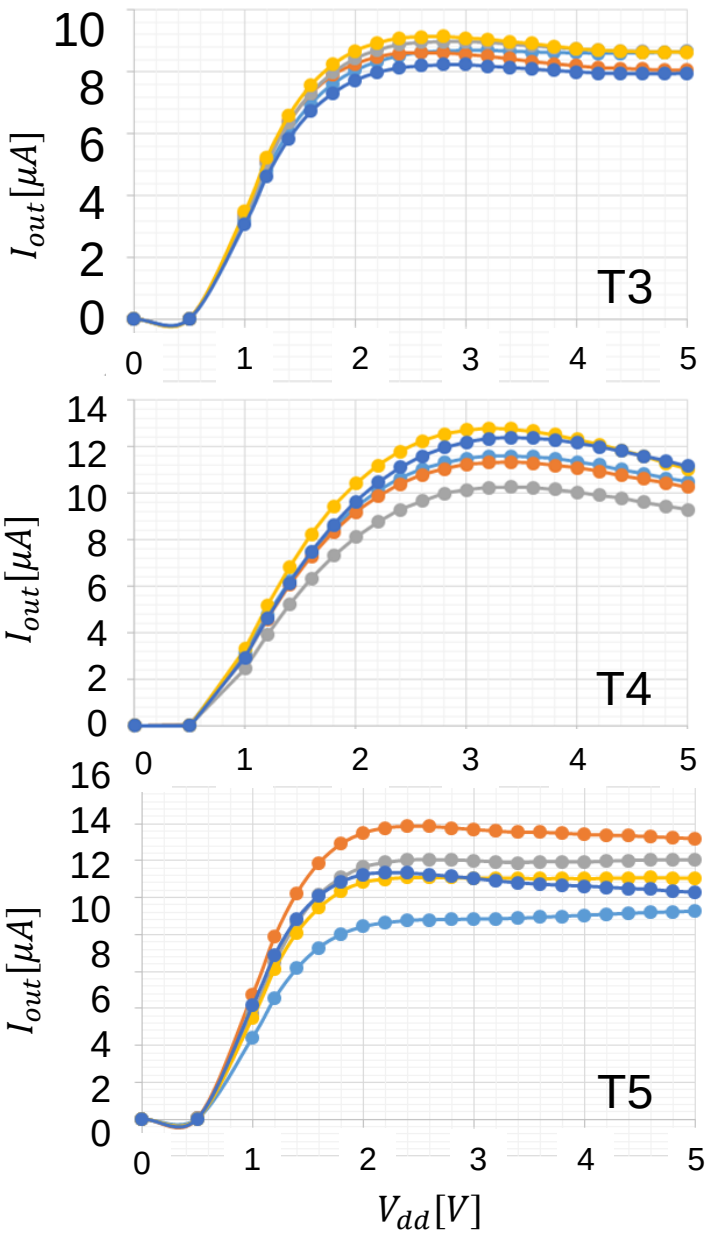


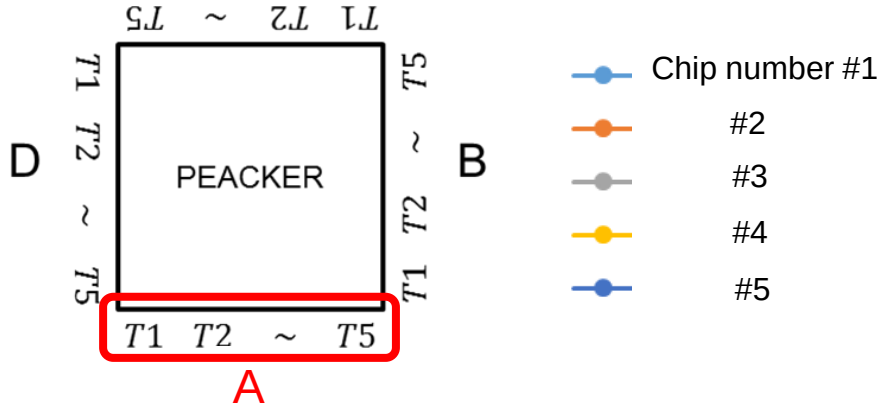


I_{OUT} Measurement Results (Side A)

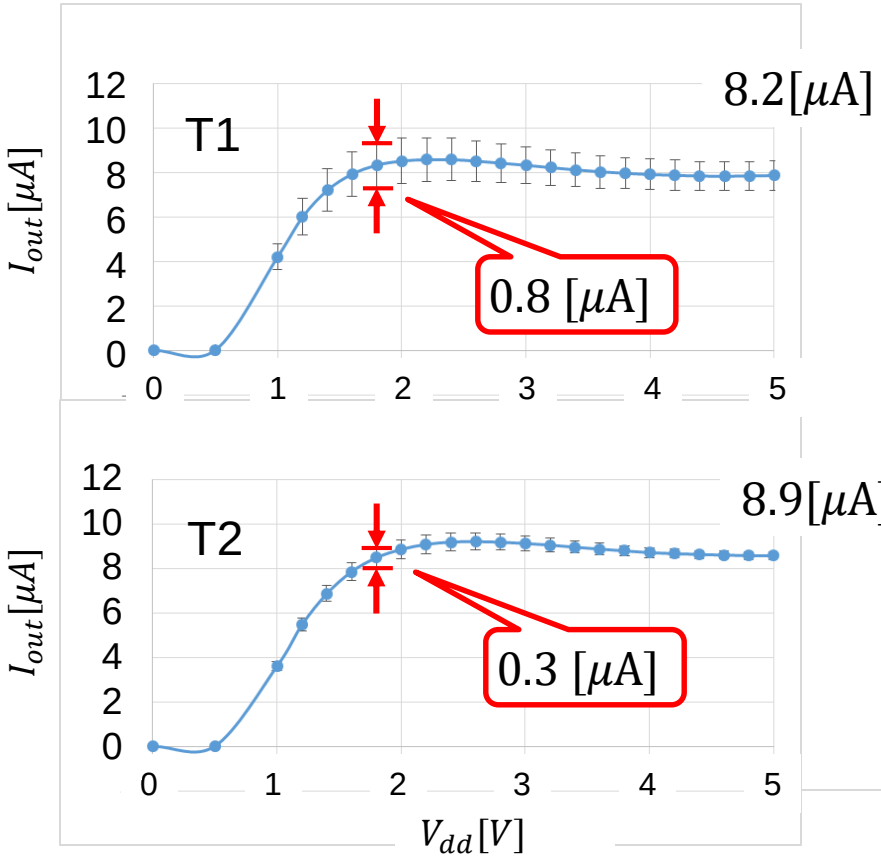
$V_{OUT} = 3V$

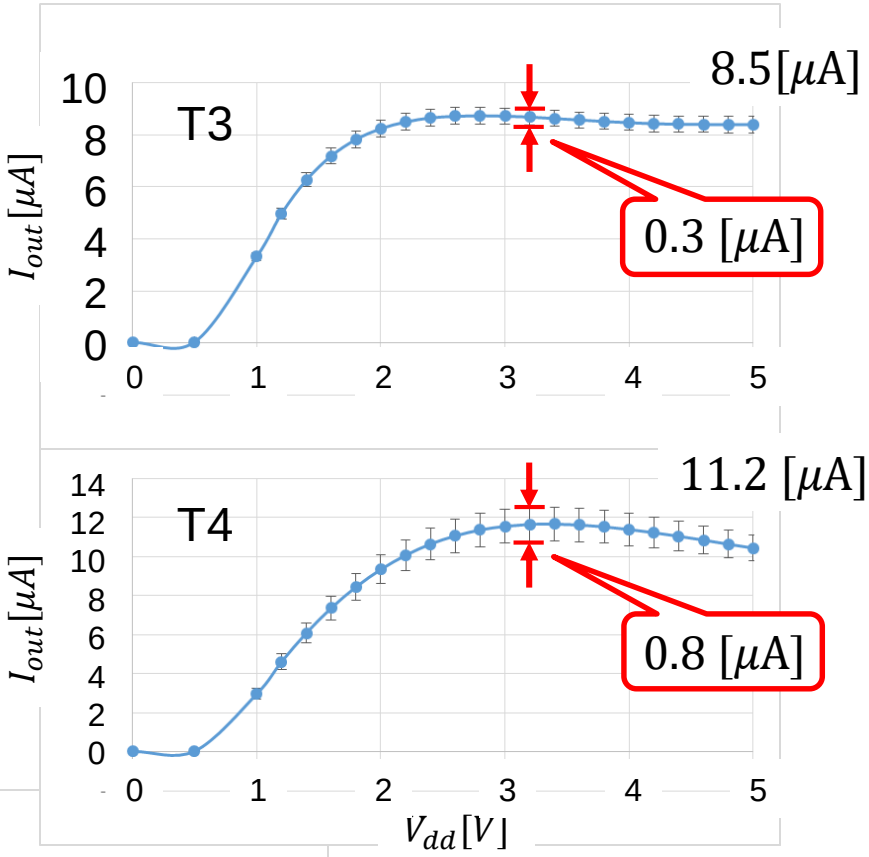


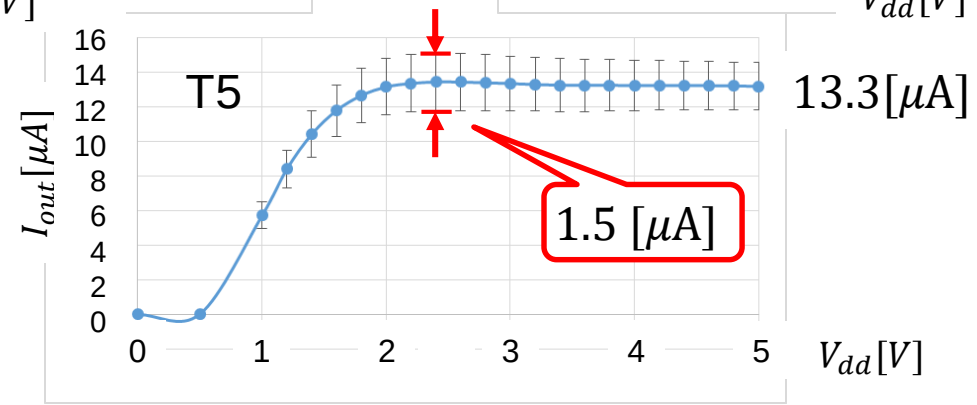




Standard Deviation of I_{OUT} (Side A)

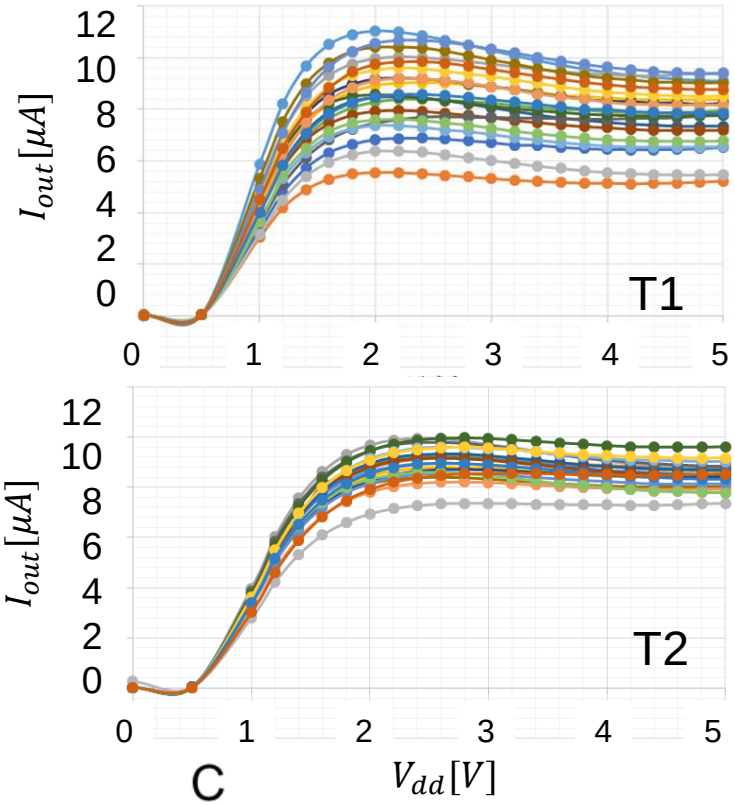


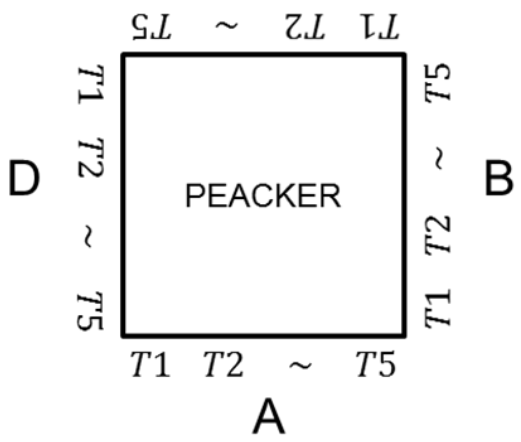


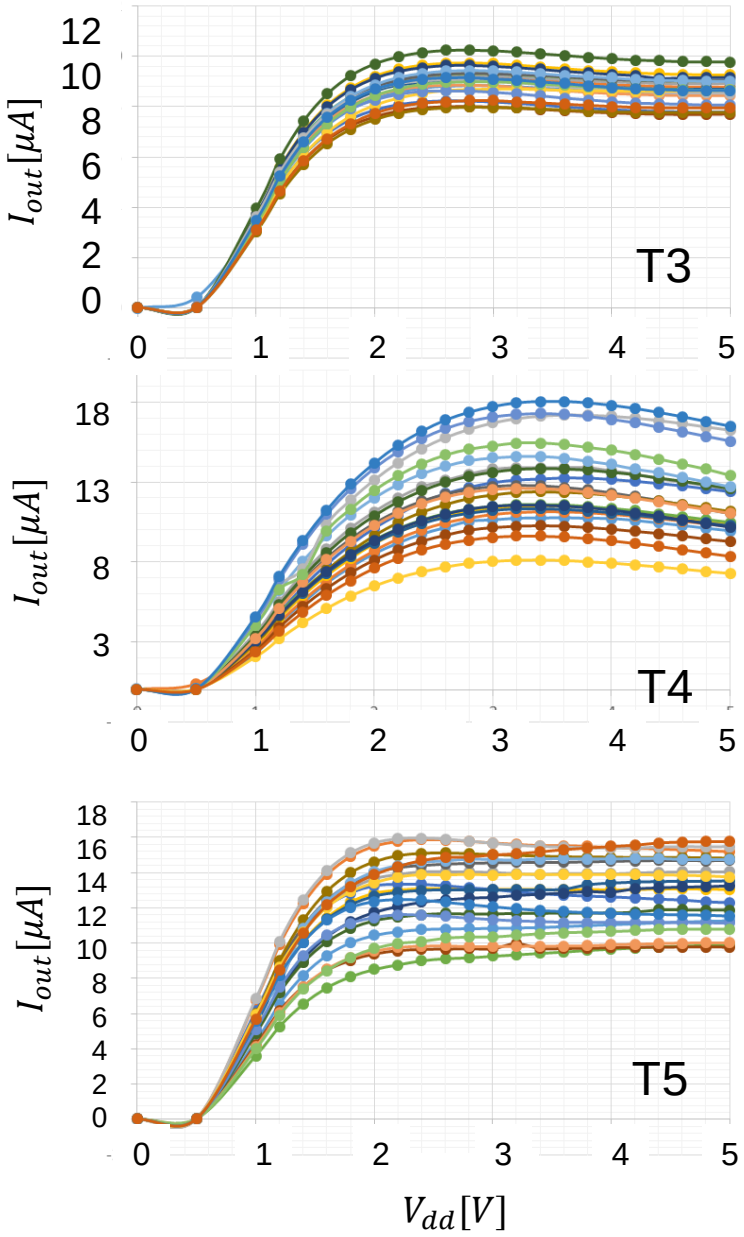


Comparison with All Data

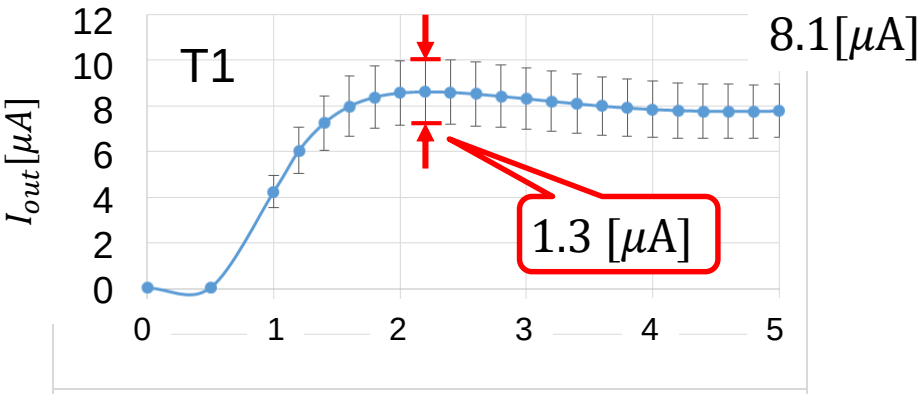
$V_{OUT} = 3V$

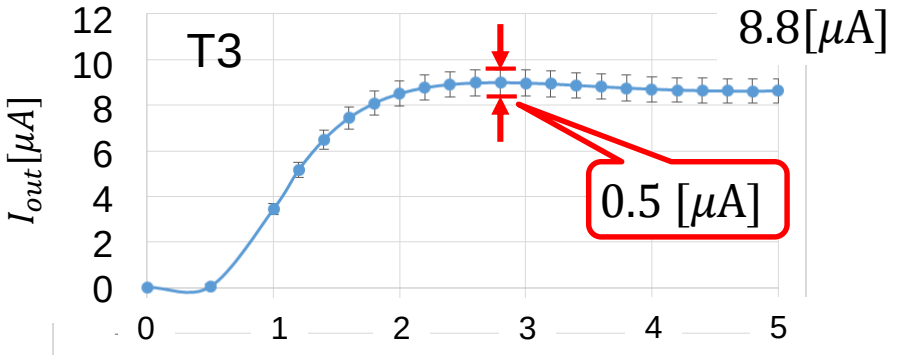


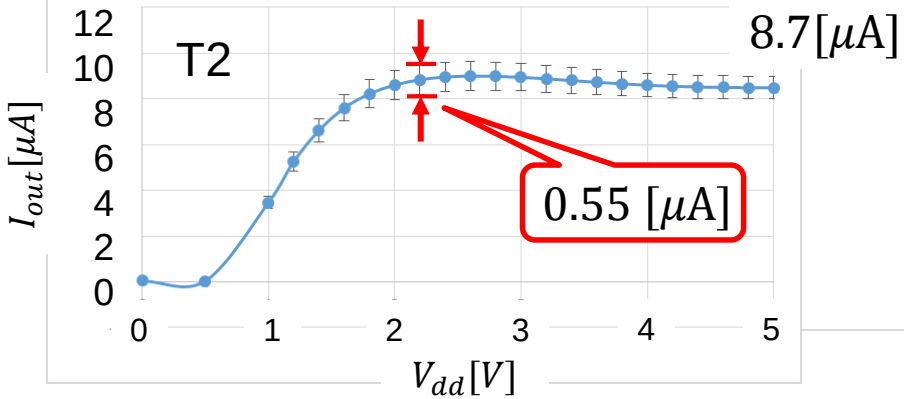


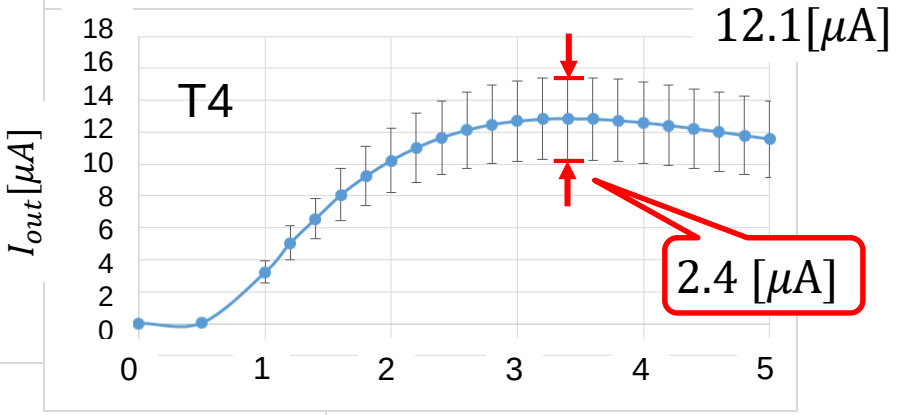


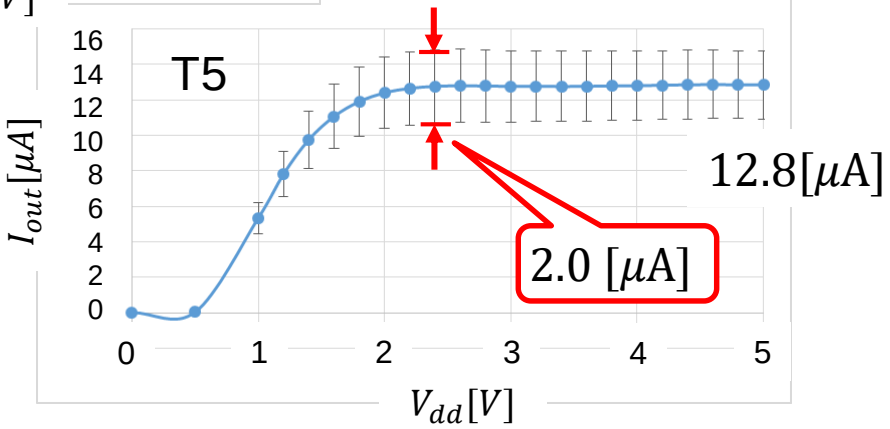
Standard Deviation of All Data



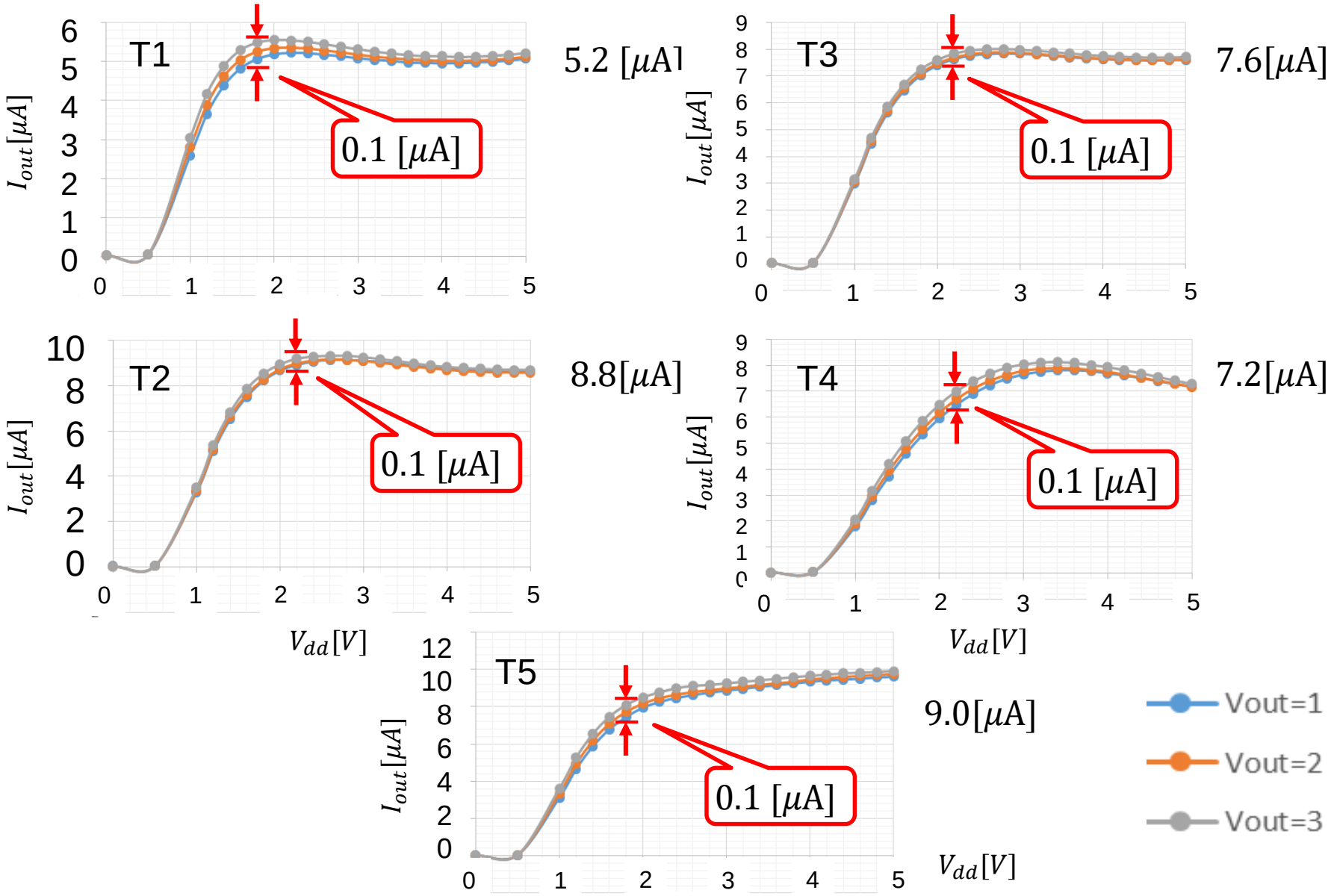








Effect of Output Voltage on I_{OUT}



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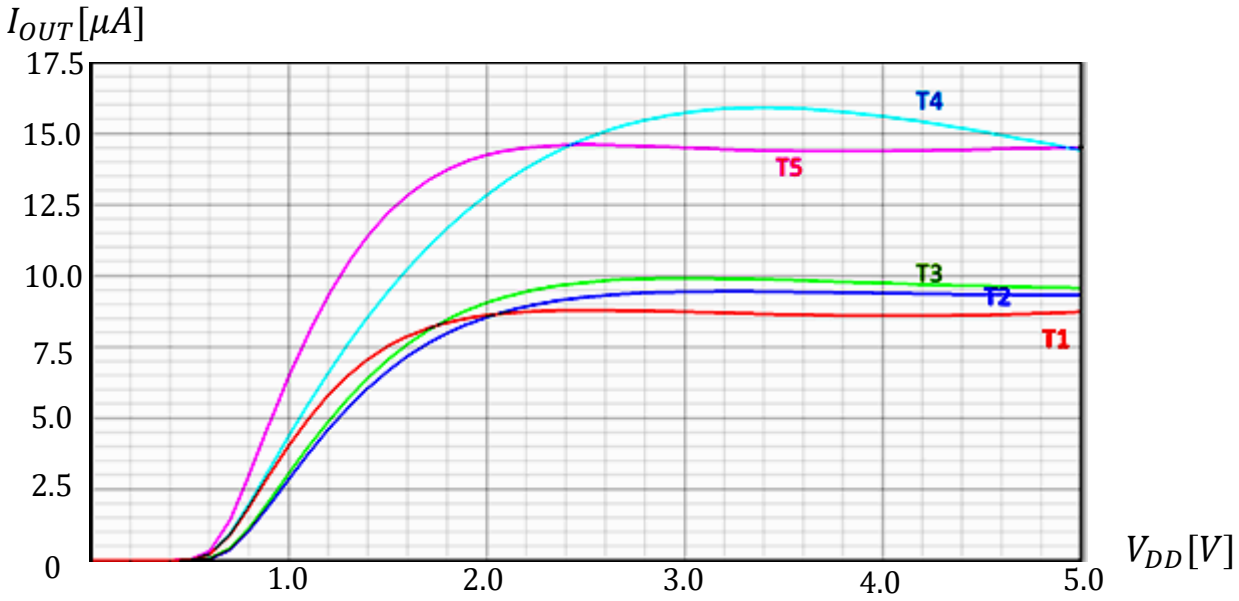
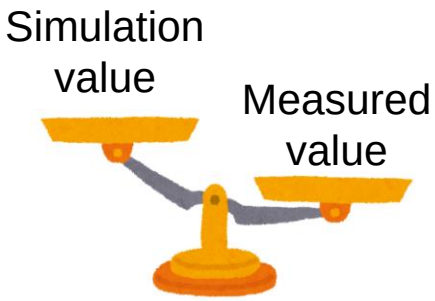
Comparison of Measurement & Simulation

Circuit Type	T1	T2	T3	T4	T5
Measured value [μA]	8.1	8.7	8.8	12.4	12.8
Simulation value [μA]	8.7	9.3	9.8	15.2	14.6



Simulation results of 5 circuits

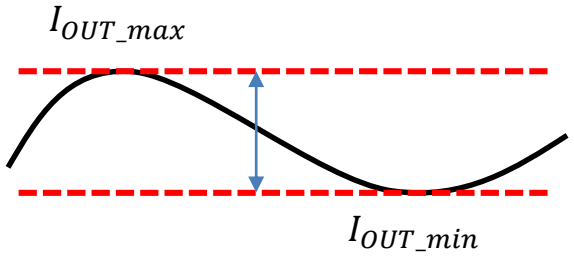


About 5～15%

Effect of process variation from typical process condition

Average Variation of I_{OUT} Over I_{IN}

$$Variation = \left[\frac{I_{OUT\_max} - I_{OUT\_min}}{(I_{OUT\_max} + I_{OUT\_min})/2}\right] \times 100[\%]$$



Circuit Type	T1	T2	T3	T4	T5
Variation [%]	2.9	1.7	1.5	5.7	1.6

Variation of T4 is the worst

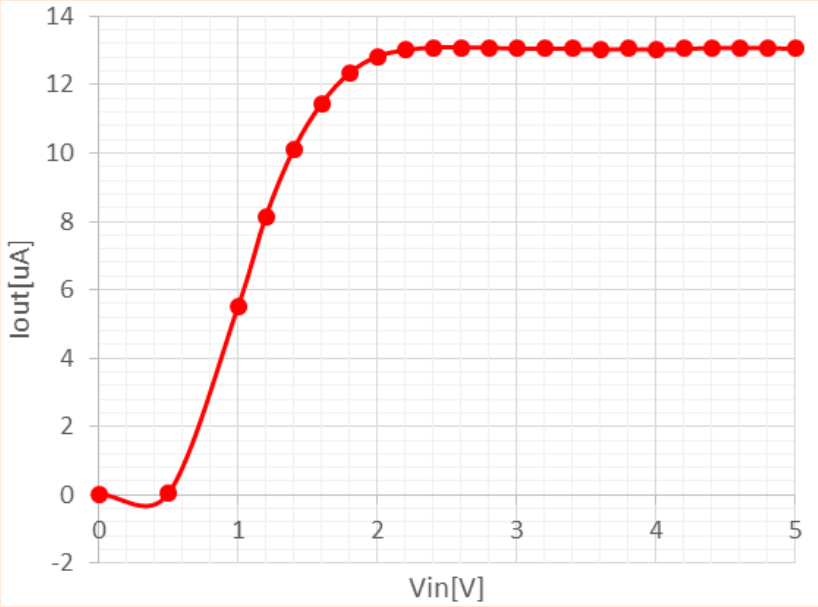
Number of peaks is 3 in T4

Larger number of peaks ⇨ more stable I_{OUT}

Minimum Variation of I_{OUT} Over I_{IN}

Circuit Type	T1	T2	T3	T4	T5
Variation [%]	1.9	1.1	1.2	4.9	0.5

Measurement result



I_{OUT} in minimum variation

I_{OUT} is constant for supply voltage variation

Number of peaks in design freedom

➡ Suppress variation

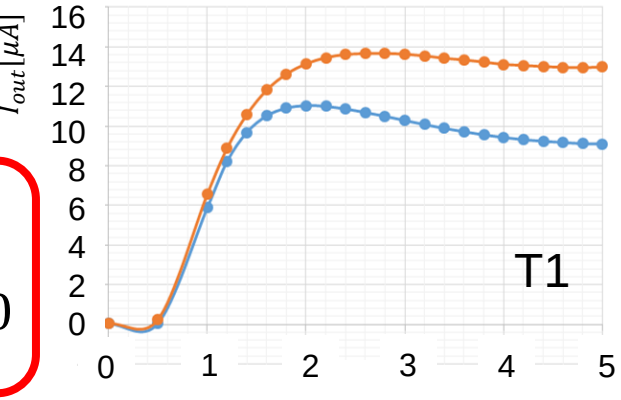
Temperature Characteristics

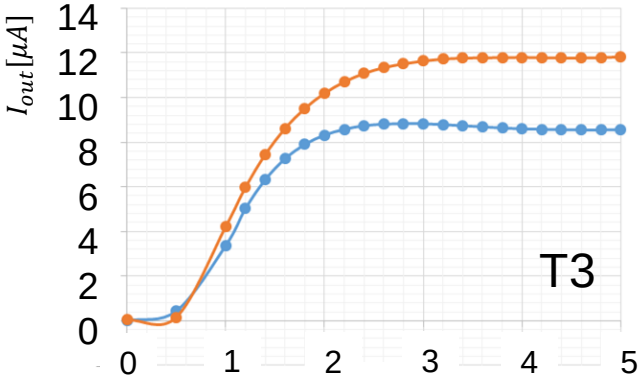
$$Variation = \frac{I_{OUT\_h} - I_{OUT\_r}}{I_{OUT\_r}} \times 100$$

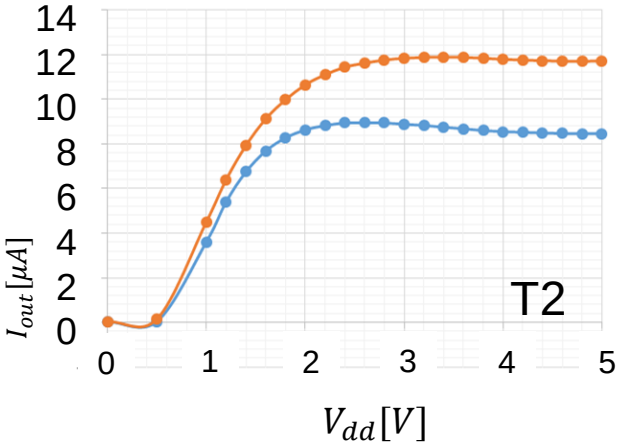
Room temperature

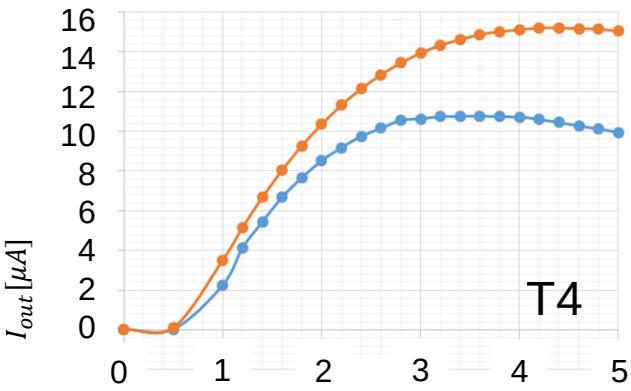
High temperature

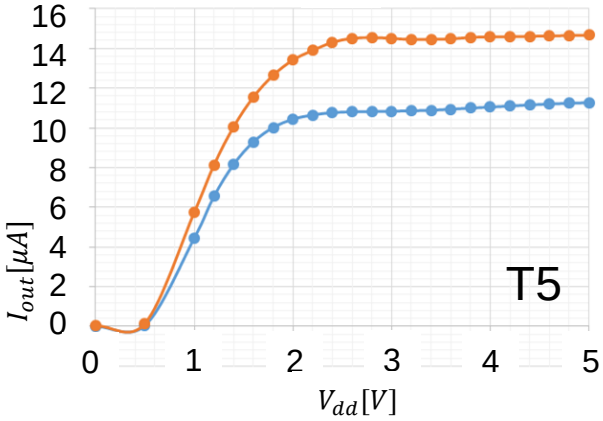
Use a hair dryer











Circuit Type	T1	T2	T3	T4	T5
Room temp.[μA]	10.0	8.7	8.6	10.2	10.9
High temp. [μA]	13.2	11.6	11.5	14.0	14.4
Variation [%]	32	33	34	37	32

Outline

- Research Background
- Nagata current mirror circuit
- Improved circuit
- Design guideline
- Design & implementation
- Measurement
- Evaluation
- Conclusion

Conclusion

- ✔ Proposal of MOS reference current sources
  - ➡ Realized by addition of multiple current peaks
- ✔ Design guidelines of proposed circuits
- ✔ SPICE simulation results
- ✔ Measurement & valuation of prototype circuits

Proposed circuits

- ✔ Simple
- ✔ Fairly stable current reference
- ✔ insensitive to wide range of power supply voltage variation