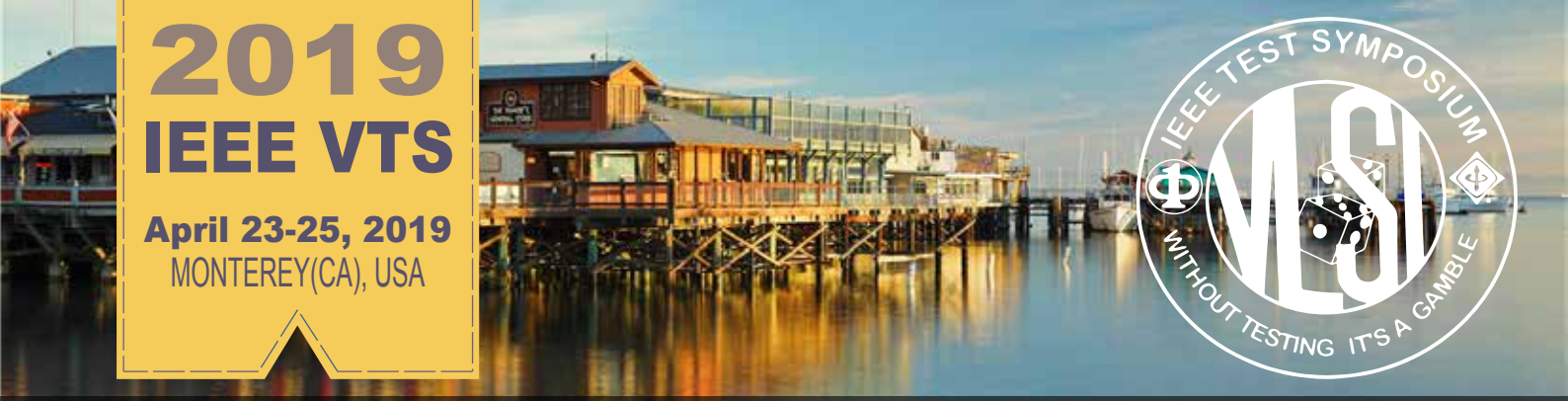

2019 IEEE VTS

April 23-25, 2019
MONTEREY(CA), USA

IEEE TEST SYMPOSIUM
VLSI
WITHOUT TESTING IT'S A GAMBLE

TEST RELIABILITY AND SECURITY CHALLENGES IN VLSI SYSTEMS

CALL FOR PAPERS

The IEEE VLSI Test Symposium (VTS) explores emerging trends and novel concepts in testing, reliability and security of microelectronic circuits and systems. The VTS Program Committee invites original, unpublished **paper submissions** for VTS 2019. Proposals for the **innovative practices** and special **sessions tracks** are also invited.

Major topics include but are not limited to:

- Analog/Mixed-Signal/RF Test
- ATPG & Compression
- Silicon Debug
- Automotive Test & Safety
- Built-In Self-Test (BIST)
- Defect & Current Based Test
- Defect/Fault Tolerance
- Delay & Performance Test
- Design for Testability (DFT)
- Design Verification/Validation
- Embedded System & Board Test
- Embedded Test Methods
- Emerging Technologies Test
- FPGA Test
- Fault Modeling and Simulation
- Hardware Security
- Low-Power IC Test
- Microsystems/MEMS/Sensors Test
- Memory Test and Repair
- On-Line Test & Error Correction
- Power/Thermal Issues in Test
- System-on-Chip (SOC) Test
- Test Standards
- Test Economics
- Test of Biomedical Devices
- Test of High-Speed I/O
- Test Quality and Reliability
- Test Resource Partitioning
- Transients and Soft Errors
- 2.5D, 3D and SiP Test

New hot topics:

This year VTS puts particular emphasis on enlarging its scope soliciting submissions on testing, reliability and security aspects on the following hot topics: ***approximate computing, neuromorphic computing and quantum computing***

KEY DATES

Oct 05, 2018 - Submission deadline
Dec 09, 2018 - Notifications
Feb 10, 2019 - Camera ready upload

Submissions

6 pages in a standard IEEE two columns format.

Submit at:
http://www.tttc-vts.org

VTS 2019 will present a Best Paper Award, a Best Special Session Award, and a Best Innovative Practices Session Award based on the evaluations of reviewers, attendees, and an invited panel of judges. We also plan to organize various Student Activities including the TTTC Best Doctoral Thesis Contest, details for which will be made available through the VTS website.

The best papers of VTS 2019 will be invited to resubmit to the IEEE Design & Test of Computers where they will undergo a regular, but expedited, review process.

TTTC Test Technology Educational Program (TTEP) tutorials on emerging test technology topics will be offered in conjunction with VTS 2019. Tutorial proposals should be submitted according to TTEP 2019 submission guidelines, which will be posted on http://computer.org/tab/tttc/teg/ttep.

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