

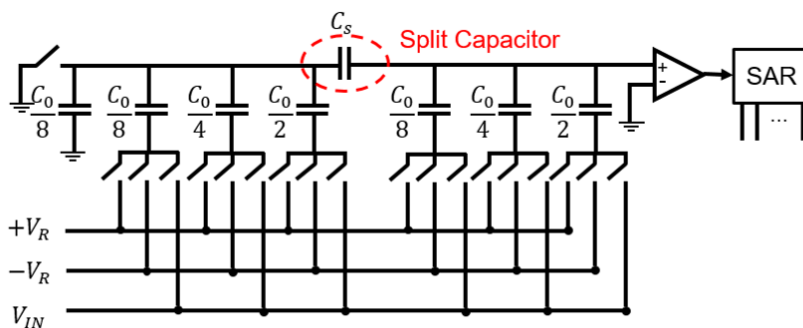
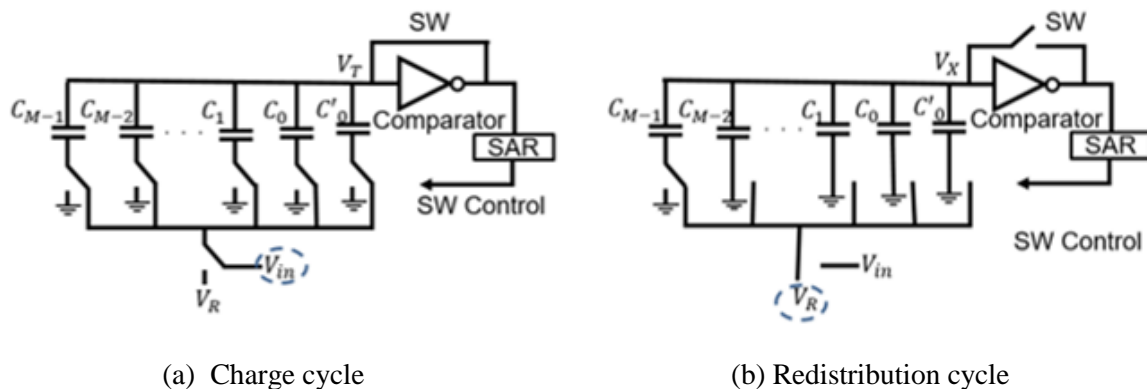
## Charge Distribution SAR ADC Architecture with Split Capacitor and its Testing

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This paper presents a charge distribution successive-approximation-register analog-to-digital converter (SAR ADC) architecture with a split capacitor connected in series. Fig.1 shows the charge distribution SAR ADC architecture; Fig. 1 (a) shows its charge cycle operation and Fig. 1 (b) explains its redistribution cycle one. At the beginning, in the charge cycle, the switch at the upper end of the comparator is turned on, and the lower end of each capacitor is connected to  $V_{in}$ . The upper end of the capacitor array at this time is  $V_T$ . Then in the redistribution cycle, the switch is turned off, only some of the capacitors are connected to  $V_R$  and the others are connected to GND. The upper end of the capacitor array at this time is  $V_X$ . Since the number of bits of the capacitor connected to  $V_R$  varies according to the analog input signal, the analog signal is converted into a digital signal of integer value.

However, with this method, capacitor array mismatches are caused in manufacturing process, so that the ADC linearity is limited. Here, as shown in Fig.2, dividing the binary weight into two parts and connecting with the split capacitor ( $C_s$ ) reduces the ratio of the capacitors in the circuit, making it easier to realize highly accurate circuits.

As a disadvantage of split capacitor usage, due to its parasitic capacitances, the overall ADC linearity degrades with specific digital codes. For this reason, if these codes are intensively examined in production test, high quality test can be done in a short time.<sup>[1]</sup>



[1] Yujie Zhao, Yuto Sasaki, Yuki Ozawa, Riho Aoki, Anna Kuwana and Haruo Kobayashi "ADC Histogram Test for Specific Codes", AMDE, Kiryu (Dec.2018)