Charge Distribution SAR ADC Architecture with Split Capacitor and its Testing

Riho Aoki, Anna Kuwana, Haruo Kobayashi (Gunma University) t15304001@gunma-u.ac.jp

1.Objective

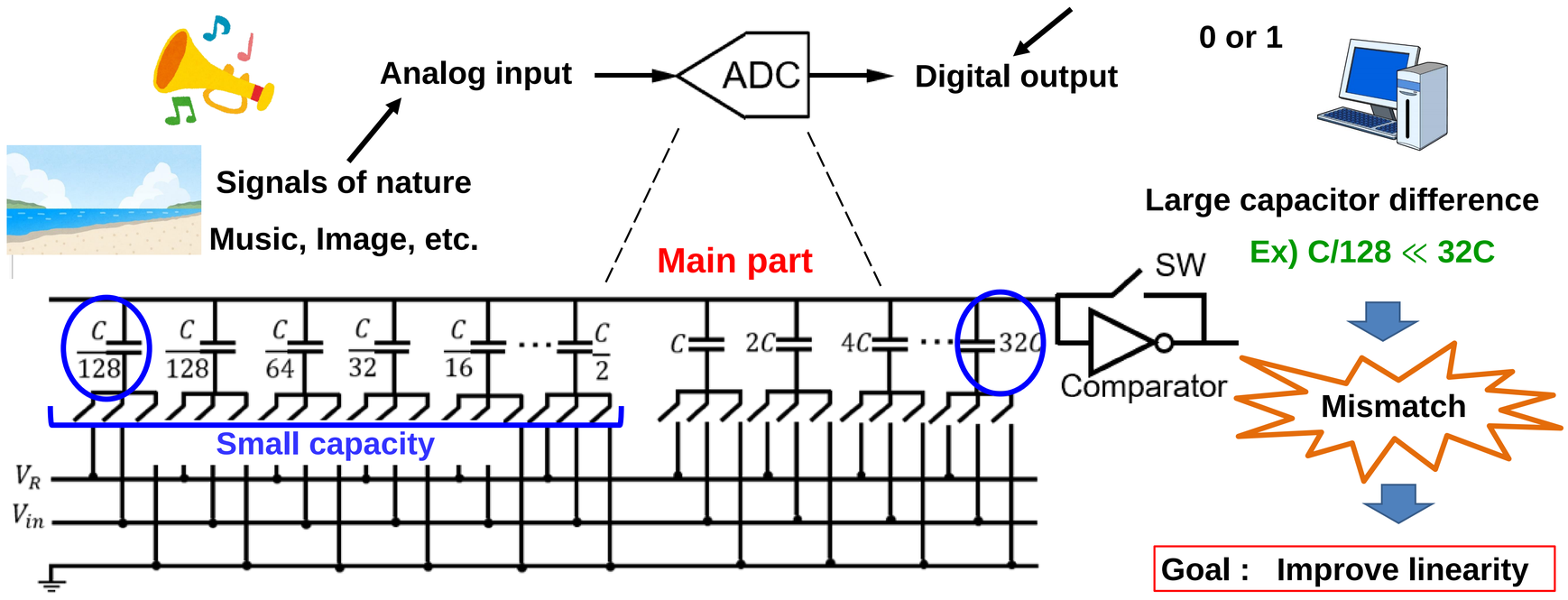
Development of high-Resolution,
high-Linearity
Charge Distribution SAR ADC

☹ Restriction of linearity
due to capacitor array mismatches

Approach

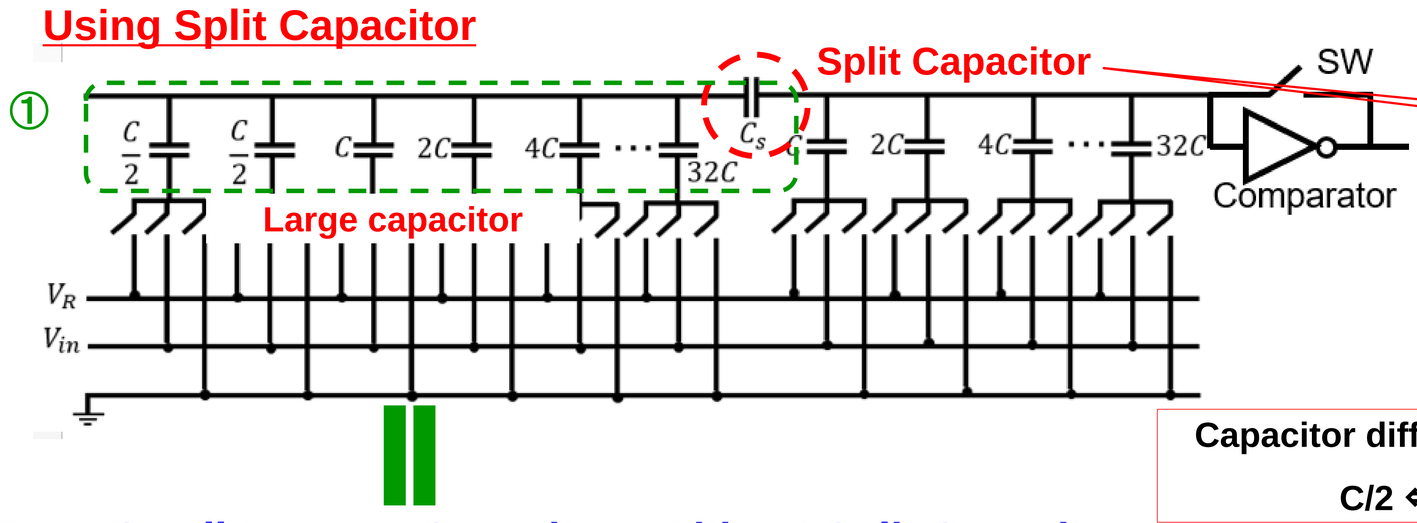
Improve linearity using Split Capacitor

2.Background

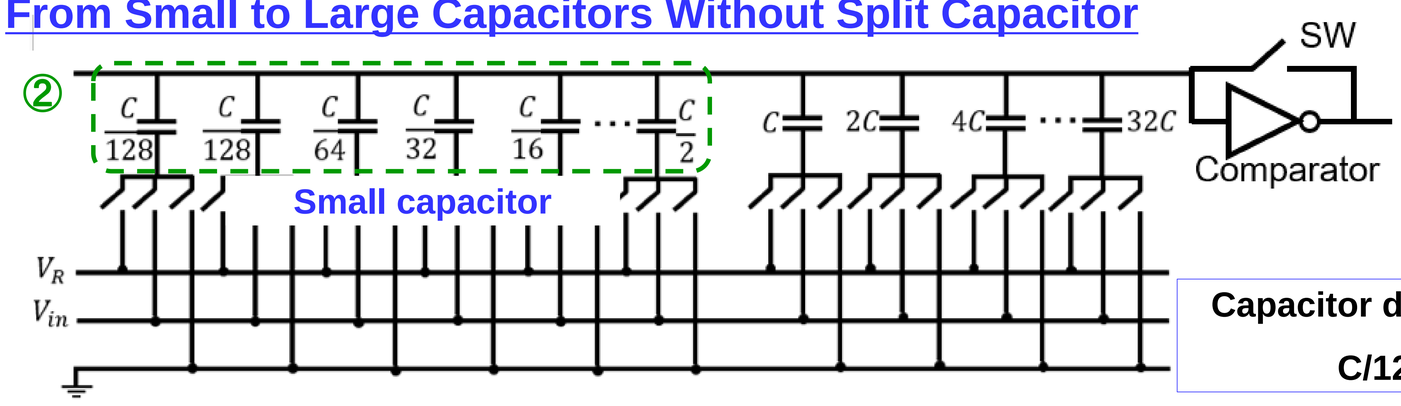


3.Proposed Circuit

Using Split Capacitor



From Small to Large Capacitors Without Split Capacitor



Capacitor difference : Small
C/2 ⇔ 32C

Capacitor difference : Large
C/128 ⇔ 32C

Connect Split Capacitor in series

Large capacitor =>
Equivalent small capacitor
Ex) 32C ⇒ C/2 4C ⇒ C/16

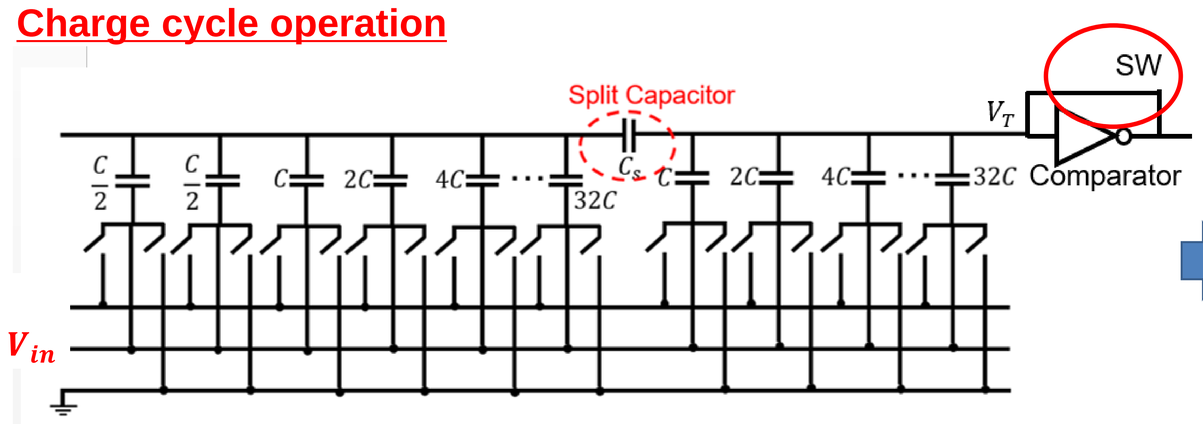
Capacitor difference → Small
Capacitor array mismatches → Small

Improve linearity

4. ADC Operation

Charge cycle operation

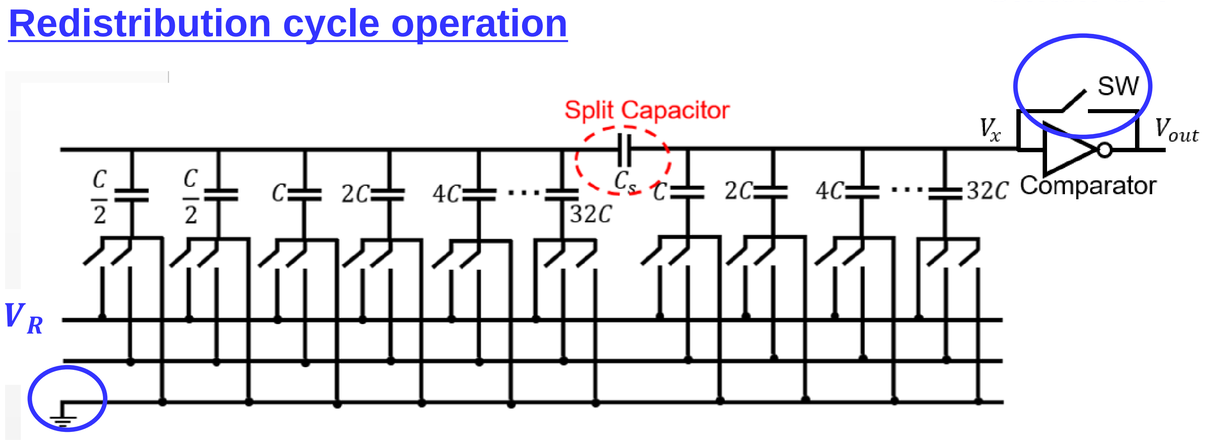
Switch ON



Connect all capacitors to V_{in} (analog input)

Redistribution cycle operation

Switch OFF



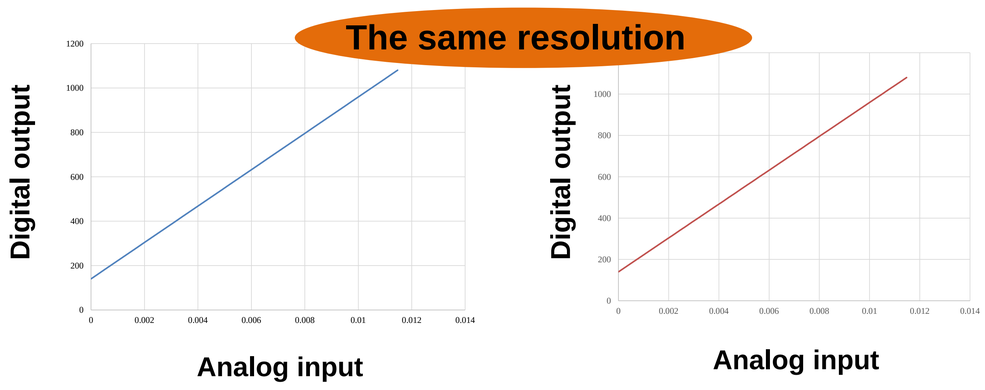
Connect some capacitors to V_R, and the rest to GND

5. Results

Capacitors connected to V_R ($V_T = V_X$)

Digital output

The same resolution



Without Split Capacitor
(Small capacitor)

With Split Capacitor
(Large capacitor)

<Split Capacitor Calculation>

① Equivalent capacitance

$$\frac{64CC_S}{64C + C_S}$$

=

② Equivalent capacitance

$$C$$

$$\therefore C_S = \frac{64C}{63} \cong 1.02C$$

Development of high-resolution without small capacitors

6.Conclusion

< Charge Distribution SAR ADC >

Conventional : Restriction of linearity
due to capacitor array mismatches

Proposed : Using Split Capacitor

- Capacitor array mismatches → Small
- Improve linearity

Reference

[1] Yujie Zhao, Yuto Sasaki, Yuki Ozawa, Riho Aoki, Anna Kuwana and Haruo Kobayashi "ADC Histogram Test for Specific Codes", AMDE, Kiryu (Dec.2018)