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Second-order DWA Algorithm and Circuit Design for Multi-bit ΔΣADC/DAC

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This paper describes a performance improvement technique of multi-bit ΔΣ ADCs/DACs, which are used for IoT applications such as sensor face interface. Their multi-bit configuration for low power causes overall DAC non-linearity due to characteristics mismatches among multiple unit cells [1] . We show here an algorithm as well as its circuit design to overcome this problem. Simulation results confirm the effectiveness of the proposed method.

Fig. 1 shows an equivalent block diagram of a ΔΣADC, where, When an internal DAC is multi-bit, then its nonlinearity is modelled by δ(t), which is not noise-shaped inside the modulator.

$$Y(z)=\frac{H(z)}{1+H(z)}[X(z)-\delta(z)]+\frac{1}{1+H(z)}E(z)$$

This paper proposes a second-order DWA (Data Weighted Averaging) or DEM (Dynamic Element Matching) algorithm to reduce the effects of mismatches among DAC unit elements with 2nd-order noise-shaping. It requires a two clock operation with switched capacitor circuit, which might make the circuit operation slow, but it is easy to implement. Our Matlab simulation confirmed its effectiveness.

Matlab simulations have been conducted with a 3-bit 2nd-order low pass ΔΣADC. We have compared 4 cases: (i) ideal DAC (without mismatches), (ii) with mismatches without DWA, (iii) mismatches with the 1st-order DWA, (iv) with mismatches with the proposed 2nd-order DWA.

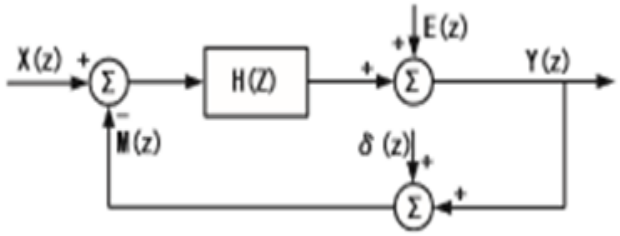

Fig.1: ΔΣAD modulator equivalent block diagram

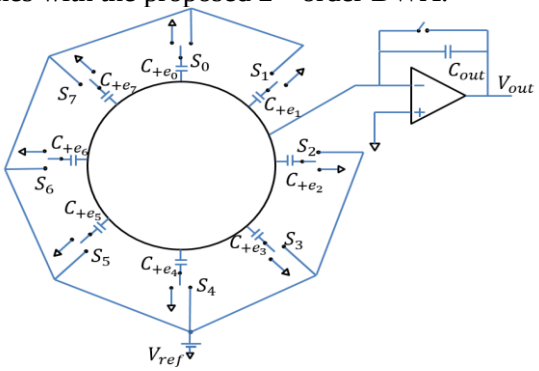

Fig 2: A multi-bit (9-level) DAC with the switched capacitor

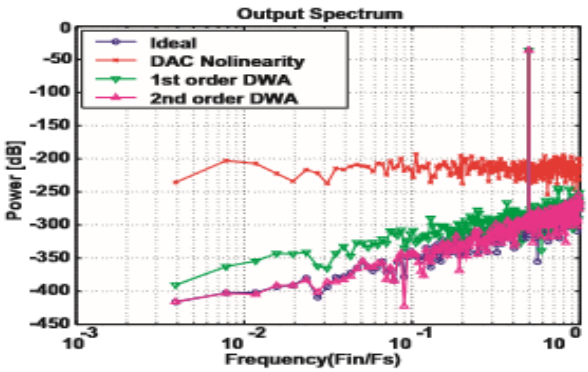

Fig.3 Simulated modulator output spectrum

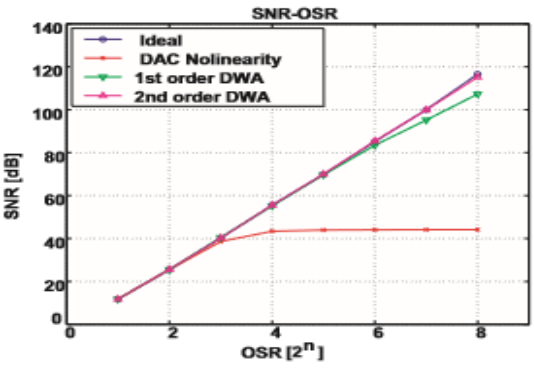

Fig.4 Modulator SNR obtained by MATLAB simulation

[1]R. Schreier, G.C Temes, Understanding Delta-Sigma DataConverters, Wiley-IEEE press (2009).