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5th International Symposium of Gunma University Medical Innovation and
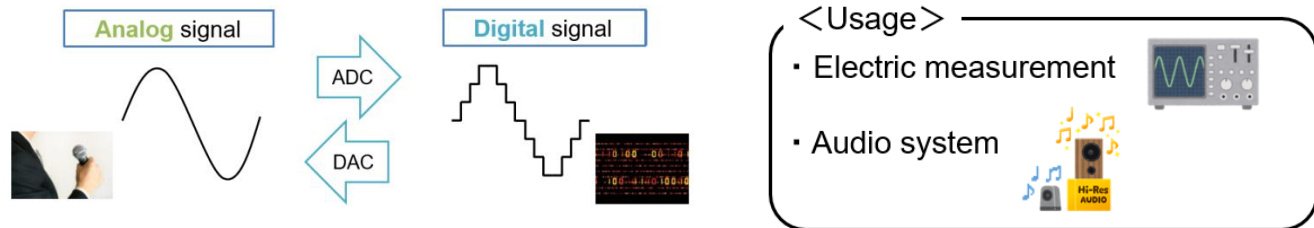9th International Conference on Advanced Micro-Device Engineering
(**GUMI&AMDE 2018**)

# Second-order DWA Algorithm and Circuit Design for Multi-bit ΔΣADC/DAC

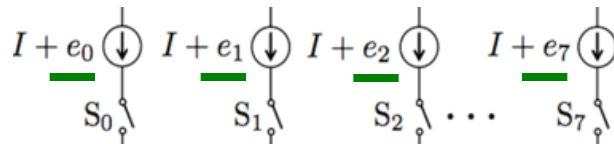**H. Hagiwara, Yuanyang Du, M. Murakami, H. San, A. Kuwana,  H. Kobayashi**

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Background：Digital-to-Analog Converter (DAC) for IoT applications

Problems：  Manufacturing variation among unit circuits in DAC

Linearity degradation

$e_0, e_1, .. e_7$: variations

Our approach:  Development of digital signal processing algorithm

Complicated yet smart, reliable, low-cost

$e_0, e_1, .. e_7$: variations are compensated.