P082

Second-order DWA Algorithm and Circuit Design for Multi-bit ΔΣADC/DAC

AMDE2018

6th December

Yuanyang Du , H. Hagiwara, M. Murakami, H. San, A. Kuwana, H. Kobayashi

Division of Electronics and Informatics, Gunma University (t171d602@gunma-u.ac.jp)

群馬大学 GUNMA UNIVERSITY

Kobayashi Laboratory

Research Objective & Background

Background

Background

ΔΣ ADCs/DACs for IoT applications

Sensor interface

Challenge

Multi-bit configuration
- Small hardware Good !
- Non-linearity Bad !

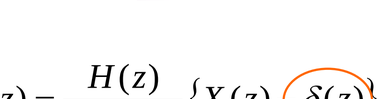
DWA algorithm
- Conventional:1st-order DWA
- Iur approach:2nd-order DWA

Objective

Problems

Manufacturing variation among unit circuits in DAC

Linearity degradation



e0, e1, .. e7: variations

Approach

Development of DSP algorithm
Complicated yet smart, reliable, low-cost

Variations are compensated.

What is DWA ?

DWA Techniques

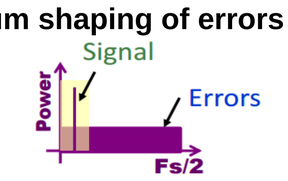
Error Correction:

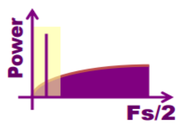
No measurement of errors

Redundancy usage

Time averaging of errors

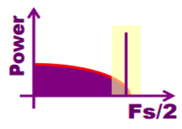
Spectrum shaping of errors





LP DWA

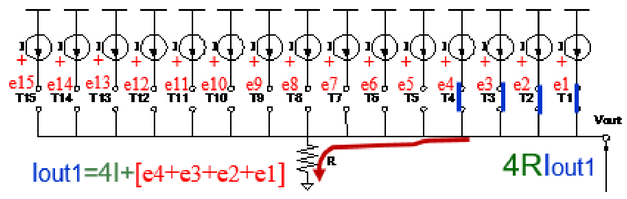
BP DWA

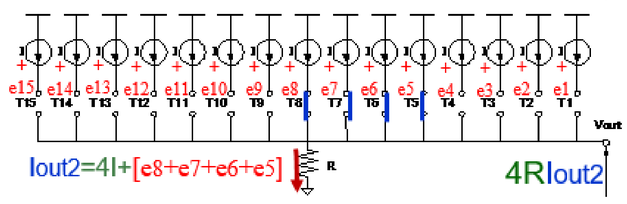


HP DWA

W/O DWA

Unit Cell Mismatches





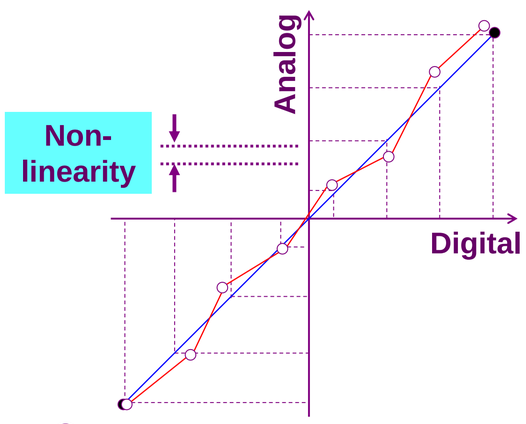
Spectrum shaping by cell selection order

DWA algorithm will solve this problem

DWA: Data Weighted Averaging

Multi-bit ΔΣADC/DAC

Multi-bit DAC Nonlinearity



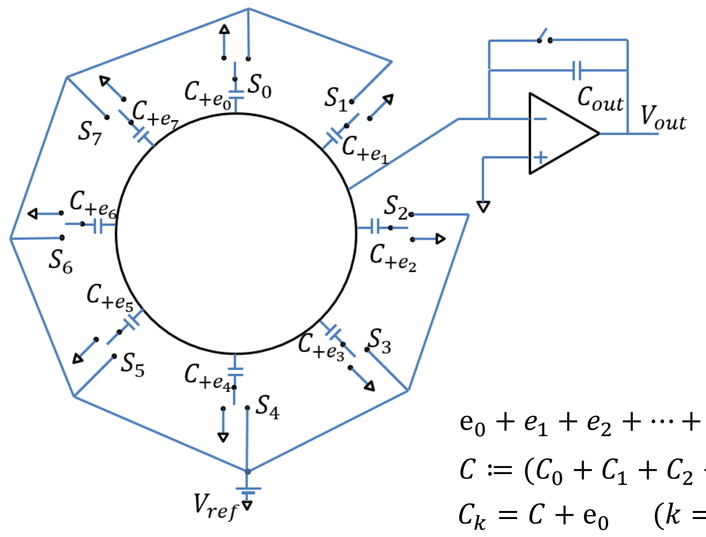
● :Single-bit Output
○ :Multi-bit Output

$$Y(z)=\frac{H(z)}{1+H(z)}\{X(z)-\delta(z)\}+\frac{1}{1+H(z)}E(z)$$

δ(z) is NOT noise-shaped

Multi-bit ΔΣADC/DAC

A multi-bit (9-level) DAC with switched capacitor



Digital input *m*
Without DWA algorithm

Output voltage

$$V_{out}=-m\frac{C}{C_{out}}V_{ref}+\delta$$

DAC nonlinearity

$$\delta=-\frac{e_0+e_1+e_2+\ldots+e_{m-1}}{C_{out}}V_{ref}$$

$$e_0+e_1+e_2+\cdots+e_7=0$$

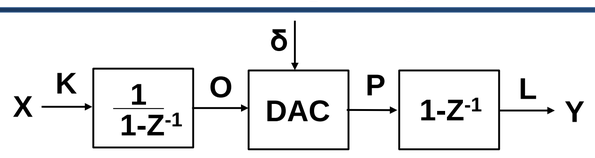
$$C:=(C_0+C_1+C_2+\cdots+C_7)/8$$

$$C_k=C+e_0 \quad (k=0,1,2\cdots,7)$$

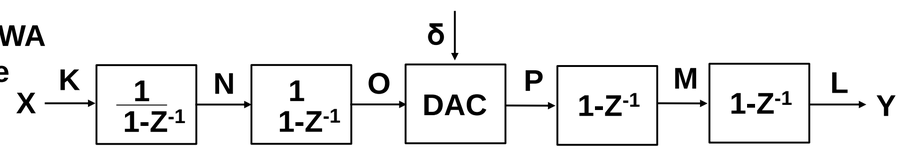
Proposed 2nd-order DWA Algorithm

2nd-order Noise-Shaping of DAC Nonlinearity

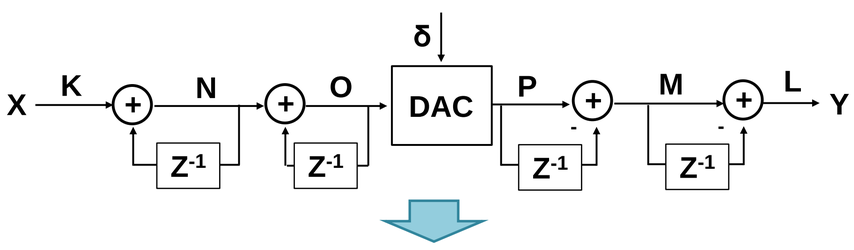
(a) 1st-order DWA architecture



(b) 2nd-order DWA architecture

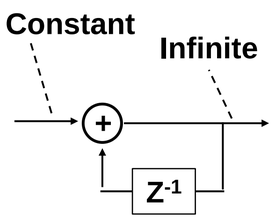


(c) Equivalent block diagram



$$Y(z)=X(z)+(1-z^{-1})^2\delta(z)$$

Problem



Does not work !

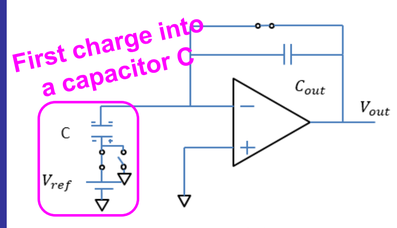
Operation of Proposed Algorithm

Time ↓

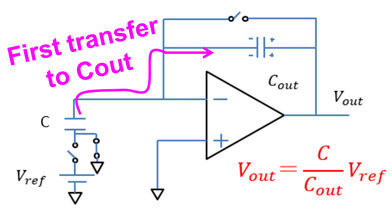
Input	C0	C1	C2	C3	C4	C5	C6	C7
3	+	+	+					
4			-	+	+	+	+	+
2			++					
5	+		-	+	+	+	+	+
6		++	++	+	+			
1	+		-	-	-	+	+	+
2		-	+	+	+			
3		++	+					
3		-	-	+	+	+	+	+

Circuit Realization

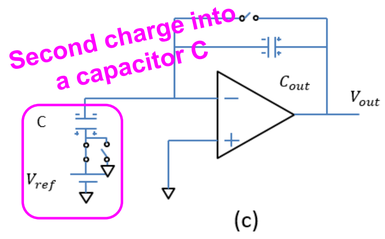
Twice unit cell output is realized with 2 clock operation.



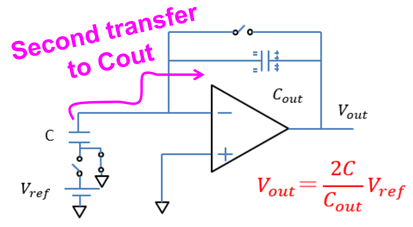
(a)



(b)

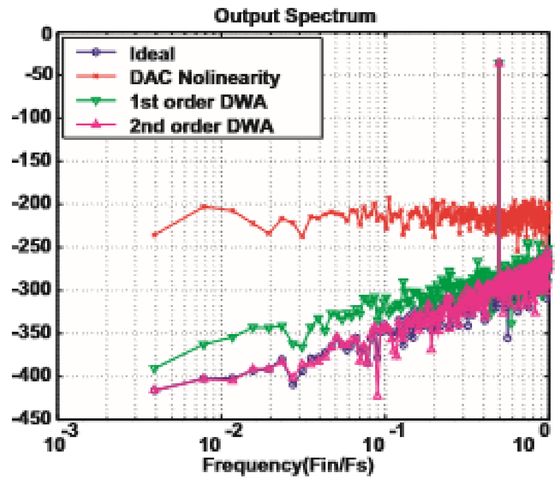


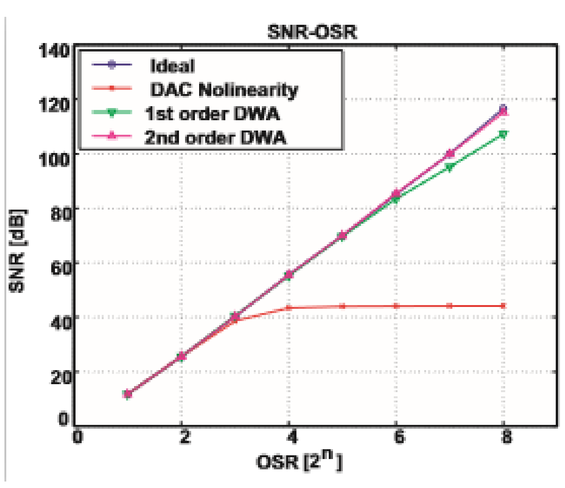
(c)



(d)

Simulation Result





- 2nd-order DWA is more effective
- But its circuit/operation become complicated

Summary

- A 2nd-order DWA algorithm is proposed
- Reduce mismatches with 2nd-order noise-shaping
- Requires a two clock operation with switched capacitor circuit
- Make the circuit operation slow, but easy to implement