AMDE

Algorithm for Improving SNDR in ΔΣ DAC

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This paper presents linearity improvement algorithms for multi-bit ΔΣ digital-to-analog converters (DACs), utilizing digital techniques. The ΔΣ DACs are used for communication systems, electronic measurement, automatic test equipment as well as audio systems, for their easy implementation of high resolution [1]. However, their multi-bit configuration causes overall DAC non-linearity due to characteristics mismatches among multiple unit cells, even though they can be implemented with small hardware and power.

Therefore, we have investigated Data-Weighted Averaging (DWA) algorithms [2-5] which improve their DAC linearity. We have simulated a ternary (three values: -1, 0, +1 for unit cell) DAC [5] as well as a binary (two values: 0, +1) DAC. Then we have found from that for the low-pass (LP) signal band, DWA (type I) is effective in case of both ternary and binary DACs; for high-pass (HP), band-pass (BP) signal bands, DWA (type I) is effective in the case of the ternary, whereas DWA (type II) is effective in the case of the binary.

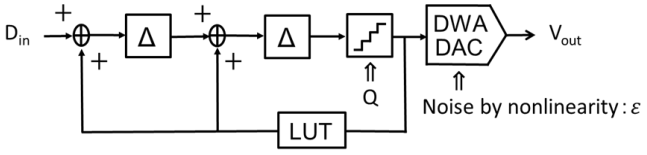
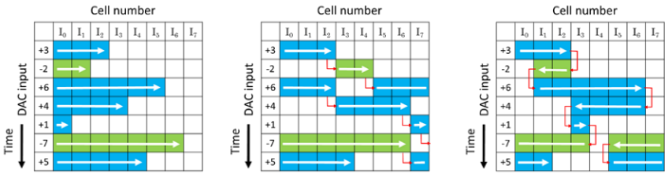


Fig.1. 2nd-order HP or BPΔΣ DAC configuration.



(a) multi-bit DAC (b) DWA type I (c) DWA type II
Fig. 2. Multi-bit DAC unit cell selection methods.

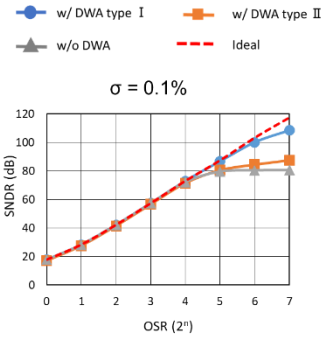
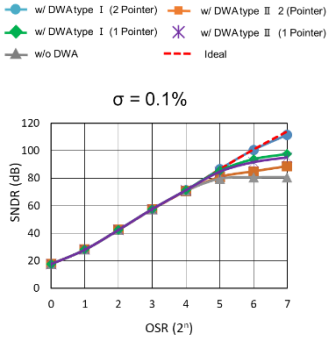


Fig.3. SNDR vs. OSR of HP ΔΣ DAC



.Fig.4. SNDR vs. OSR of BP ΔΣ DAC.

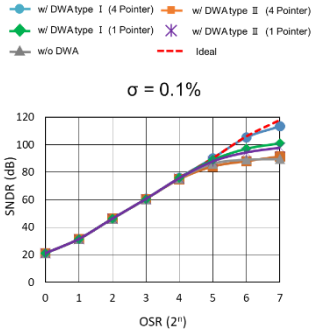


Fig.5. SNDR vs. OSR of BP ΔΣ DAC.

Table.1. Binary, Ternary DWA Overview

Signal Band	Value	Number (N) of Signal Bands	DWA type
LP	Binary	1	I
	Ternary	1	I
HP	Binary	1	II
	Ternary	1	I
BP	Binary	2	II
	Binary	4	II
	Ternary	2	I
	Ternary	4	I

Reference:

[1] R. Schreier, G.C Temes, Understanding Delta-Sigma Data Converters, Wiley-IEEE press (2009).
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[3] M. Murakami, H. Kobayashi, et. al., "I-Q Signal Generation Techniques for Communication IC Testing and ATE Systems", IEEE International Test Conference (Nov. 2016).
[4] A. Motozawa, H. Hagiwara, Y. Yamada, H. Kobayashi, et. al., "Multi-BP ΔΣ Modulation Techniques and Their Applications", IEICE Tran, vol. J90-C, no.2, pp.143-158 (Feb. 2007).
[5] I. Jang, et. al., "A 4.2mW 10MHz BW 74.4dB SNDR Fourth-order CT DSM with Second-order Digital Noise Coupling Utilizing an 8b SAR ADC", VLSI Circuits Symp (June 2017).