P081

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SNDR Improvement Algorithms in Binary and Ternary ΔΣDAC

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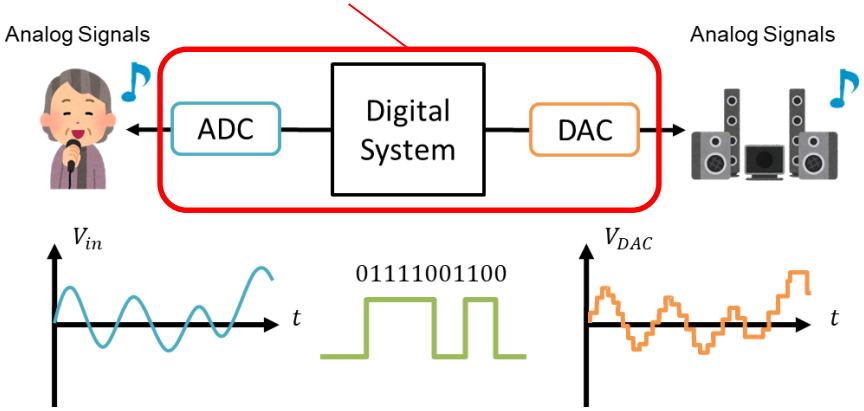
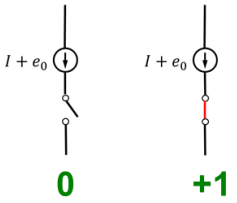
Demand for better digital-to-analog converter (DAC)



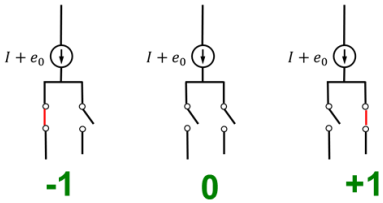
Binary



Binary unit cell ➡ 1-bit

Conventional

Ternary

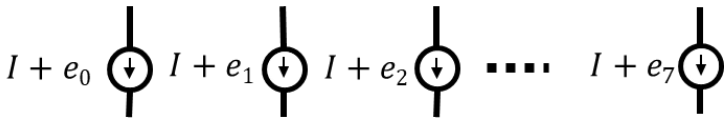


Ternary unit cell ➡ 1.5-bit

High resolution

Problem

Manufacturing variations
among DAC circuit elements



Purpose of this work

DSP algorithms
to suppress the variation effects
for binary and ternary DACs