1. Objective

Demand for better digital-to-analog converter (DAC)

**Problem**

Manufacturing variations among DAC circuit elements

**Purpose of this work**

DSP algorithms to suppress the variation effects for binary and ternary DACs

2. Background

**δΣ Digital to Analog Converter (Low Pass)**

![δΣ Digital to Analog Converter Diagram]

**Purpose**

- Measurement & audio applications
- Mostly digital circuit
- High-resolution, high-linearity
- DC signal, low frequency signal generation
- Purpose:
  - Improve linearity (High resolution)

3. Introduction to Ternary

**8 current sources**

- Binary unit cell: 1-bit
- Ternary unit cell: 1.5-bit

**Forces**

- Binary ⇒ ± and 0 value
- Ternary ⇒ ±, - and 0 value

**Reasons for Ternary Usage**

- Higher resolution for given current sources
- Smaller number of current sources for given resolution

4. DWA* Algorithm (* Data-Weighted Averaging)

**Conventional**

- Cell number

  - Unit cell mismatch ⇒ Accumulation

**DWA type I**

- Cell number

  - Push unit cell mismatch ⇒ Averaging

**DWA type II** (Back and forth)

- Cell number

**SNDR Improvement Algorithms**

- **LP**
  - Binary 1
  - Ternary 1

- **HP**
  - Binary 1
  - Ternary 1

- **BP**
  - Binary 2
  - Ternary 2

- **Ternary 4**

**New Findings**

It is high linearity when DWA type I is used.

5. Binary, Ternary DWA Overview

**Segmented DAC with ternary unit cells**

- High-pass (HP) δΣ DAC (N=1)
- Band-pass (BP) δΣ DAC (N=2)
- Band-pass (BP) δΣ DAC (N=4)

6. Pointer

**1 Pointer**

- High-pass (HP) δΣ DAC

**2 Pointers**

- Band-pass (BP) δΣ DAC (N=2)

**4 Pointers**

- Band-pass (BP) δΣ DAC (N=4)

7. Conclusion

**< δΣ DA modulator >**

In case HP, BP δΣ DACs with ternary unit cells, DWA type I with pointers alternately used is effective.

**Reference**