SNDR Improvement Algorithms in Binary and Ternary ΔΣDAC

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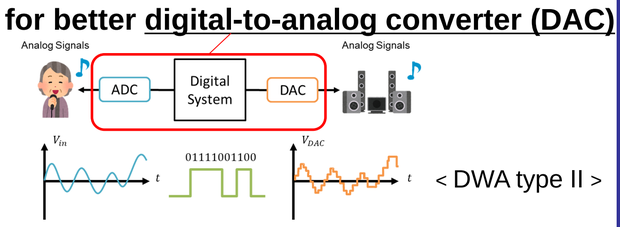
1.Objective

Demand for better digital-to-analog converter (DAC)



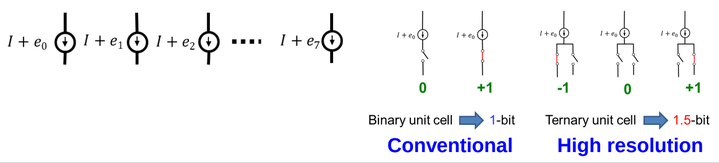
< DWA type II >

Problem

Manufacturing variations among DAC circuit elements

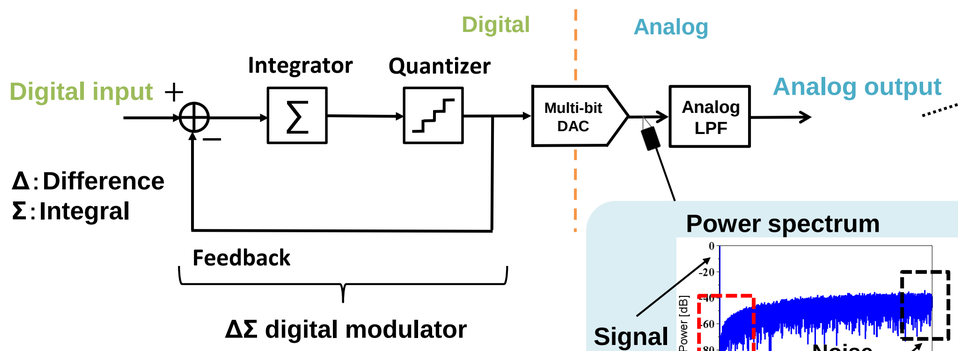
Purpose of this work

DSP algorithms to suppress the variation effects for binary and ternary DACs



2.Background

ΔΣ Digital to Analog Converter (Low Pass)



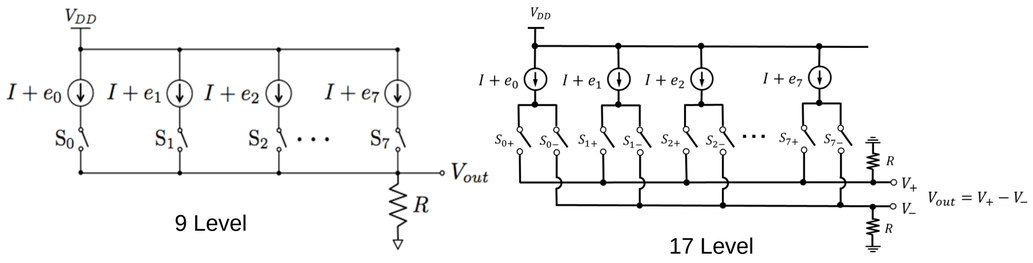
< Using >

Measurement & audio applications

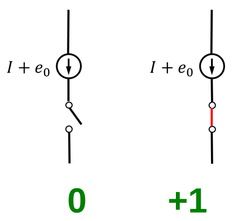
- **ΔΣ Digital-to-Analog Converter (ΔΣDAC) →Required**
  - Mostly digital circuit
  - High-resolution ,High-linearity
  - DC signal , low frequency signal generation
- **Purpose**
  - Improve linearity (High resolution)

3. Introduction to Ternary

8 current sources

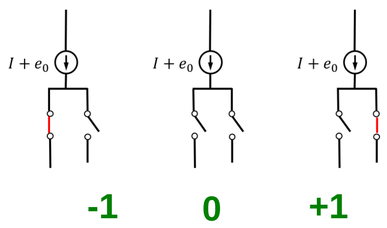


Binary



Binary unit cell ⇒ 1-bit

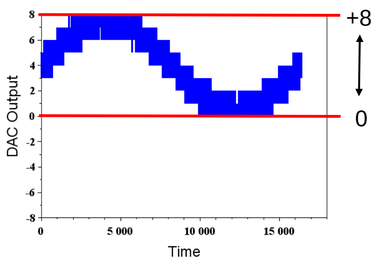
Ternary



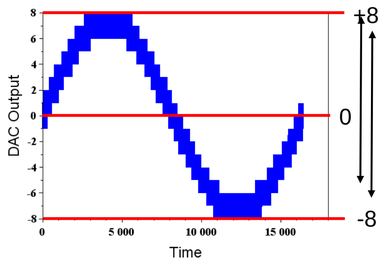
Ternary unit cell ⇒ 1.5-bit

Forces

Binary ⇒ + and 0 value



Ternary ⇒ +, - and 0 value

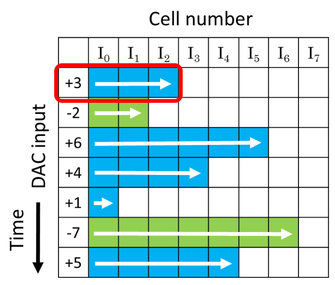


Reasons for Ternary Usage

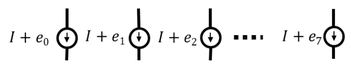
Higher resolution for given current sources
Smaller number of current sources for given resolution

4. DWA*Algorithm (* Data-Weighted Averaging)

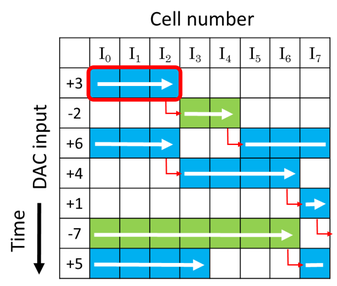
Conventional



Unit cell mismatch
⇒ Accumulation
e_i

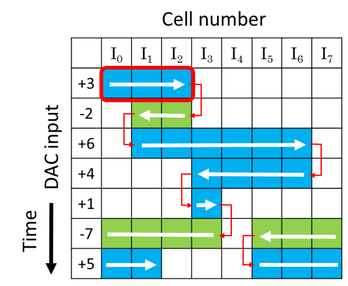


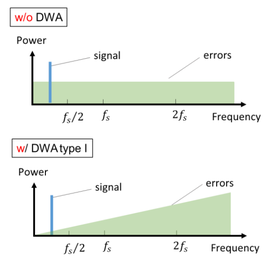
DWA type I

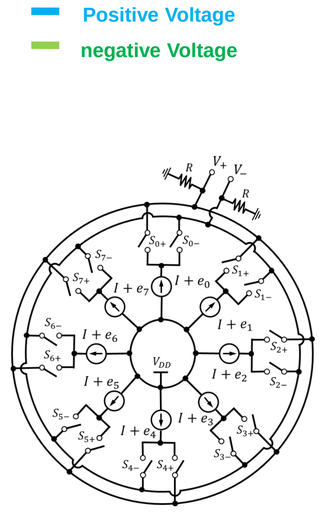


Distribute unit cell mismatch
⇒ Averaging
Improve linearity

DWA type II (Back and forth)





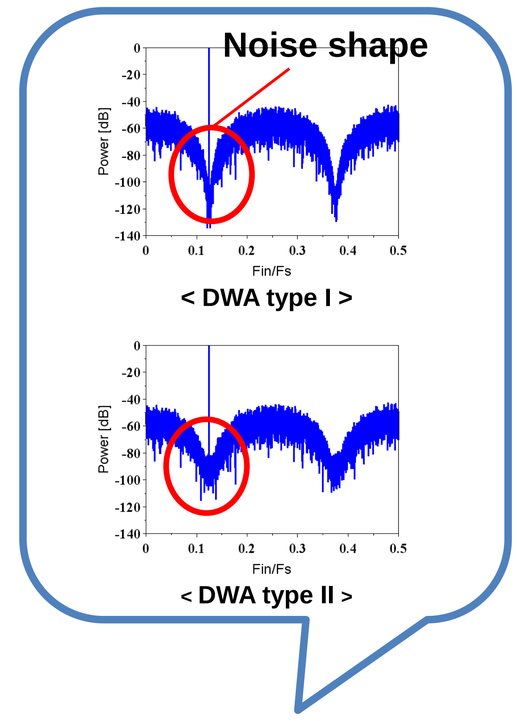


5. Binary, Ternary DWA Overview

Signal Band	Value	Number (N) of Signal Bands	DWA type
LP	Binary	1	I
	Ternary	1	I
HP	Binary	1	II
	Ternary	1	I
BP	Binary	2	II
	Binary	4	II
	Ternary	2	I
	Ternary	4	I

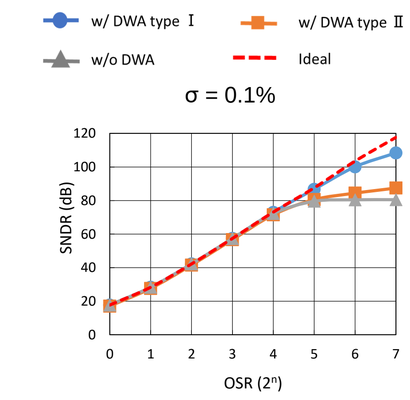
New Findings

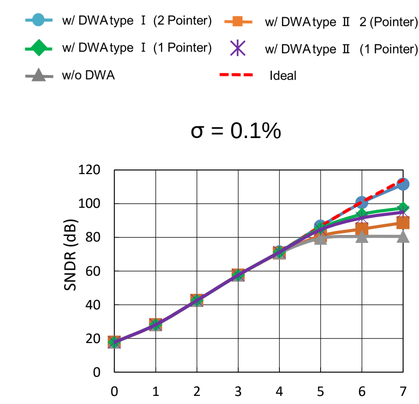
It is high linearity when DWA type I is used.

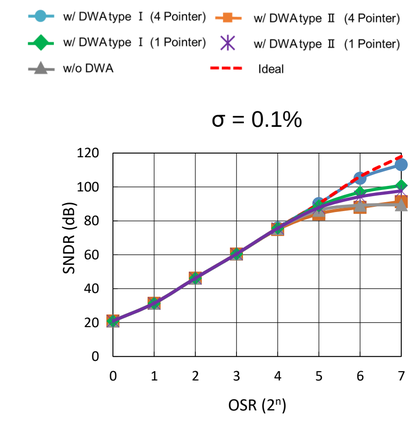


Segmented DAC with ternary unit cells

- High-pass (HP) ΔΣ DAC (N=1)
- Band-pass (BP) ΔΣ DAC (N=2)
- Band-pass (BP) ΔΣ DAC (N=4)

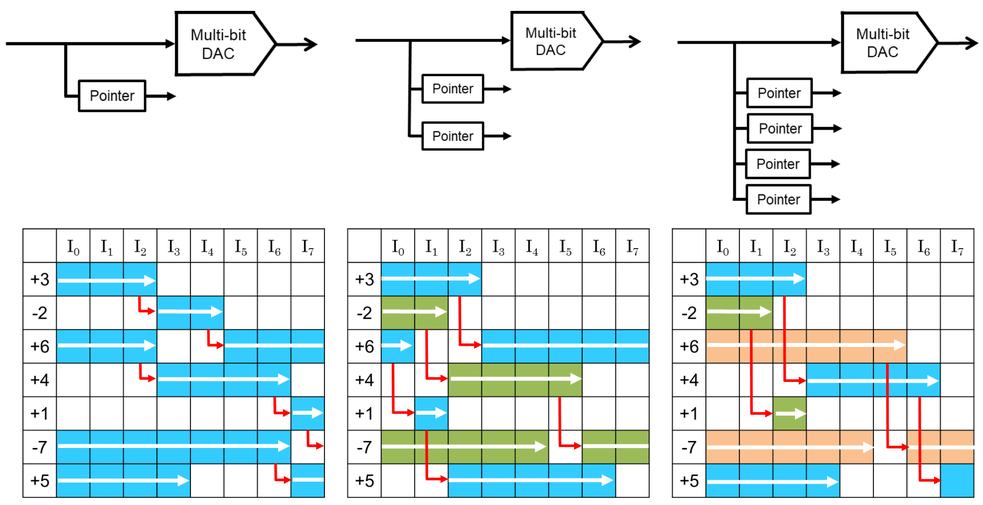






6.Pointer

1 Pointer **2 Pointers** **4 Pointers**



7.Conclusion

＜ ΔΣ DA modulator ＞

In case HP, BP ΔΣ DACs with ternary unit cells, DWA type I with pointers alternately used is effective.

Reference

[1] R. Schreier, G.C Temes, Understanding Delta-Sigma Data Converters, Wiley-IEEE press (2009).[2] Y. Geerts, M. Steyaert, W. Sansen, Design of Multi-Bit Delta-Sigma A/D Converters, Kulwer Academic Publisher (2002).

[3] M. Murakami, H. Kobayashi, et. al., "I-Q Signal Generation Techniques for Communication IC Testing and ATE Systems", IEEE International Test Conference (Nov. 2016).

[4] A. Motozawa, H. Hagiwara, Y. Yamada, H. Kobayashi, et. al., "Multi-BP ΔΣ Modulation Techniques and Their Applications", IEICE Tran, vol. J90-C, no.2, pp.143-158 (Feb. 2007). [5] I. Jang, et. al., "A 4.2mW 10MHz BW 74.4dB SNDR Fourth-order CT DSM with Second-order Digital Noise Coupling Utilizing an 8b SAR ADC", VLSI Circuits Symp (June 2017).