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Integration-type Time-to-Digital Converter Using Vernier Oscillators

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This paper proposes an integration-type time-to-digital converter (TDC) architectture using two oscillators with different frequencies f_1, f_2 (Figs.1, 2). This TDC architecture is inspired by the integration-type ADC, and hence we call it an integration-type TDC. It consists of two trigger circuits, a sampling flip-flop, a binary counter and additional small logic circuit. The time measurement resolution is given as $1/f_1 - 1/f_2$, and this method may be also called a Vernier oscillator TDC from the resemblance of a Vernier micrometer principle. Notice that the frequency is a stable signal, and hence accurate time resolution of $1/f_1 - 1/f_2$ as well as good overall TDC linearity be obtained without calibration.

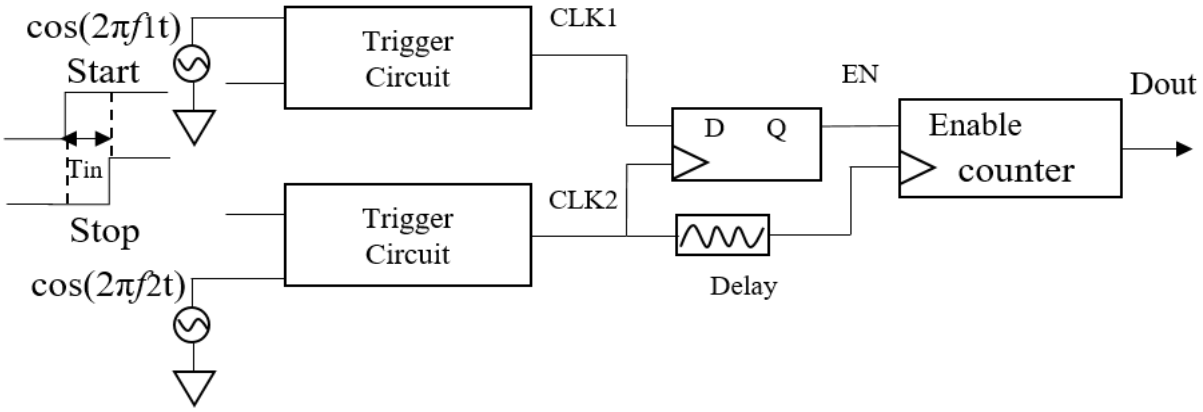

Fig. 1. Proposed integration-type TDC with Vernier oscillators.

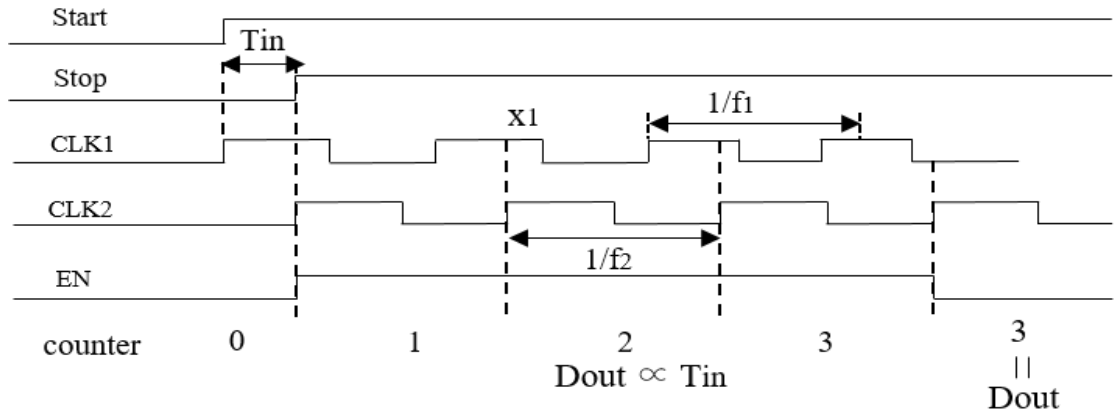

Fig. 2. Timing chart in Fig. 1.

[1]Renato Turchetta, Analog Electronics for Radiation Detection,Science and Technology Facilities Council,United Kingdom (2016)
[2] K. Machida, Y. Ozawa, Y. Abe, H. Kobayashi, "Time-to-Digital Converter Architectures Using Two Oscillators With Different Frequencies", 27th IEEE Asian Test Symposium, Hefei, Anhui, China (Oct. 2018)
[3] Y. Sasaki, H. Kobayashi, "Integral-type Time-to-Digital Converter", IEEE 14th International Conference on Solid-State and Integrated Circuit Technology, Qingdao, China (Nov. 2018)