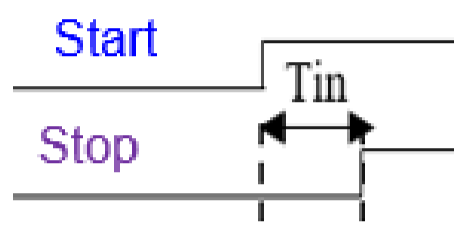




1. Research Objective

Research for time-to-digital converter architectures with Vernier oscillators

- Time Measurement between Start and Stop rising edges digital output D_{out}

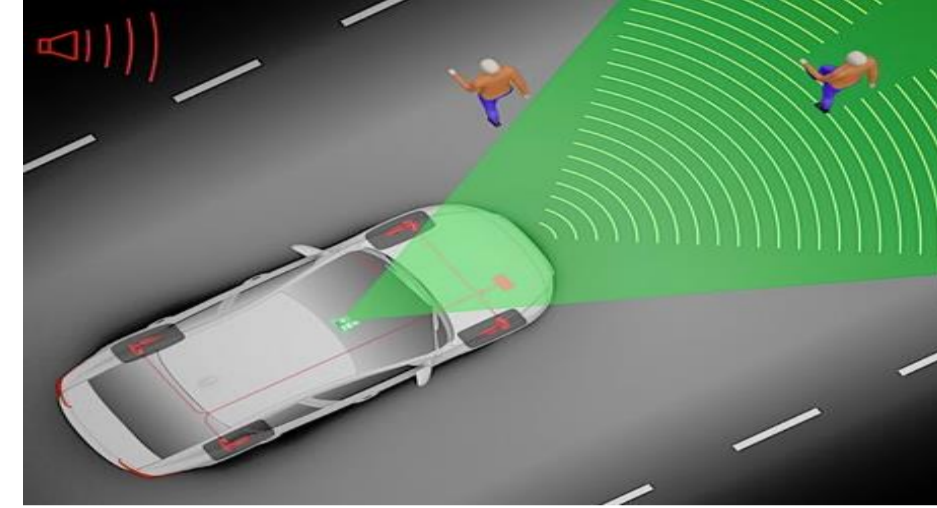


- Inspired by integration-type ADC
- Two oscillators with different frequencies
Fine time resolution $T_1 - T_2$
 $T_1 = 1/f_1, T_2 = 1/f_2$
- Simple circuit
- Good linearity without calibration

2. TDC & Vernier Application Examples



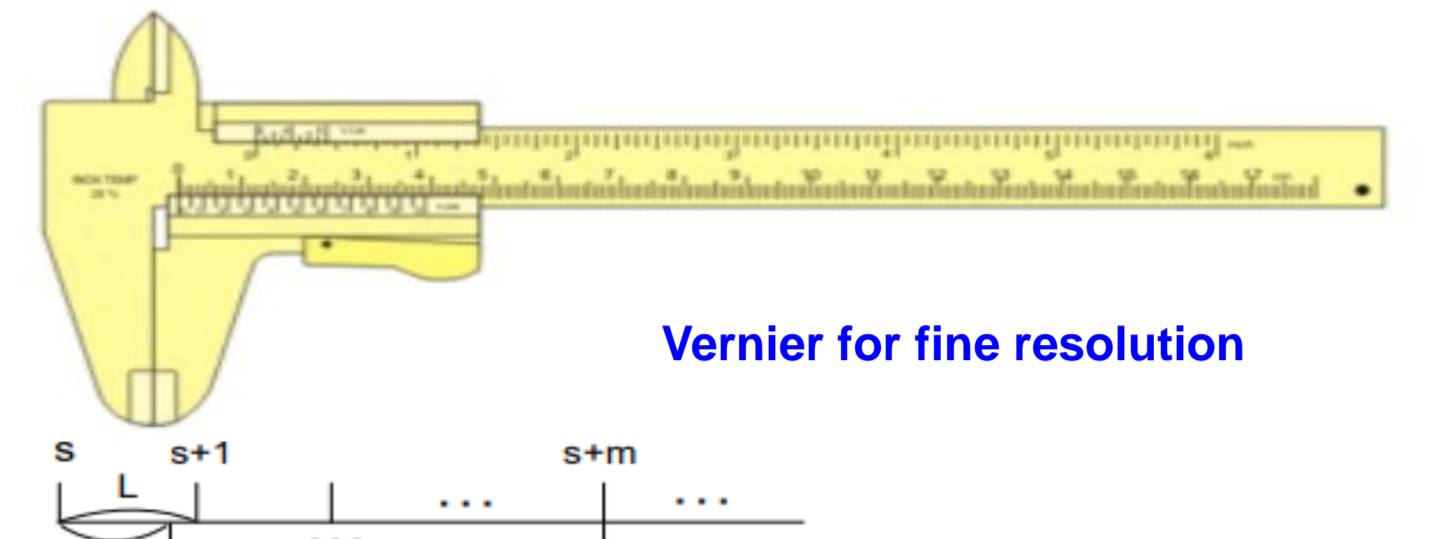
Radar distance measurement



Vehicle distance measurement



Tram arrival time



Vernier for fine resolution

Taking the scale of the minor scale

$$L' = \frac{n-1}{n}L \quad \dots(1)$$

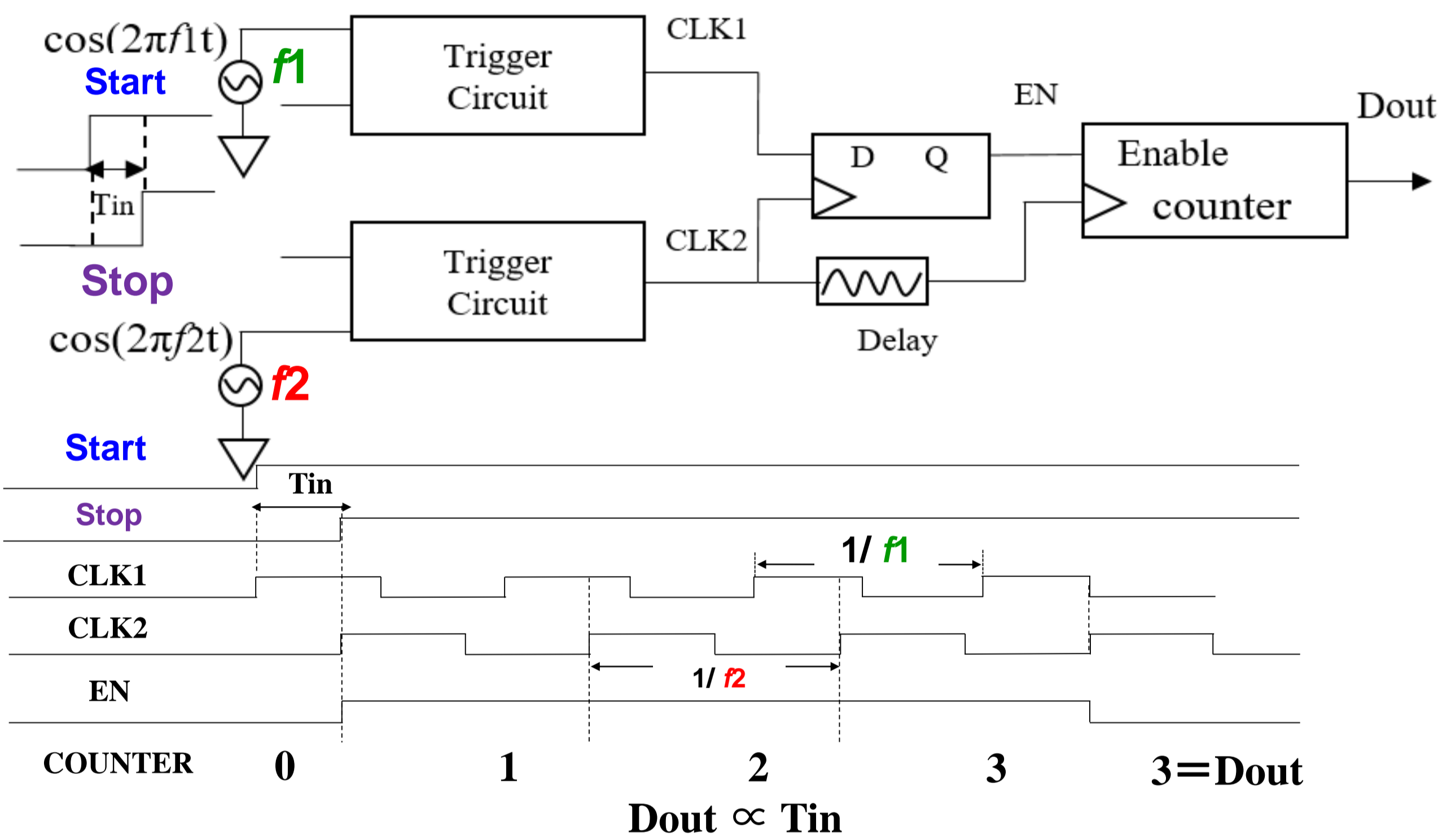
As shown in the figure

$$((s+m) - s)L = x + mL' \quad \dots(2)$$

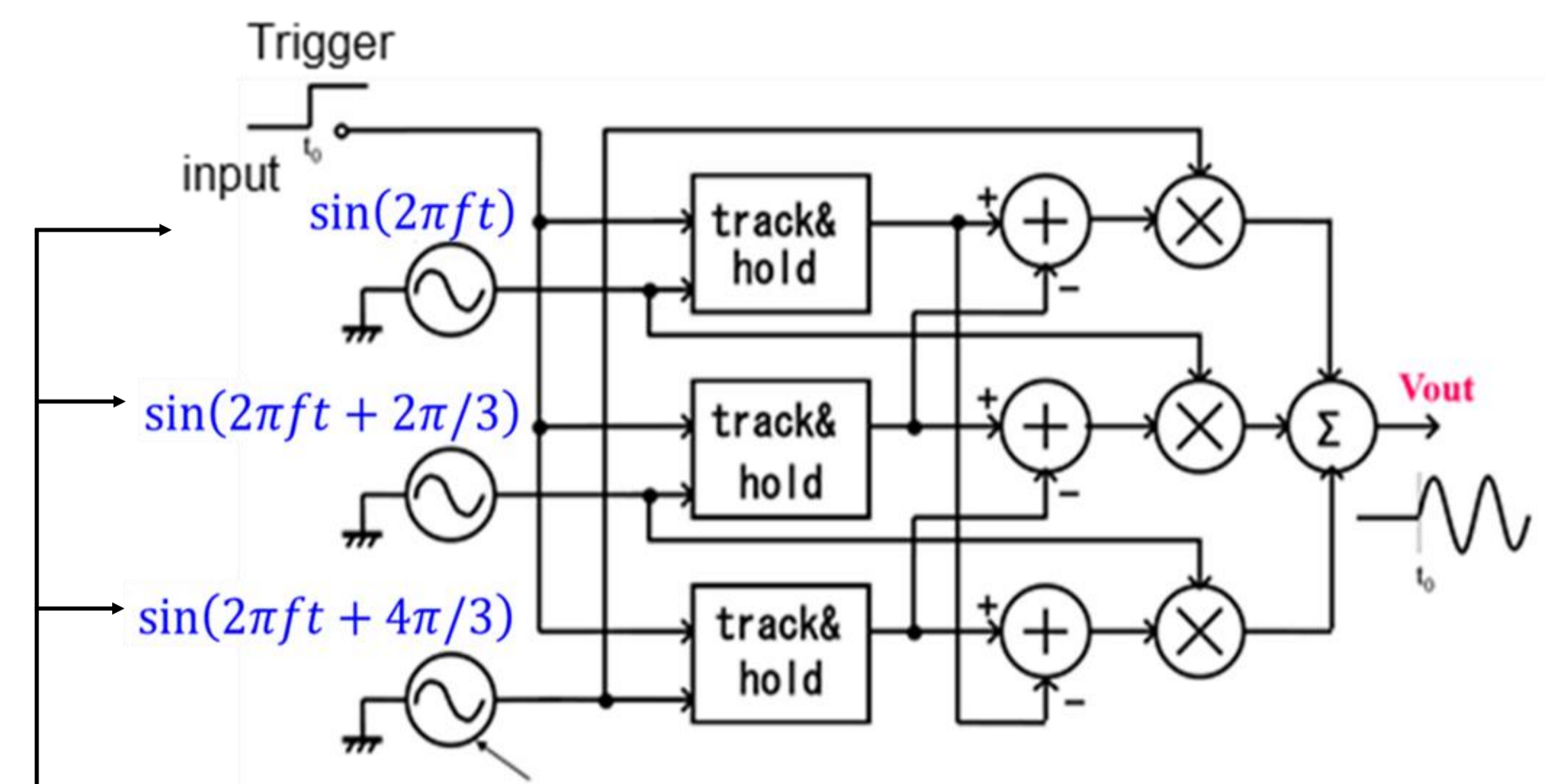
$$mL = x + m \frac{n-1}{n}L$$

$$x = \frac{L}{n}m \quad \dots(3)$$

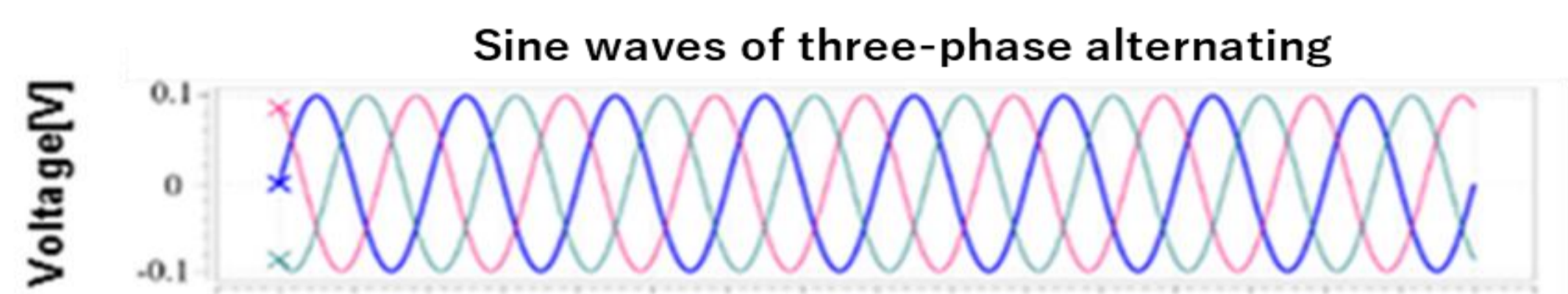
3. Proposed Circuit



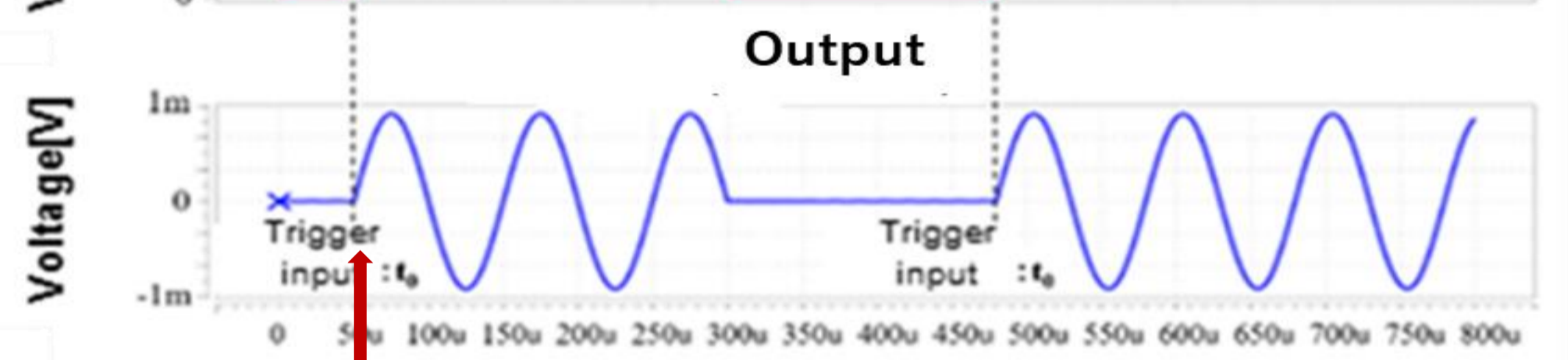
4. Trigger Circuit & Simulation Results



Enter three sine waves

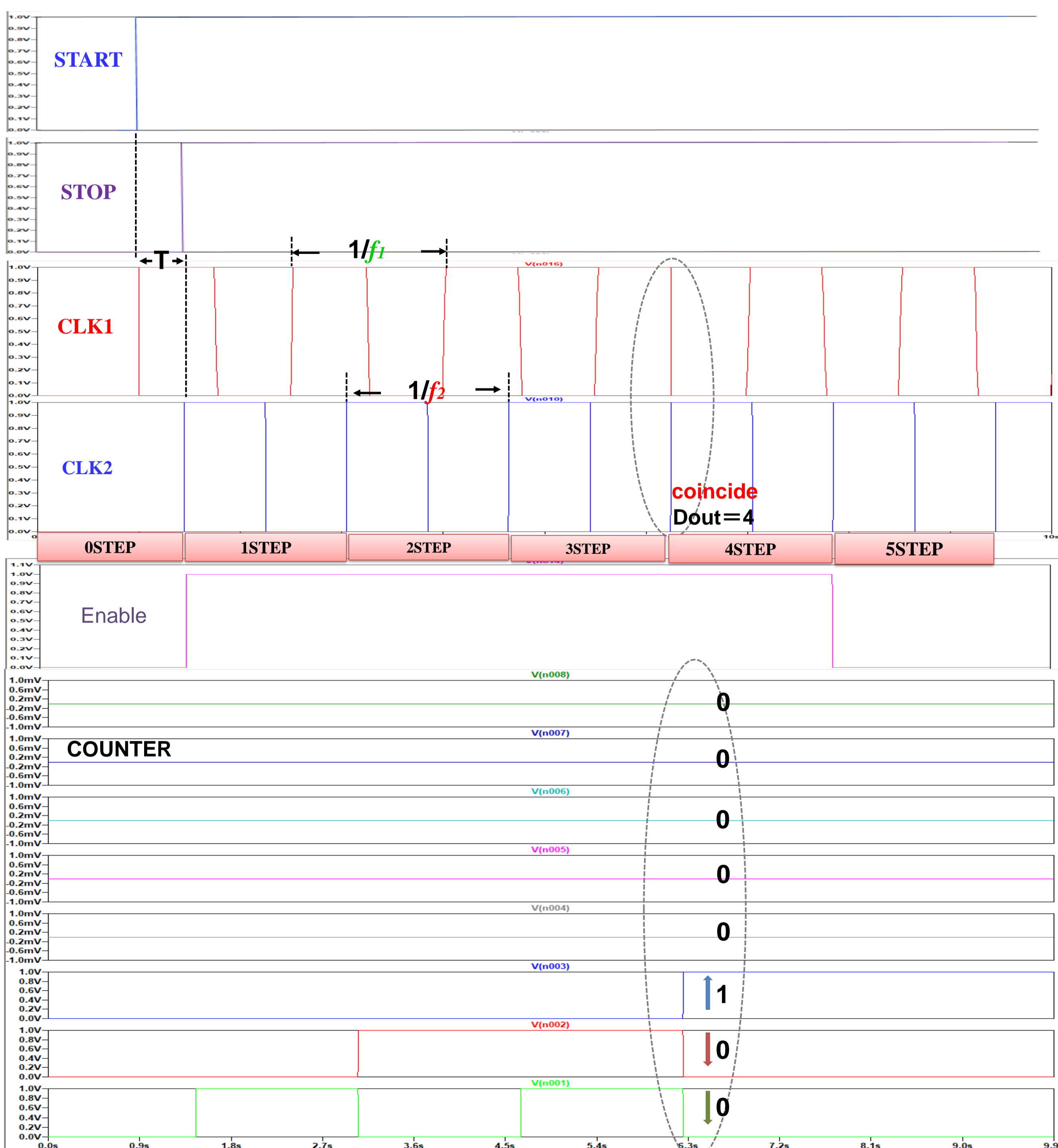


Sine waves of three-phase alternating



Output starts to oscillate at the rising time edge of trigger input

5. Simulation Results



Counter output results is 00000100
Binary number \rightarrow Octal number
00000100=4

$$D_{out} \times |1/f_1 - 1/f_2| = T$$

Period difference = $0.1 \text{ ps} \times 4 = 0.4 \text{ ps}$



6. Conclusion

- New time-to-digital converter architecture
- Accurate fine time resolution of $1/f_1 - 1/f_2$
- Good overall linearity without calibration
- Long measurement time
- Operation is confirmed with simulation



谢谢

ありがとうございます。

Thank you