AMDE

Experimental Verification of Improved Nagata Current Mirrors

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This paper describes silicon verification of our improved peaking current mirror, originally invented by Nagata Minoru in 1966. Our improved MOS current mirror circuits are insensitive to wide range of power supply voltage variation and they are realized by addition of multiple current peaks. We show their chip design/measurement results, and their performance evaluation. The proposed circuits are simple (such as, no need for startup circuit), small yet well-insensitive to power supply voltage variations, and they can be widely used in analog ICs.

We proposed an improved Nagata current mirror in which provides constant current over much wider range of the power supply voltage fluctuation than the original Nagata current mirror, using multiple current mirror circuits with different current peaks in Figs.1, 2.

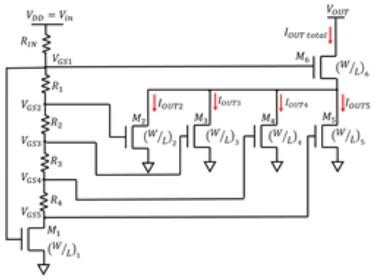

Fig. 1. Proposed MOS reference current source.

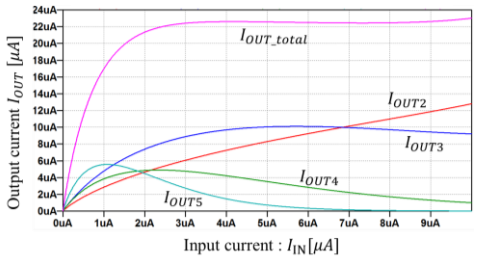

Fig. 2. SPICE simulation results

We have designed the circuits in Fig. 1 and fabricated them through TSMC 0.35µm CMOS process (Fig. 3). One chip has 4 sets (A, B, C, D sides) of the designed circuits (T1, .., T5). Each set is rotated by 90 degrees with respect to the side (Fig. 4). We have evaluated 5 chips (#1, …, #5), and measured 20 samples (4 (A, B, C, D) x 5 (#1, .., #5)) for each circuit (T1, …, T5).

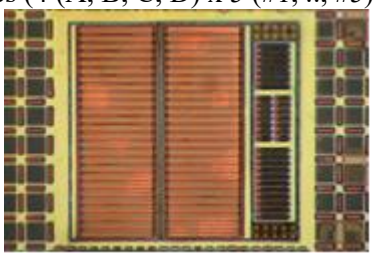

Fig. 3. Chip photo of our proposed circuit.

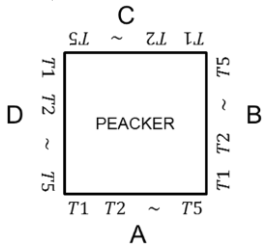

Fig.4. Arrangement of prototype chip

We measured the total output current (Iout) in Fig. 1, for the input voltage (Vin) from 0 to 5.0V by varying the output voltage (Vout) from 1V to 3V, and obtained the results as expected.

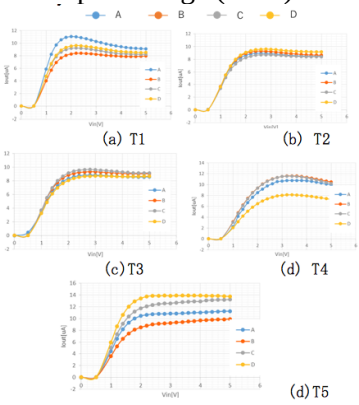

Fig. 5. Output current measurement results of circuit type (T1~T5) on (A~D) sides of chip #1

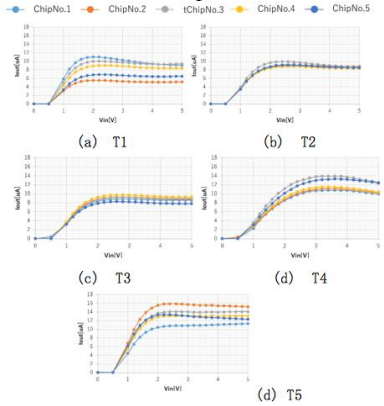

Fig. 6. Output current measurement results on side A across chips (#1~#5)

[1] M. Hirano, N. Tsukiji, H. Kobayashi, "Simple Reference Current Source Insensitive to Power Supply Voltage Variation - Improved Minoru Nagata Current Source", IEEE 13th International Conference on Solid-State and Integrated Circuit Technology, Hangzhou, China (Oct. 2016).