AMDE

ADC Histogram Test for Specific Codes

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To test one 1 dollar chip, the upper limit is 1 second for the time you can spend. However, the test of the high-resolution low-speed ADC takes a long time, because of the following problems: (a) low-speed sampling, (b)high-resolution (large number of codes). In this research, we aim to reduce the time taken for testing. This is important for mass production shipment of ADC.

By inputting a sinusoidal wave, the nonlinearity of the ADC can be tested using the histogram method. Instead of sampling all the digital output codes, it is possible to shorten the test time by sampling only the necessary range of codes.

The random sampling employs an asynchronous sampling clock for the measured waveform signal, and we consider the case that it is periodic and each sampling time from the phase zero of the measured waveform is measured and known. After many sampling data acquisitions, a waveform with one period can be reconstructed. Fig.1 shows the case that the input waveform is a sine wave. asaki et. al. investigated the relationship between f_{CLK} and f_{sig} to revealed a "golden ratio" that efficiently obtains all codes. [1]

In this paper, we investigate the relationship between f_{CLK} and f_{sig} and θ (the initial phase of f_{sig}) in order to enable samples of only the necessary range of codes.

Figs.2-5 show some examples. Histograms are drawn from sampled sine waves. The vertical axis represents the number of sampled data and the horizontal axis represents digital output code. The number of sample points is the same in all figures. All codes are obtained equally in Fig.2. As shown in Figs. 3-5, when the relationship between f_{CLK} and f_{sig} are changed, only specific codes are obtained. The position of the code depends on θ.

The following tasks are future work: (a) formulation of the relationship between f_{CLK} and f_{sig} and θ (b) quantitatively evaluate how short the test time is reduced.

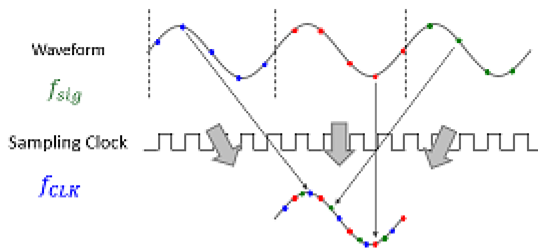

Fig.1 Random Sampling

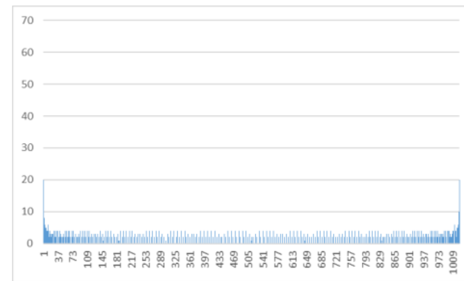

Fig.2 $f_{sig} \approx f_{CLK}$, $\theta = 0$

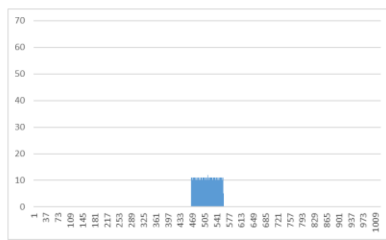

Fig.3 $f_{sig} \approx 3.1415 \times f_{CLK}$ $\theta = 0$

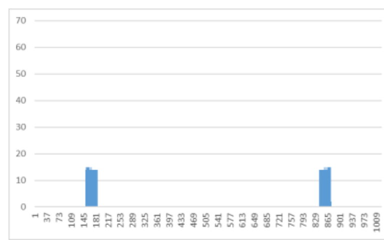

Fig.4 $f_{sig} \approx 3.1415 \times f_{CLK}$ $\theta = \pi/2 \times 0.5$

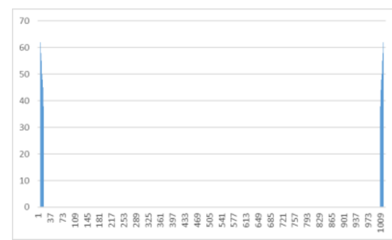

Fig.5 $f_{sig} \approx 3.1415 \times f_{CLK}$ $\theta = \pi/2 \times 0.9$

References

[1] Yuto Sasaki, Yujie Zhao, Anna Kuwana and Haruo Kobayashi, "Highly Efficient Waveform Acquisition Condition in Equivalent-Time Sampling System", 27th IEEE Asian Test Symposium, Hefei, Anhui, China (Oct. 2018)