### Background

**Research Target**

- Short time, high quality testing of high resolution, low speed analog-to-digital converter (ADC)

![ADC Diagram](image)

**Background**

- Internet of Things (IoT)
  - Everything is connected to internet.
  - Exchange information
  - Process, analyze data on the server.

Sensor interface ADC is a key.

**ADC Histogram Test**

- ADC test with high precision linearity
- But it takes long time

### Overview

**Sinewave Sampling**

- Shorten ADC test time by sampling only necessary range of codes.

**Our Approach**

- Realize by setting proper relationship among $f_{CLK}$, $f_{sig}$ and $\theta$ (initial phase)

### Result

#### Simulation Setting (1)

$$f_{CLK} = f_{sig} \times \frac{x + 1}{x}$$

- $f_{CLK} = \frac{f_{sig}}{100000 + 1} = 1.00001f_{sig}$

Relationship between $f_{CLK}$ and $f_{sig}$ changes scope of bin.

![Simulation Setting (1) Diagram](image)

#### Simulation Result (1)

- $\theta = 0$
  - $480, 513$

- $\theta = \pi/2 \times (-0.1)$
  - $401, 432$

- $\theta = \pi/2 \times (-0.3)$
  - $252, 280$

$\theta$ changes position of bin.

#### Simulation Setting (2)

- $f_{CLK} = f_{sig} \times \frac{100000}{2(100000 + 1)} = 2.00002f_{sig}$

![Simulation Setting (2) Diagram](image)

#### Simulation Result (2)

- $\theta = 0$
  - $480, 545$

- $\theta = \pi/2 \times 0.2$
  - $354, 385$
  - $640, 671$

- $\theta = \pi/2 \times 0.4$
  - $212, 238$
  - $787, 813$

### Summary

We investigate relationship among $f_{CLK}$, $f_{sig}$ and $\theta$ (initial phase of waveform) in order to sample only necessary range of codes.

Future work:

(a) Formulation of relationship among $f_{CLK}$, $f_{sig}$ and $\theta$
(b) Quantitatively evaluation of test time reduction.