TIME-TO-DIGITAL CONVERTER ARCHITECTURES USING TWO OSCILLATORS WITH DIFFERENT FREQUENCIES

Kosuke Machida Yuki Ozawa Yudai Abe Haruo Kobayashi
Division of Electronics and Informatics, Graduate School of Science and Technology,
Gunma University, 1-5-1 Tenjin-cho, Kiryu 376-8515, Japan
t14304108@gunma-u.ac.jp t13304037@gunma-u.ac.jp t15304003@gunma-u.ac.jp koba@gunma-u.ac.jp

ABSTRACT

This paper proposes time-to-digital converter (TDC) architectures using two asynchronous oscillators with different frequencies; each starts oscillation at different cycle at the rising timing of the corresponding input timing signal. We show here that by counting their oscillation start phase difference using digital counters, a highly linear stable time digitizer circuit can be realized. We propose two architectures using this principle: analog centric one and digital centric one. The analog centric one uses oscilloscope trigger circuits and the digital centric one uses ring oscillators. For analog centric one, its operation is stable but two external asynchronous sine signals are required. For digital centric one, all TDC circuits including the calibration can be implemented with full digital circuit. We present their configuration, operation and simulation verification.

Index Terms— Time-to-Digital Converter, Trigger Circuit, Vernier Ring Oscillator, Timing Measurement

I. INTRODUCTION

A time-to-digital converter (TDC) converts the time interval between two timing signals to digital data (Fig.1), and it is widely used as timing measurement BIST/BOST and ATE components [1-9]. The TDC circuit benefits from CMOS scaling down since it deals with signals in time domain instead of voltage domain and it often utilizes delay lines formed by array of delay units (buffers) [1]. However, their characteristics vary due to power supply voltage, temperature and process variations, and its overall linearity may degrade. Then their compensation circuits are often required.

This paper introduces two TDC architectures: analog and digital centric ones. Both of them employ two asynchronous oscillators with different frequencies but without analog delay lines. They can obtain high linearity with simple circuit; significant reduction of the amount of buffers and DFFs as well as power compared to the flash TDC.

(i) Analog centric one uses oscilloscope analog trigger circuits [10, 11] and requires two asynchronous external sine signals. Its advantage is stable operation without calibration.

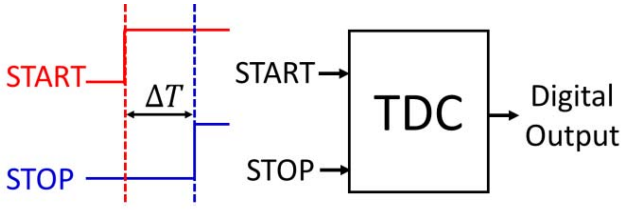


Fig.1. Role of TDC

(ii) Digital centric one uses two ring oscillators and requires one external reference clock, with which the frequencies of the ring oscillators can be measured together with a counter. All of the circuits can be implemented with full digital circuits; digital FPGA implementation is also possible.

II. CONVENTIONAL FLASH TDC ARCHITECTURE

The basic form of a TDC circuit is the flash TDC (Fig.2, [1]) and it is made up of a delay line (formed by buffers) and DFFs where each D-input is connected with the corresponding buffer output. Two timing signals are input to the start and stop terminals. The start signal goes through buffers each by each and is slowed by a time equal to the number of buffers multiplied by the delay time of each buffer. The stop signal is input to the clock terminal in each DFF in order to recognize the time sequence of the start and stop signals. If the delayed start signal is still in front of the stop signal at rising edge, the output of DFF is 1 since the start signal turns from 0 to 1 before the stop signal does. If the start signal is delayed too much and unable to catch up with the stop signal, the output of the corresponding DFF shows 0. In this way the array of outputs become a thermometer code and the critical buffer shows the number of buffers that is equal to the time interval of two signals.

In order to construct an n-bit flash TDC, a number of $(2^n - 1)$ buffers and DFFs are required. As a result, if we raise to a higher bit to reach a wider range of timing measurement, the number of units would experience an exponential growth and these will cause large circuit area and power assumption. Also the flash TDC can only reach a time resolution equal to the delay time of the buffers used. The thermometer-to-binary encoder is used to convert the outputs of the DFF array in a

2377-5386/18/$31.00 ©2018 IEEE
DOI 10.1109/ATS.2018.00046

thermometer code to a binary number. Also the variations among delays lead to the overall TDC nonlinearity, which has to calibrate in many cases.

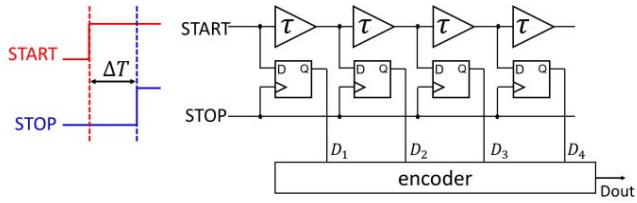


Fig.2. Flash TDC configuration

III. PROPOSED TDC – ANANLOG CENTRIC

Fig. 3 shows our proposed TDC which consists of two trigger circuits, inverters, DFFs and two binary up-counters. The two step signals 'START' and 'STOP' have different start phases, and their start phase difference (or their oscillation start timing difference) is represented by $t_0 = t_2 - t_1 (> (1/2f_1))$. First, the oscilloscope trigger circuits [9,10] convert sine waves of three-phase alternating current to A_1 and A_2 (Fig. 4). A_1 and A_2 are expressed as follows:

$$A_1 = \begin{cases} 0 & (0 \le t \le t_1) \\ \frac{3\sqrt{3}}{2}\sin\{2\pi f_1(t-t_1)\} & (t_1 < t) \end{cases} \quad (1)$$

$$A_2 = \begin{cases} 0 & (0 \le t \le t_2) \\ \frac{3\sqrt{3}}{2}\sin\{2\pi f_2(t-t_2)\} & (t_2 < t) \end{cases} \quad (2)$$

Fig. 4 shows a three-stage trigger circuit [11], where the input is a step signal and also sine waves of three-phase alternating voltages are provided. The output signal starts to oscillate at the rising timing of the step input with the same frequency as the three-phase alternating voltages, and Fig.5 shows its SPICE simulation results. Its operation in each mode of the track/hold circuit (Fig.5) is as follows:

Track mode:

$$\begin{aligned} V_{out} = \sin(2\pi ft + 4\pi/3)\{\sin(2\pi ft) - \sin(2\pi ft + 2\pi/3)\} \\ + \sin(2\pi ft)\{\sin(2\pi ft + 2\pi/3) \\ - \sin(2\pi ft + 4\pi/3)\} \\ + \sin(2\pi ft + 2\pi/3)\{\sin(2\pi ft + 4\pi/3) \\ - \sin(2\pi ft)\} = 0 \end{aligned}$$

Hold mode:

$$\begin{aligned} V_{out} = \sin(2\pi ft + 4\pi/3)\{\sin(2\pi ft_0) - \sin(2\pi ft_0 + 2\pi/3)\} \\ + \sin(2\pi ft)\{\sin(2\pi ft_0 + 2\pi/3) \\ - \sin(2\pi ft_0 + 4\pi/3)\} \\ + \sin(2\pi ft + 2\pi/3)\{\sin(2\pi ft_0 + 4\pi/3) \\ - \sin(2\pi ft_0)\} = \frac{3\sqrt{3}}{2}\sin\big(2\pi f(t-t_0)\big) \end{aligned}$$

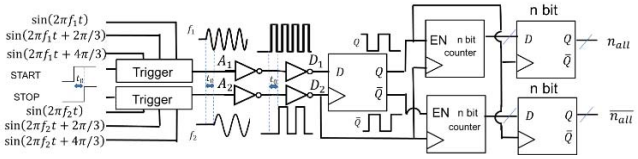


Fig. 3. Proposed analog centric TDC architecture

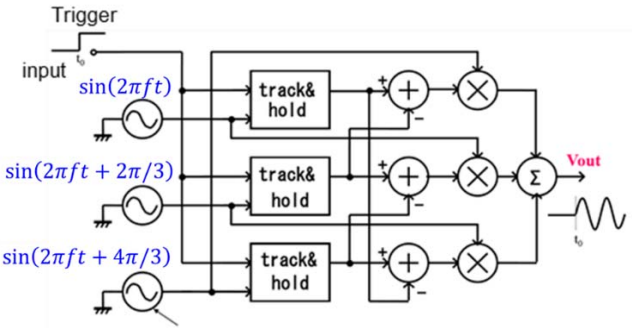


Fig. 4. Three-stage configuration trigger circuit

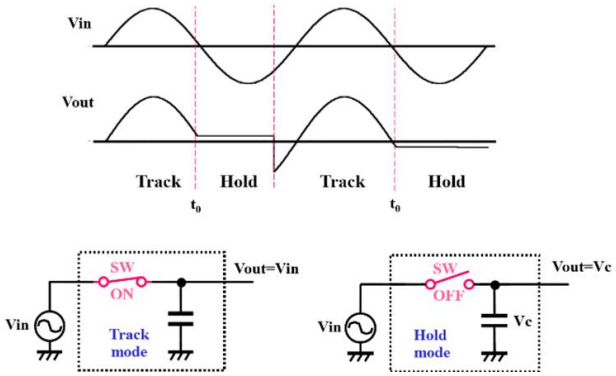


Fig. 5. Track/hold circuit

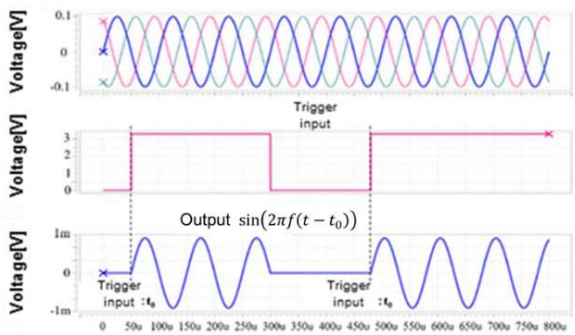


Fig.6 Simulation results of the trigger circuit in Fig. 5

The inverters convert A_1 and A_2 to D_1 and D_2 respectively, and they are shown as follows:

$$D_1 = \begin{cases} 1 & (A_1 > 0) \\ 0 & (A_1 \le 0) \end{cases} \quad (3)$$

$$D_2 = \begin{cases} 1 & (A_2 > 0) \\ 0 & (A_2 \leq 0) \end{cases} \quad (4)$$

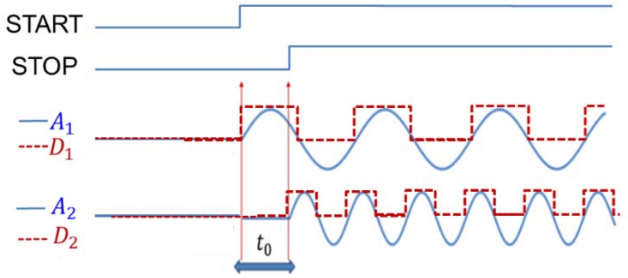


Fig. 7. A_1, A_2, D_1 and D_2 start to oscillate with different frequencies at the rising timing edges of START and STOP signals respectively.

D_1 is fed to D in a DFF, whereas D_2 is provided as a clock. f_1 and f_2 are defined as frequencies of A_1 and A_2 respectively ($f_1 \neq f_2$). Fig. 7 shows that the DFF latches the value of D_1 at the clock rising timing.n_{all} represents the number of 1's, whereas $\overline{n_{all}}$ represents the number of 0's.

In the proposed circuit, we can finally obtain n_{all} and $\overline{n_{all}}$. Q is a beat wave, which consists of D_1 sampled by clock D_2. These are waves with the frequency of $|f_2 - f_1|$. n_{beat} is points included by Q's one period. The more n_{beat} is present, the higher linearity is obtained. n_{beat} is defined as follows:

$$n_{beat} = \frac{f_2}{|f_2 - f_1|} \quad (5)$$

Binary up-counters increment its output value every clock when the enable signal is 1, whereas its output value holds its current value when the enable signal is 0. Finally, we use n-bit registers with clock Q. By using Q as a clock, a fixed value can be obtained at any time when the operation is ended.

When the input is Q of the DFF in Fig.3, the number of n_{all} is counted, whereas in the case of $\bar{Q}$, the number of $\overline{n_{all}}$ is counted. The number of points to be measured determine the number of required full adders and DFFs.

D_1 and D_2 have different periods from one rising timing to another rising timing. It can be expressed as t' as follows (Fig. 8) :

$$t' = \left|\frac{1}{f_2} - \frac{1}{f_1}\right| \quad (6)$$

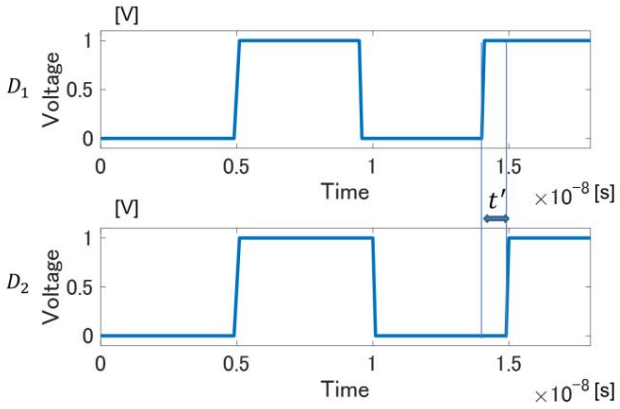


Fig. 8. Period difference between D_1 and D_2

Fig. 9 shows an example of deviation points when t_0 are 0[s] and 3[ns]. When this deviation is expressed by n_{all}, $\overline{n_{all}}$ and n_{beat}, deviation and t' give t_0 as follows :

$$t_0 = \begin{cases} (\overline{n_{all}} - n_{all})t' & (\text{in case } f_1 > f_2) \\ \{n_{beat}/2 - (\overline{n_{all}} - n_{all})\}t' & (\text{in case } f_1 < f_2) \end{cases} \quad (7)$$

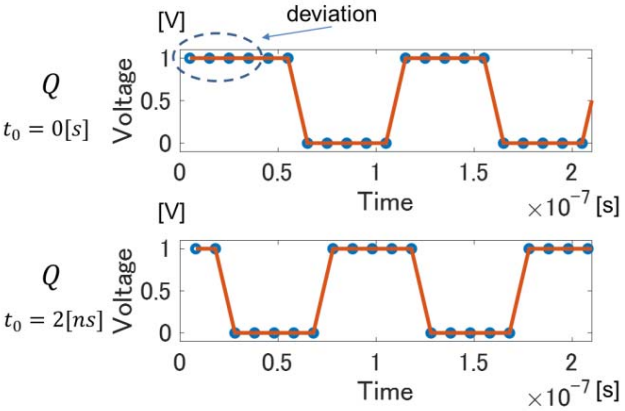
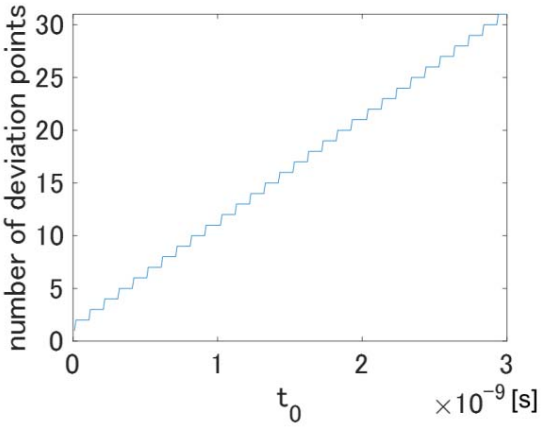
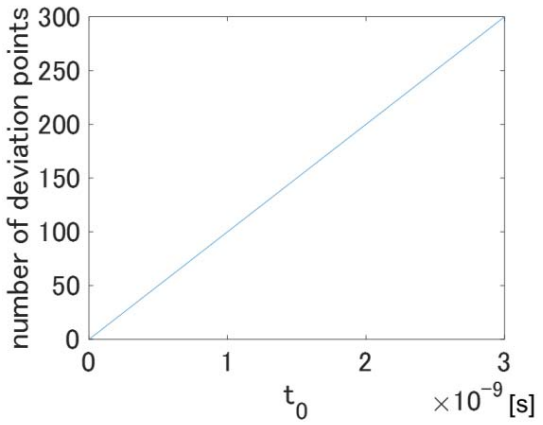


Fig. 9. Example of deviation of points $f_1 > f_2$

Fig. 10 shows the simulation results of the proposed TDC circuit and we see that it operates correctly as expected.



$(a) f_1 = 99[MHz],\ f_2 = 100[MHz]$



$(b) f_1 = 99.9[MHz], f_2 = 100[MHz]$

Fig.10. Linearity of TDC with given frequencies

Fig. 11 shows the RMS (Root Mean Squared) error of t_0 with respect to the number of $n_{beat}/2$. RSM error shows as follows:

$$\text{RMS error of } t_0 = \sqrt{\frac{1}{n_{beat}/2}\sum_{i=1}^{n_{beat}/2}(t_i)^2} \qquad (8)$$

t_i shows deviation between set t_0 and calculated t_0. As the number of $n_{beat}/2$ increases, the error of t_0 becomes smaller. We see that the proposed TDC linearity can be improved as the number of $n_{beat}/2$ increases. The simulation conditions are as follows;

(a) $f_1 = f_2\frac{2N+1}{2N}[Hz], f_2 = 100[MHz], t_0 = 1[ns]$

(b) $f_1 = f_2\frac{2N-1}{2N}[Hz], f_2 = 100[MHz], t_0 = 1[ns]$

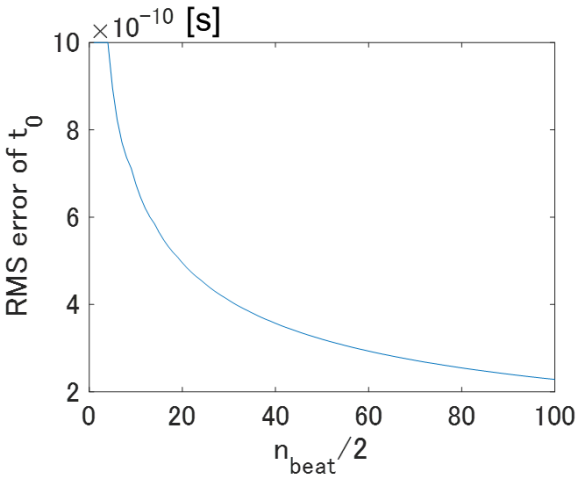


Fig. 11. RMSE of t_0 with respect to the number of $n_{beat}/2$ (in case of $f_1 > f_2$)

SPICE simulations have been also performed for the proposed circuit, and its operation has been verified.

This section has shown an analog centric TDC architecture with fine time resolution and high linearity; it employs trigger circuits, and some simulation results validate our proposed TDC architecture. We could obtain the start phase difference of the sine wave with different frequencies from the simulation results using the proposed circuit. In this circuit, we do not have to use analog delay array (buffer delay line) like conventional TDC architecture, so that the proposed TDC linearity can be easily secured. Future tasks are to perform simulations of the entire proposed TDC including the trigger circuits.

IV. PROPOSED TDC – DIGITAL CENTRIC

The trigger circuit in Fig. 9 includes some analog circuits which are difficult to implement with a digital FPGA. This paper describes the digital centric configuration. We propose here to replace two trigger circuits with two ring oscillators, each of which starts to oscillate at the rising edge timing of the corresponding "signal" in Fig. 12. The frequencies of the two ring oscillators can be designed to be different with different numbers of delay gates, and also their frequencies are measured with a reference clock and a counter.

A ring oscillator consists of an odd number of inverters. A delay element consists of an even number of inverters. As shown in Fig. 12, the delay time of one delay element is τ, and the total delay time of the inverter and the AND gate is τ_i. When "signal" rises from 0 to 1, it starts to oscillate with the periodic time T_{RO} expressed as follows:

$$T_{RO} = 2(n\tau + \tau_i)$$

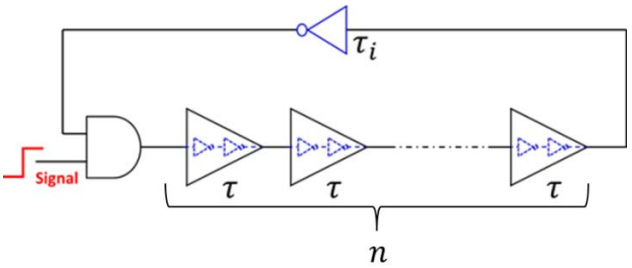


Fig.12. Ring oscillator with an oscillation start signal.

Fig.13 shows proposed digital centric TDC configuration. Digital centric TDC consists of asynchronous oscillators with different frequency, a DFF and 4 binary up-counters. Each of 4 binary up-counters counts the number of counter1 (Number of oscillation of START signal), counter2(Number of oscillation of STOP signal), counter3 (Number of 1) and counter4 (Number of0).

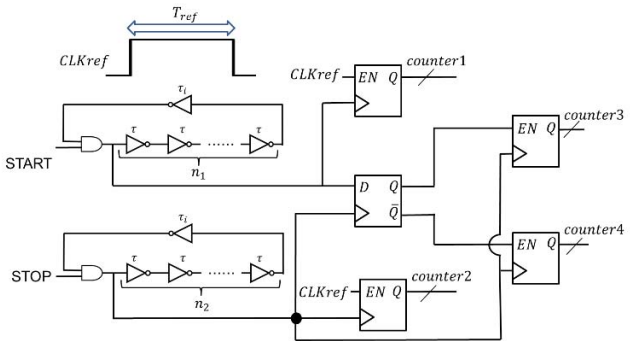


Fig. 13. Proposed digital centric TDC architecture

Using ring oscillator, START frequency f_1 and STOP frequency f_2 ($f_1 > f_2$) is as follow :

$$f_1 = \frac{1}{T_{Ro1}} = \frac{counter1}{T_{ref}} \quad (9)$$

$$f_2 = \frac{1}{T_{Ro2}} = \frac{conuter2}{T_{ref} - t_0} \quad (10)$$

counter1 and counter2 are sampling point for T_{ref}. The longer the sampling time is, the more accurate frequency measurement can be performed. Fig.14 shows the relationship between the measurement time and the calculated frequency. Simulation was performed with MATLAB. From this Fig, it can be seen that as the measurement time gets longer, the value satisfies the set frequency. Using Eq. (6)(7)(9)(10), t_0 is given as follows:

$$t_0 = \frac{(\text{counter4} - \text{counter3})(\text{counter1} - \text{counter2})T_{ref}}{counter1\{conuter2 + (\text{counter4} - \text{counter3})\}} \quad (11)$$

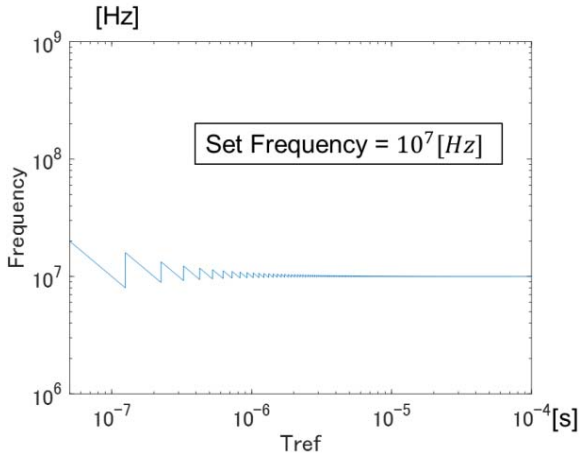


Fig.14 Relationship between the measurement time and the calculated frequency

We carry out simulation verification for digital centric type TDC with LTspice and MATLAB. The simulation conditions are as follows.

$$t_0 = 2[ns], T_{Ro1} = 10[ns], T_{Ro2} = 10.1010[ns]$$

Fig.15 is (a) counter3 and (b) counter4 outputs. When $T_{ref} = 2.4[\mu s]$, deviation point is :

$$\text{counter4} - \text{counter3} - 1 = 101 - 80 - 1 = 20.$$

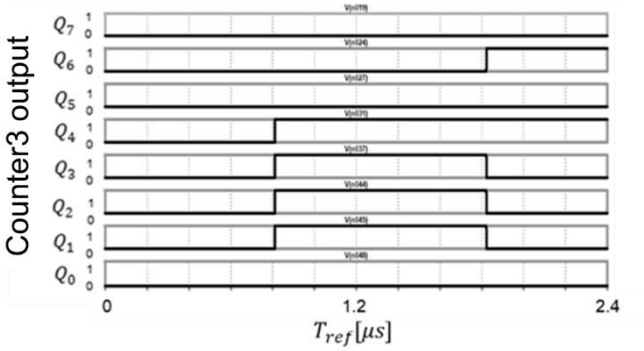


Fig.15(a) Sampling point of counter3

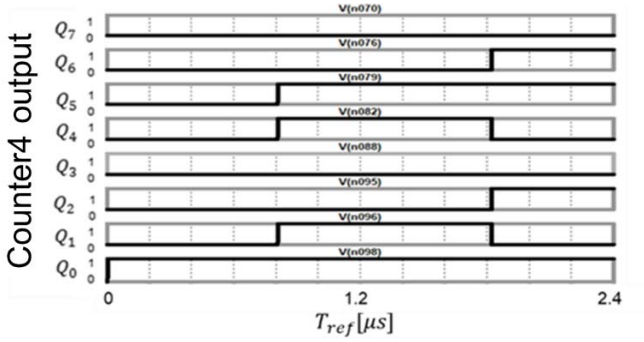


Fig.15(b) Sampling point of counter4

Fig.16 MATLAB Simulation When $T_{ref} = 0.1[ms]$, sampling point are $counter1 = 10^4, counter2 = 9.9 * 10^3$. .

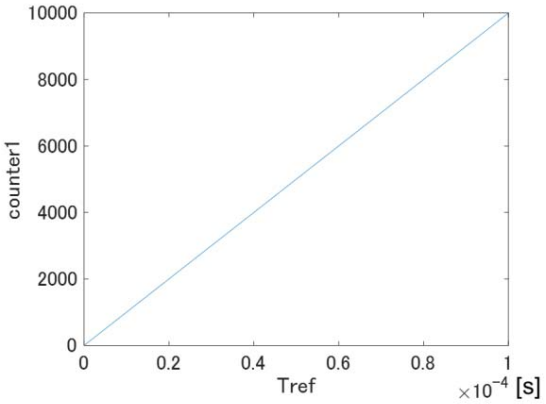


Fig.16(a) Number of sampling points of $counter1$

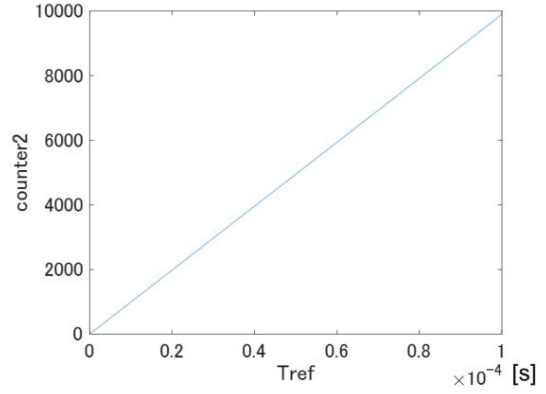


Fig.16(b) Number of sampling points of $counter2$

Using Eq.(11) and simulation results, t_0 is obtained as follows :

$$t_0 = \frac{20 * 100 * 10^{-4}}{10^4\{9.9 * 10^3 + 20\}} \approx 2.02[\text{ns}]$$

V. CONC LUSION

This paper has presented TDC architectures using two asynchronous oscillators with different frequencies; each starts oscillation at different cycle at the rising timing of the corresponding input timing signal. We have shown here that by counting their oscillation start phase difference using digital counters, a highly linear stable time digitizer circuit can be realized. We propose two architectures using this principle: analog centric one and digital centric one. The analog centric one uses oscilloscope trigger circuits and the digital centric one uses ring oscillators. For analog centric one, its operation is stable but two external asynchronous sine signals are required. For digital centric one, all TDC circuits including the calibration can be implemented with full digital circuit. We have shown their configuration/operation and simulation verification.

REFERENCES

[1] Y. Arai, T. Baba, “A CMOS Time to Digital Converter VLSI for High-Energy Physics”, IEEE Symposium on VLSI Circuits (1988).

[2] Y. Ozawa, T. Ida, S. Sakurai, S. Takigami, N. Tsukiji, R. Shiota, and H. Kobayashi, “SAR TDC Architecture With Self-Calibration Employing Trigger Circuit”, IEEE Asian Test Symposium, Taipei, Taiwan (Nov. 20017)

[3] R. Jiang, C. Li, M. Yang, H. Kobayashi Y. Ozawa, N. Tsukiji, M. Hirano, R. Shiota, K. Hatayama, "Successive Approximation Time-to-Digital Converter with Vernier-level Resolution", IEEE International Mixed-Signal Testing Workshop, Catalunyna, Spain (July 2016).

[4] J. Lee and Y. Moon, “A Design of Vernier Coarse-Fine Time-to-Digital Converter Using Single Time Amplifier”, J. of Semiconductor Technology and Science, vol.12, no. 4 (Dec. 2012).

[5] G. S. Jovanovi´c, M. K. Stoj˘cev, “Vernier’s Delay Line Time–to–Digital Converter”, Scientific Publications of the State University of Novi Pazar, Ser. A: Appl. Math Inform. and Mech. pp.11-20 (2009)

[6] S. Ito, S. Nishimura, H. Kobayashi, et al., “Stochastic TDC Architecture with Self-Calibration,” IEEE Asia Pacific Conf. Circuits and Systems, Kuala Lumpur, Malaysia (Dec. 2010).

[7] T. Chujo, D. Hirabayashi, K. Katoh, C. Li, Y. Kobayashi, J. Wang, K. Sato, H. Kobayashi, “Experimental Verification of Timing Measurement Circuit With Self-Calibration”, IEEE International Mixed-Signal Testing Workshop, Brazil (Sept. 2014).

[8] T. Ida, Y. Ozawa, J. Richen, S. Sakurai, S. Takigami, N. Tsukiji, R. Shiota, H. Kobayashi, “Architecture of High Performance Successive Approximation Time Digitizer,” IEEE International Symposium on Intelligent Signal Processing and Communication Systems, Xiamen, China (Nov. 2017).

[9] Y. Ozawa, T. Ida, R. Jiang, S. Sakurai, S. Takigami, N. Tsukiji, R. Shiota, H. Kobayashi, “SAR TDC Architecture with Self-Calibration Employing Trigger Circuit,” IEEE Asian Test Symposium, Taipei, Taiwan (Nov. 2017).

[10] S. Sakurai, S. Takigami, T. Ida, Y. Ozawa, N. Tsukiji, Y. Kobori, H. Kobayashi, R. Shiota, “Study of Multi-Stage Oscilloscope Trigger Circuit,” IEEE International Symposium on Intelligent Signal Processing and Communication Systems, Xiamen, China (Nov. 2017)

[11] M. Nelson, “A New Technique for Low-Jitter Measurements Using Equivalent-Time Sampling Oscilloscope”, Automatic RF Techniques Group 56th Measurement Conference - Metrology and Test for RF Telecommunications, Boulder, Colorado (Dec. 2000).