Oct. 18, 2018
Session 6B-II
Mixed-Signal IC Designs and ATE

Time-to-Digital Converter Architectures Using Two Oscillators With Different Frequencies

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Research Objective

Investigation of TDC architectures
with Verner oscillators

- Analog centric one
  - Using trigger circuits
  - Two oscillators with different frequencies
  - No self-calibration required

- Digital centric one
  - Two ring oscillators
    with different frequencies

Outline

- Research Background
- Measurement Principle
- Analog Centric TDC
- Digital Centric TDC
- Discussion & Conclusion

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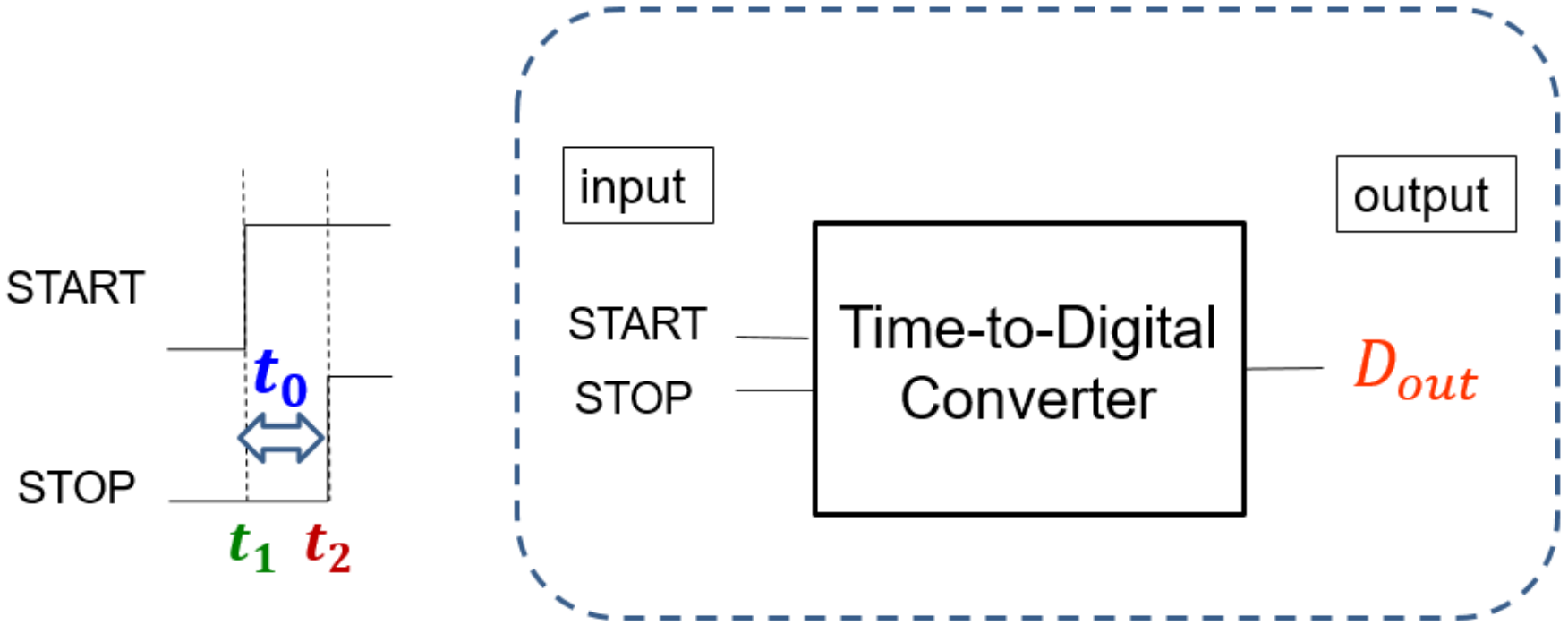
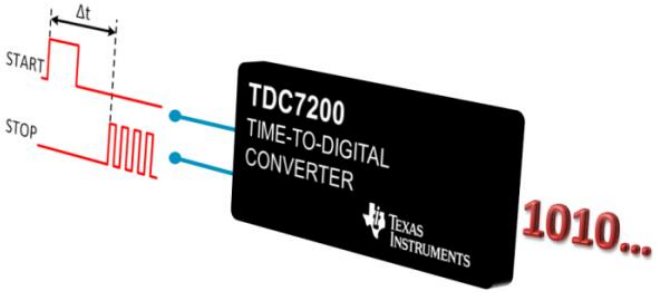
Time-to-Digital Converter

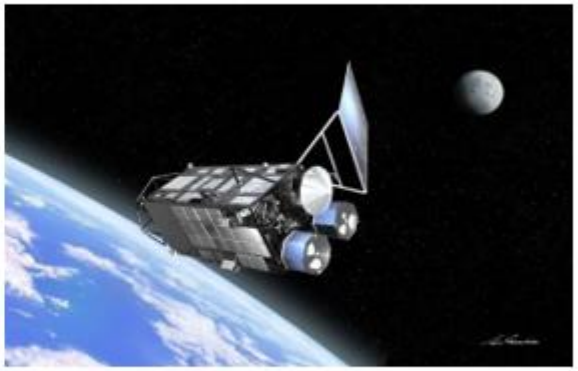


- Time-to-digital converter (TDC) measures **timing difference** t_0 between t_1 , t_2 as a **digital value** D_{out}

TDC Application Examples (1)



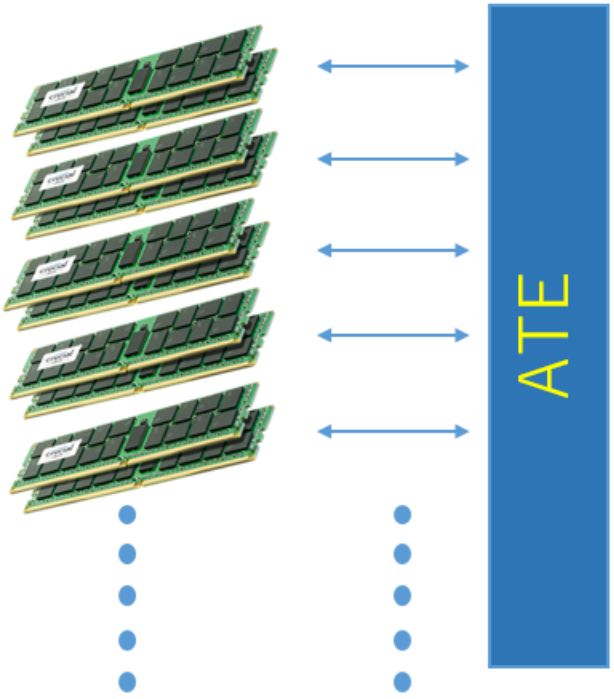
Inter-vehicular distance measurement



Satellite distance measurement

TDC Application Example (2)

Multi channels



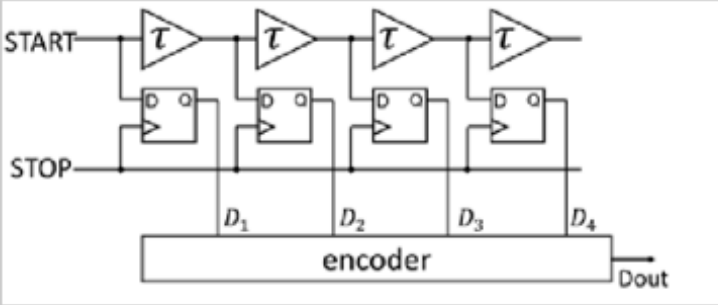
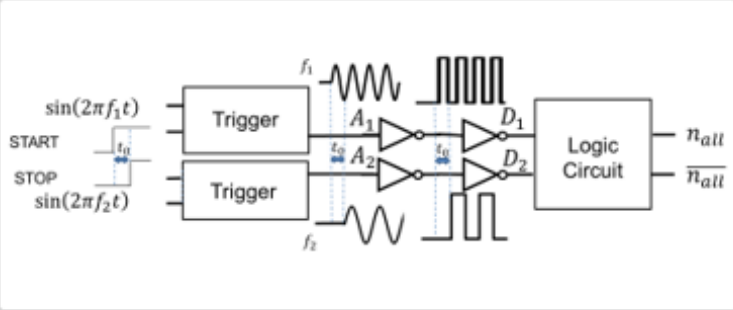
Large circuit × Large amounts

High test cost

Small circuit × Large amounts

Low test cost

Comparison of TDC Architectures

	Conventional TDC	Proposed TDC
Circuit Architecture		
Delay Line	Necessary	Not necessary
Self Calibration	Required	Not required

Delay array have variations → Self-calibration is required

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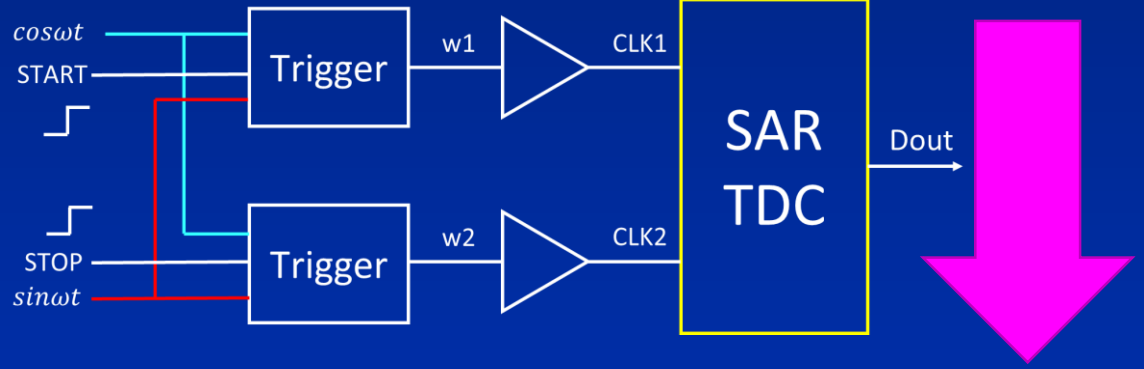
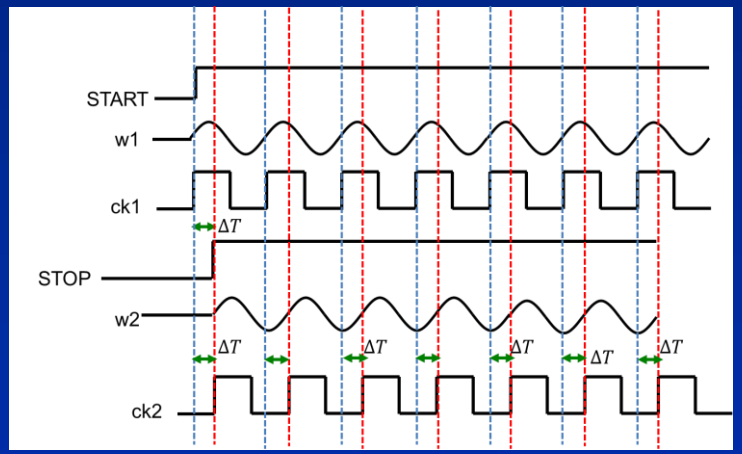
Myth and Truth of Time Signal

Myth

Voltage can be held

Time difference cannot be held

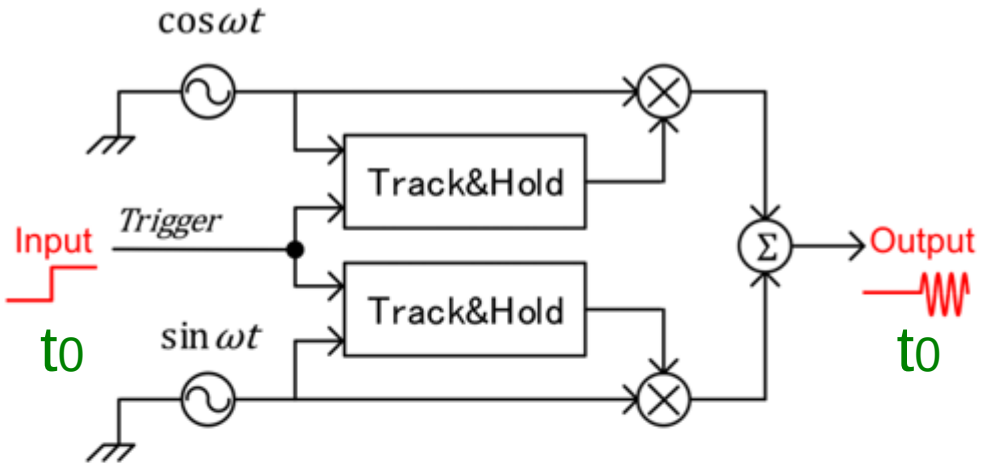


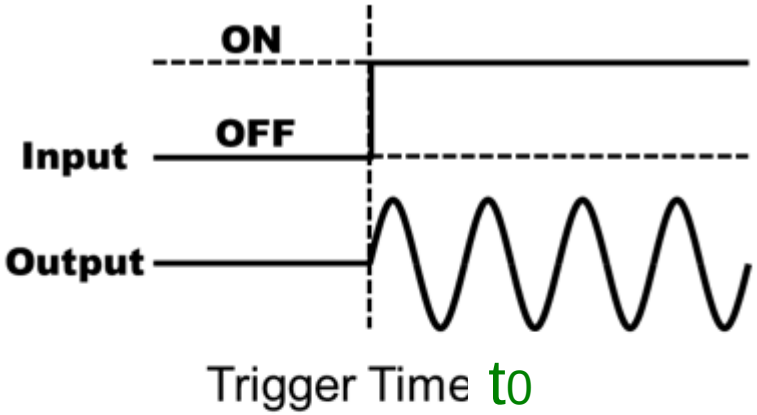


Truth

Time difference can be held !

Trigger Circuit

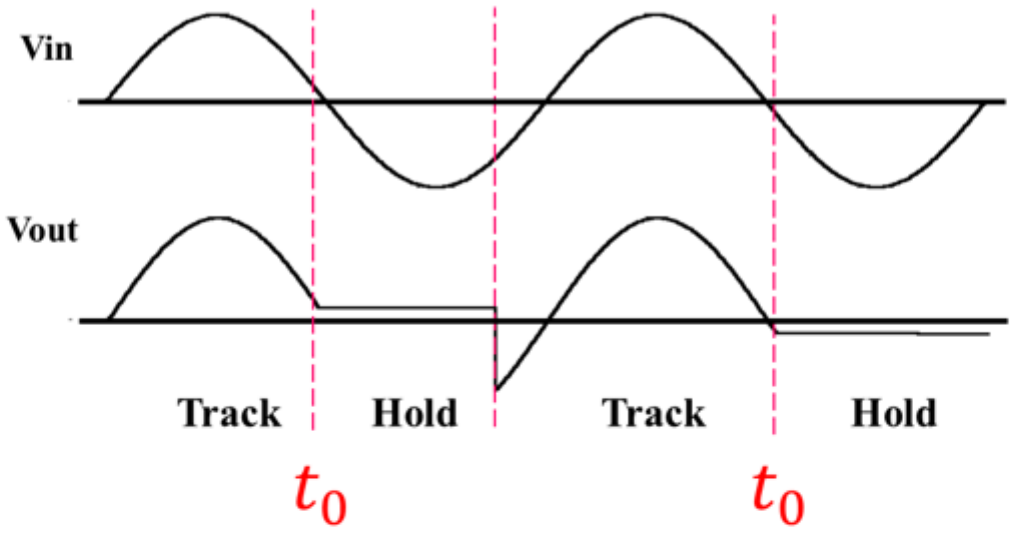


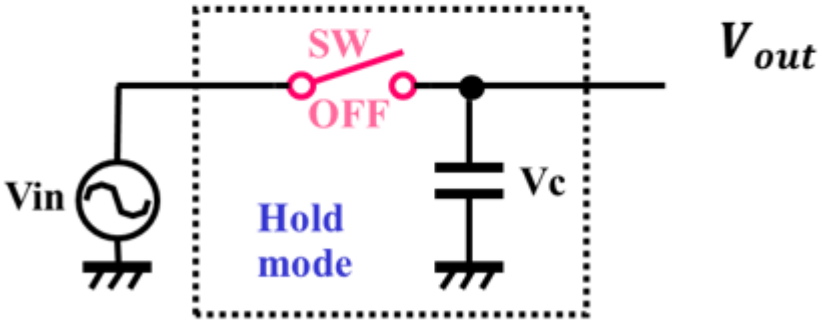


- Output starts to oscillate at rising timing edge of input
- Output waveform with no transient change

[1] M. Nelson (Tektronics) "A New Technique for Low-Jitter Measurements Using Equivalent-Time Sampling Oscilloscope", Automatic RF Techniques Group 56th Measurement Conference (Dec. 2000).

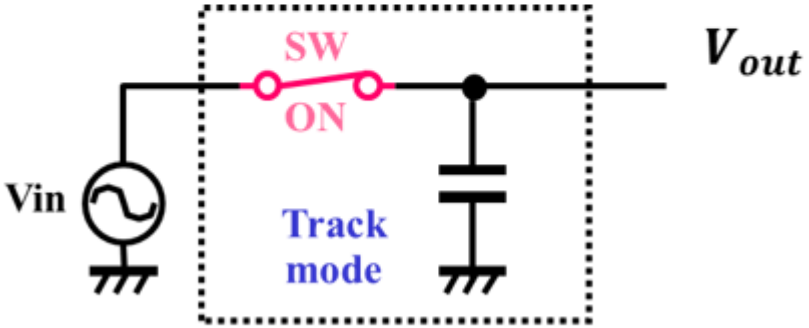
T/H Circuit





T / H circuit

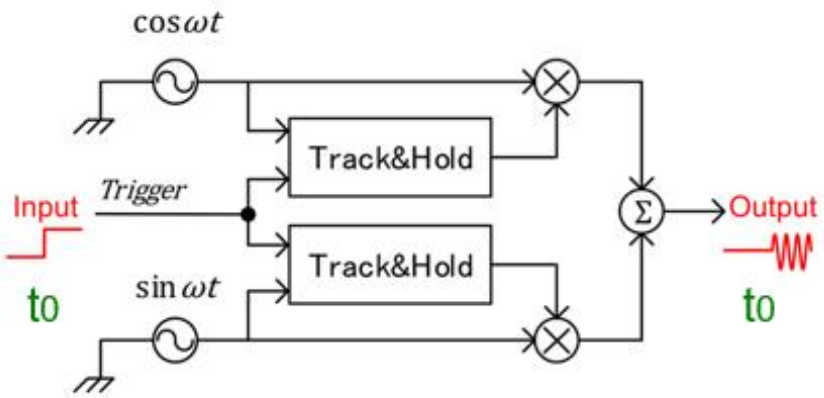
$V_C = V_{out}$

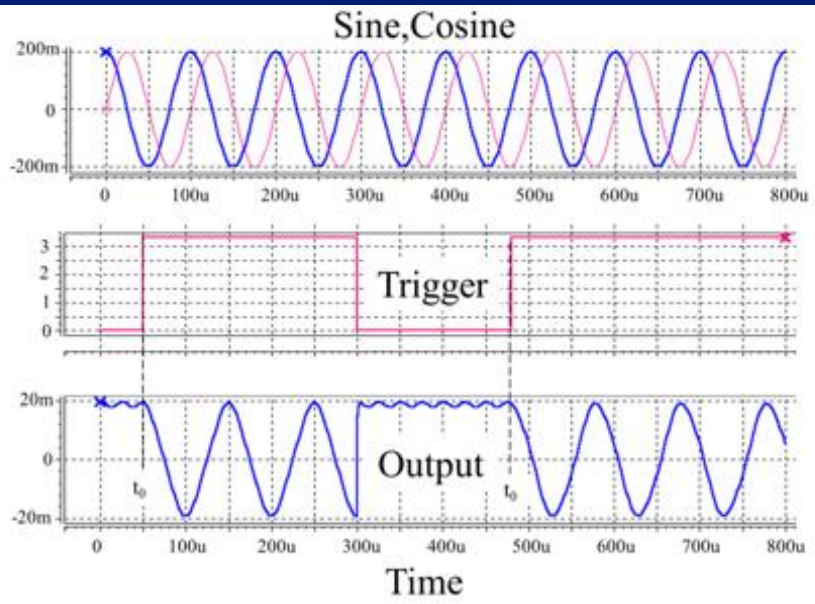


T / H circuit

$V_{in} = V_{out}$

Trigger Circuit Waveforms





T/H circuit

▪track mode

$$Vout=\cos(\omega t)\cos(\omega t)+\cos(\omega t+\pi/2)\cos(\omega t+\pi/2)$$

$$=\cos^2(\omega t)+\sin^2(\omega t)$$

$$=1$$

▪hold mode

$$Vout=\cos(\omega t)\cos(\omega t_0)+\sin(\omega t)\sin(\omega t_0)$$

$$=\cos(\omega(t-t_0))$$

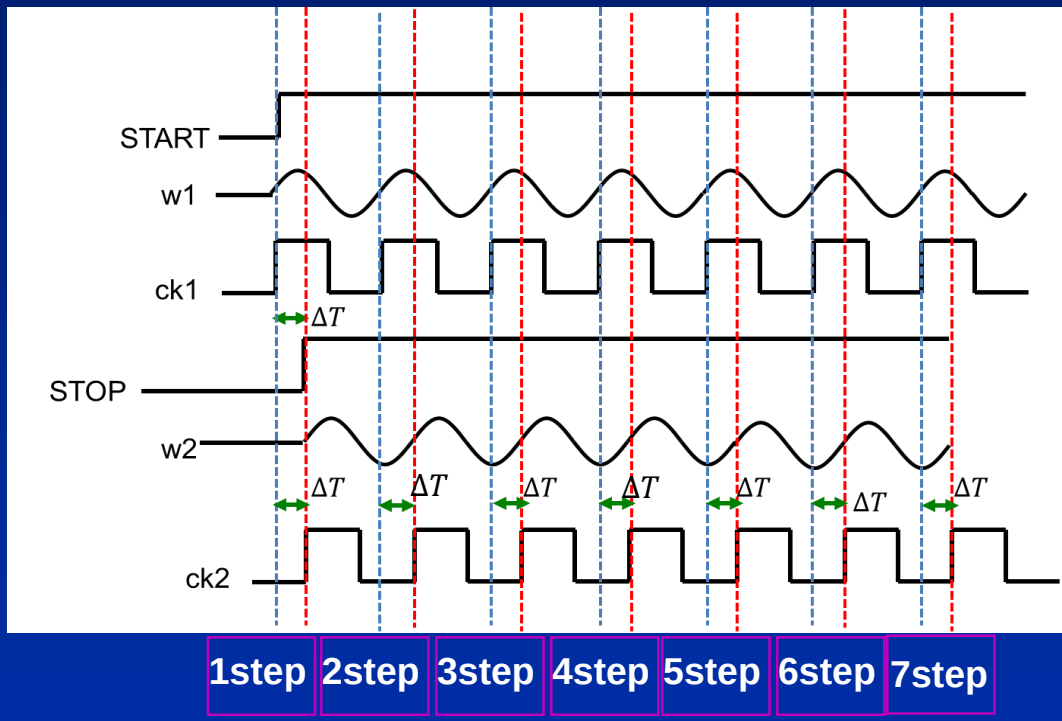
※ **trigger time:t_0**

One-shot Timing Measurement Using Trigger Circuit

Proposal

Input START, STOP signal

Oscillate with initial phase at input timing

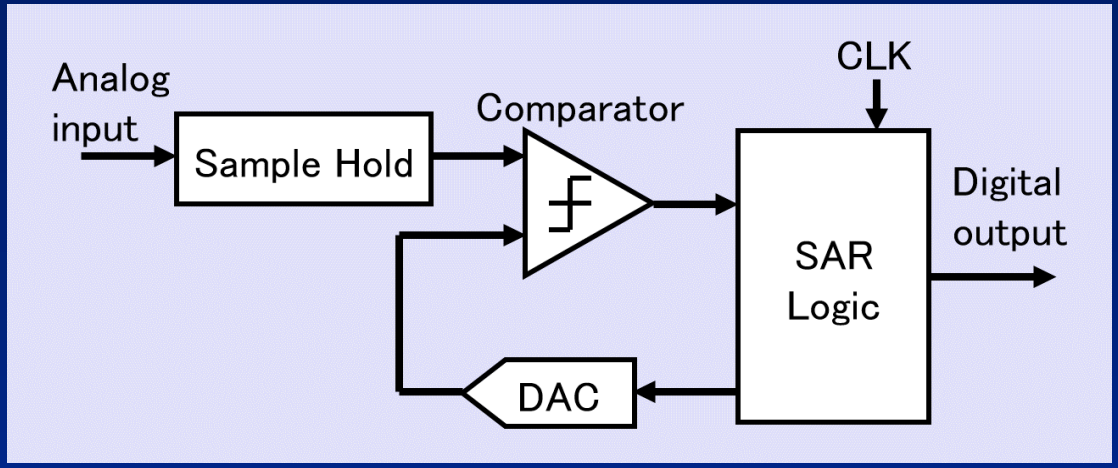


It can **hold the time difference** using two trigger circuits

SAR-ADC VS. SAR-TDC

SAR ADC :

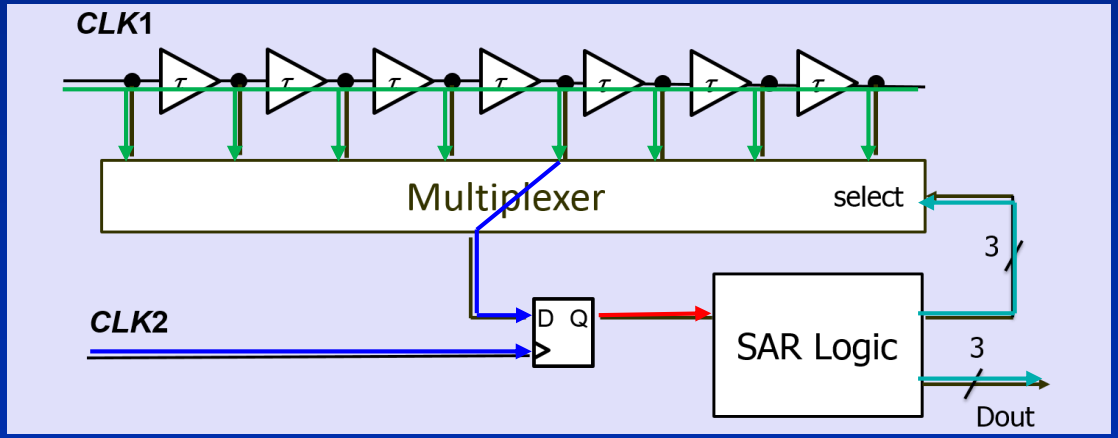
- **Comparator**
- **DAC**



SAR−ADC

SAR TDC :

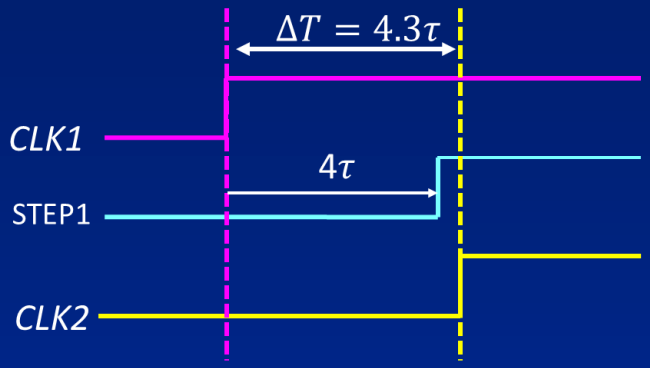
- **D-FF**
- **Delay line**

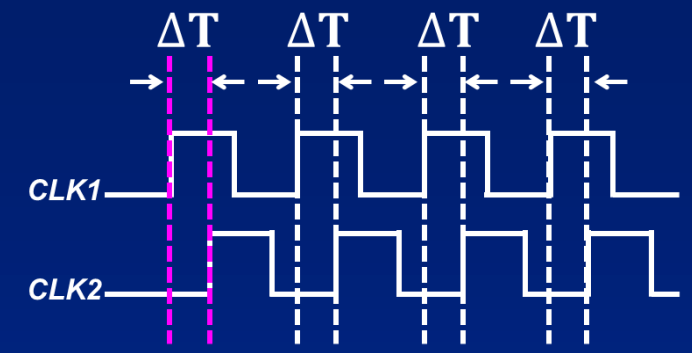


Y. Ozawa, H. Kobayashi, et. al.,
"SAR TDC Architecture with Self-Calibration Employing Trigger Circuit,"
IEEE Asian Test Symposium, Taipei (Nov. 2017).

SAR TDC Operation

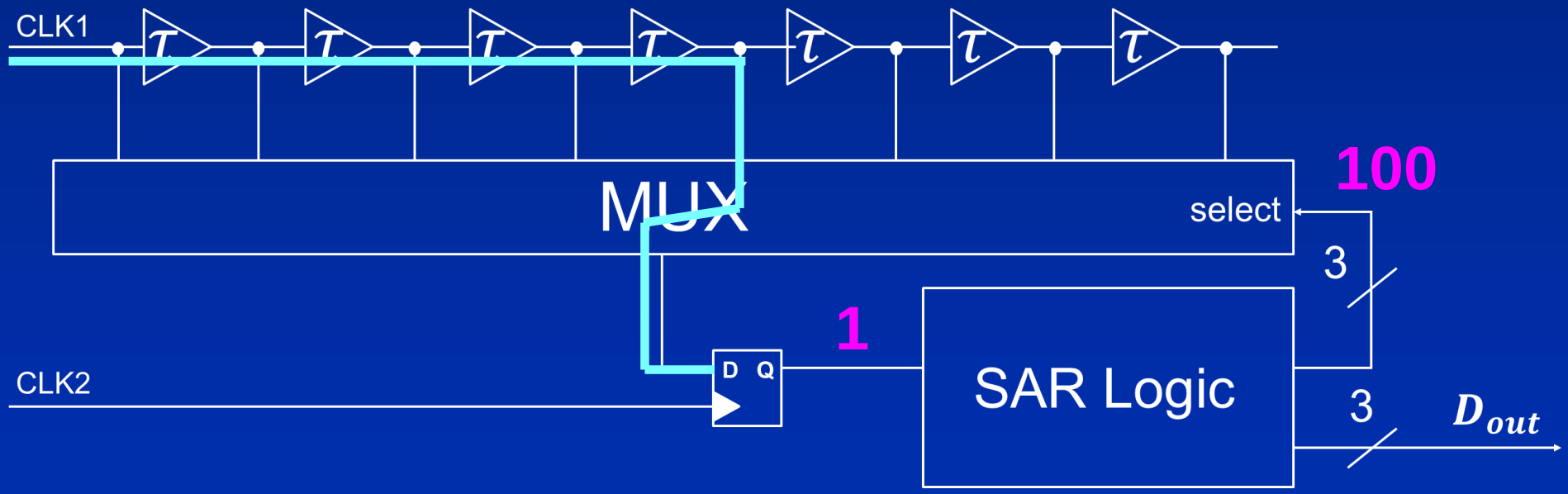
STEP1





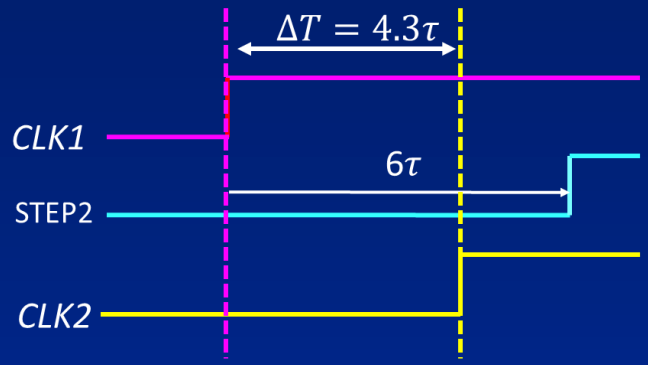
Example

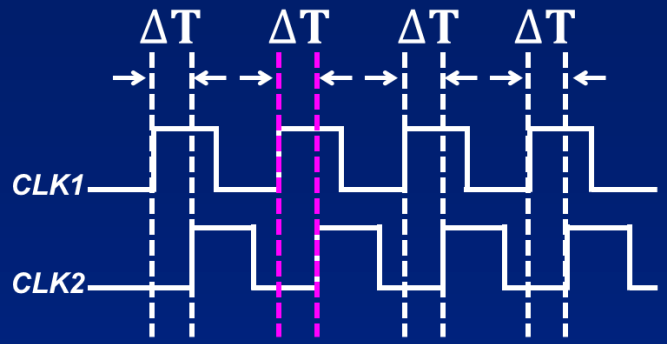
$\Delta T = 4.3\ \tau$



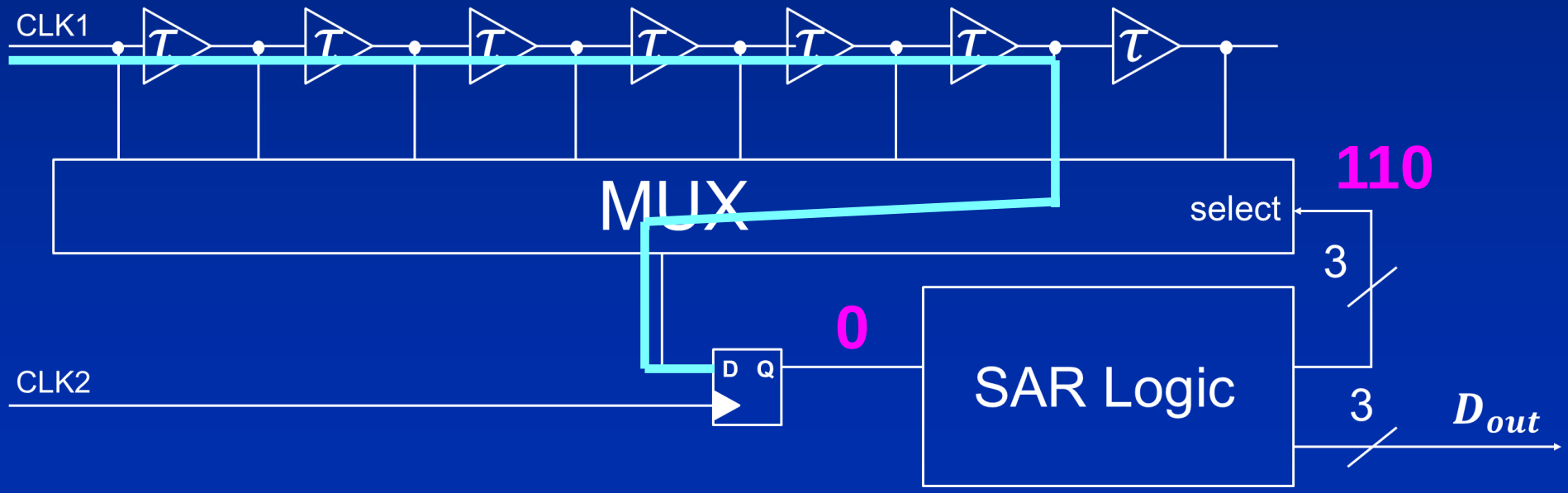
SAR TDC Operation

STEP2



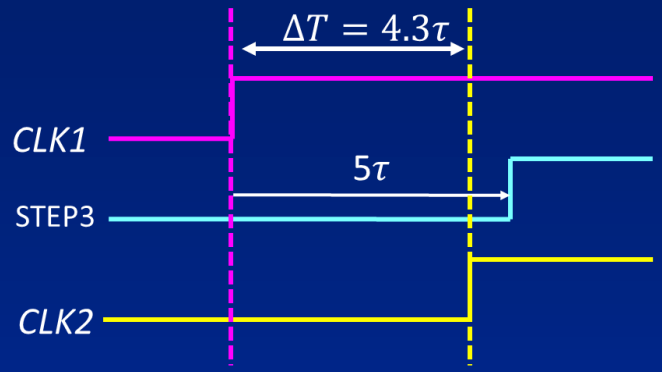


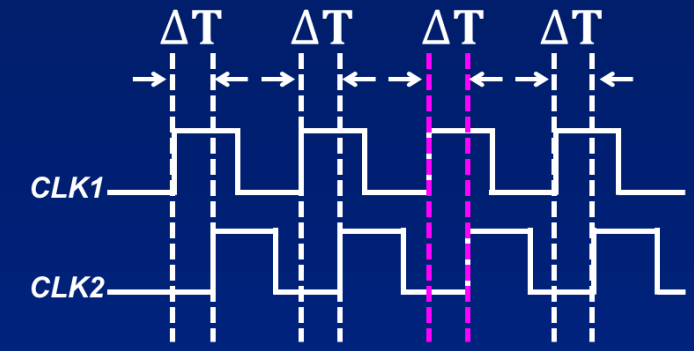
Example $\Delta T = 4.3\ \tau$



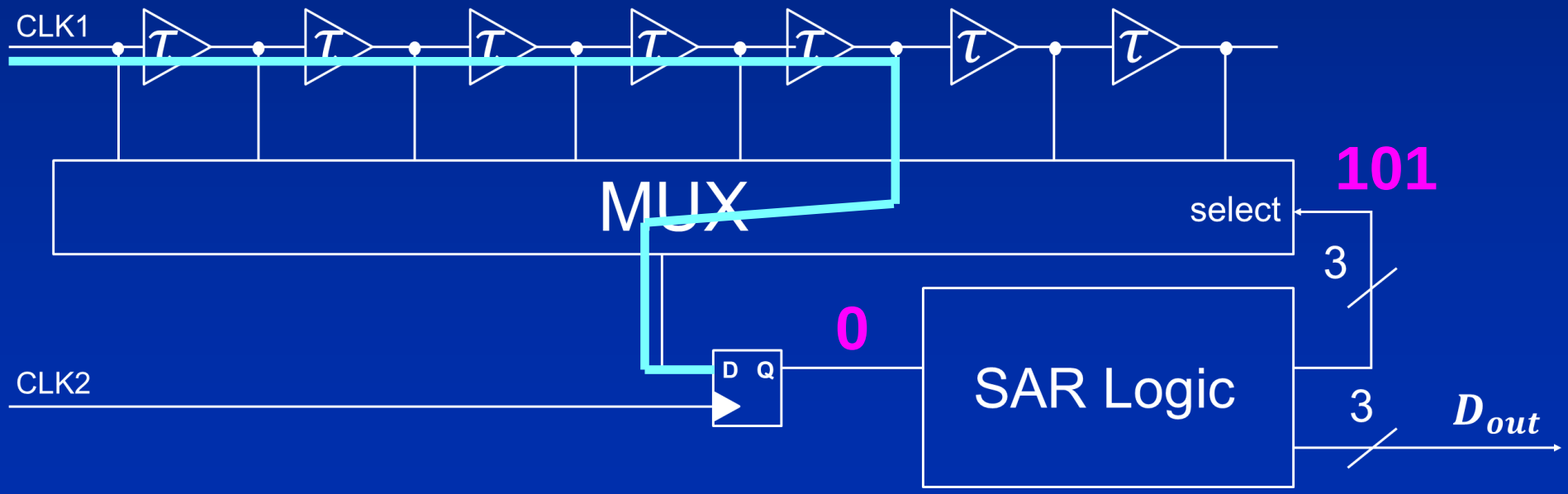
SAR TDC Operation

STEP3



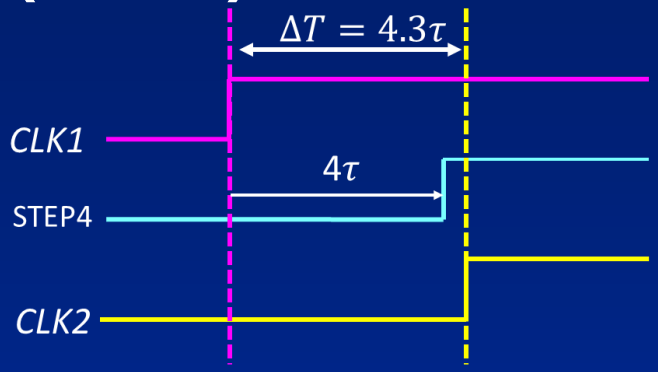


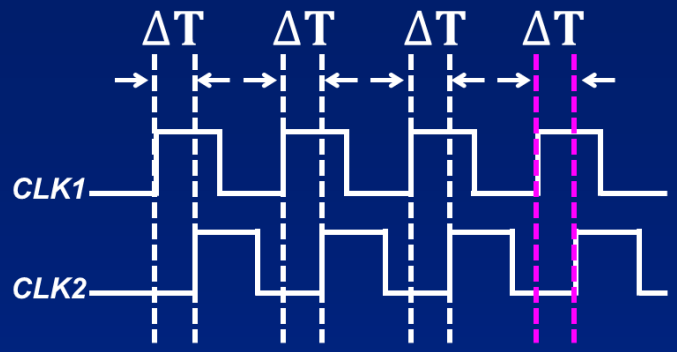
Example $\Delta T = 4.3\ \tau$



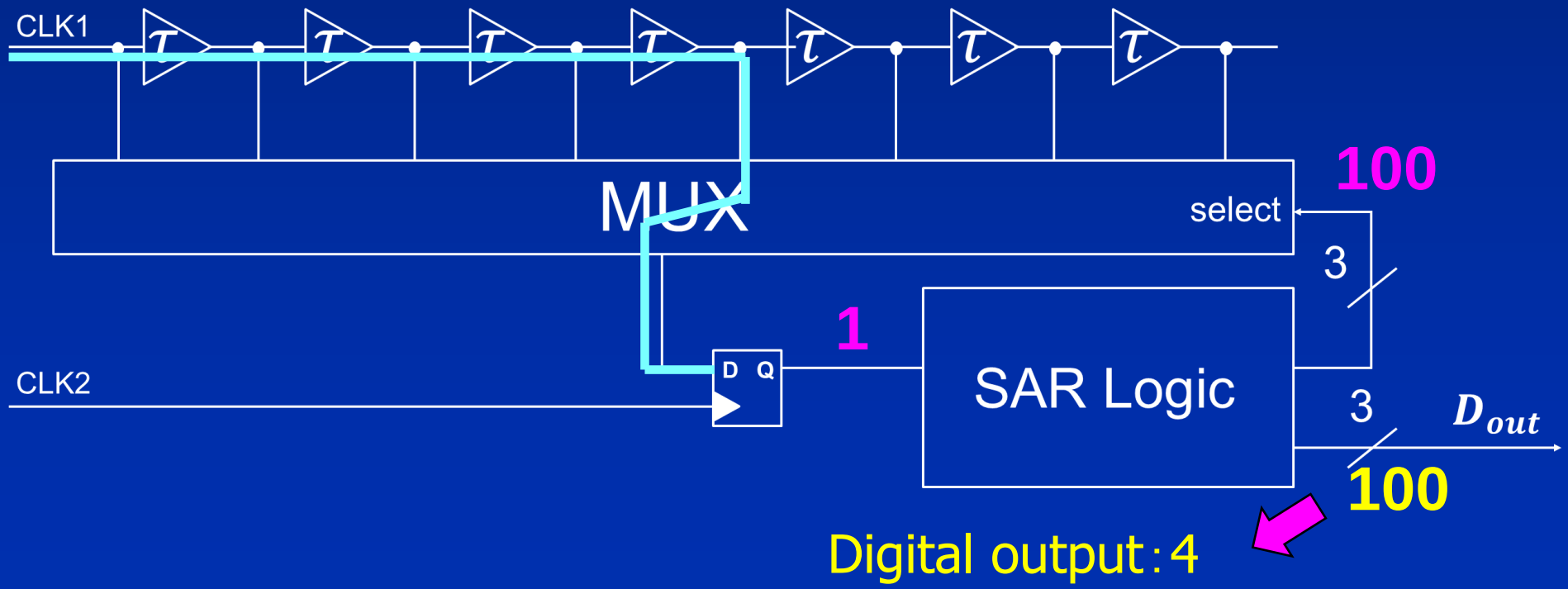
SAR TDC Operation

STEP4 (Stable)

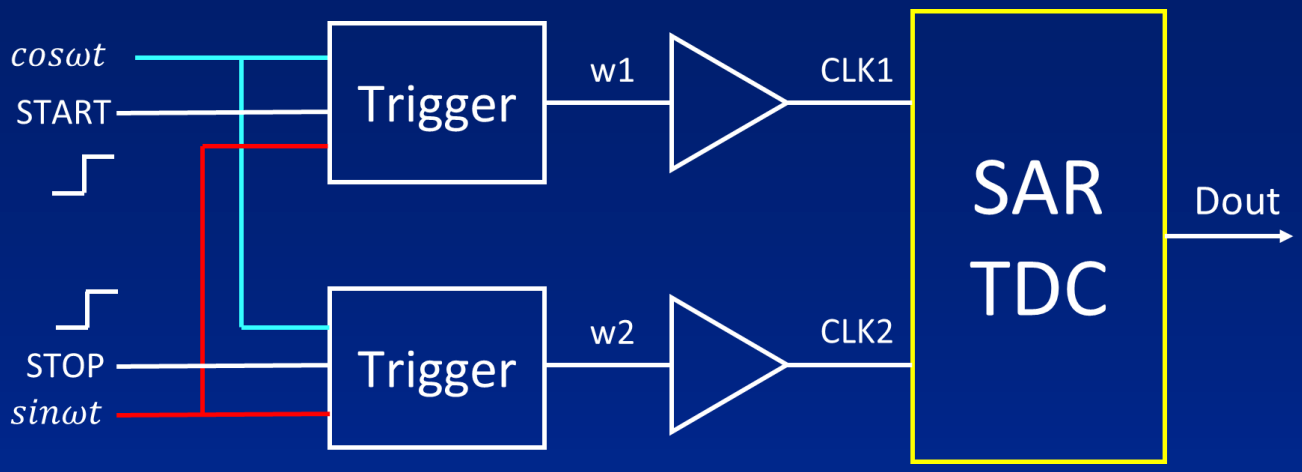


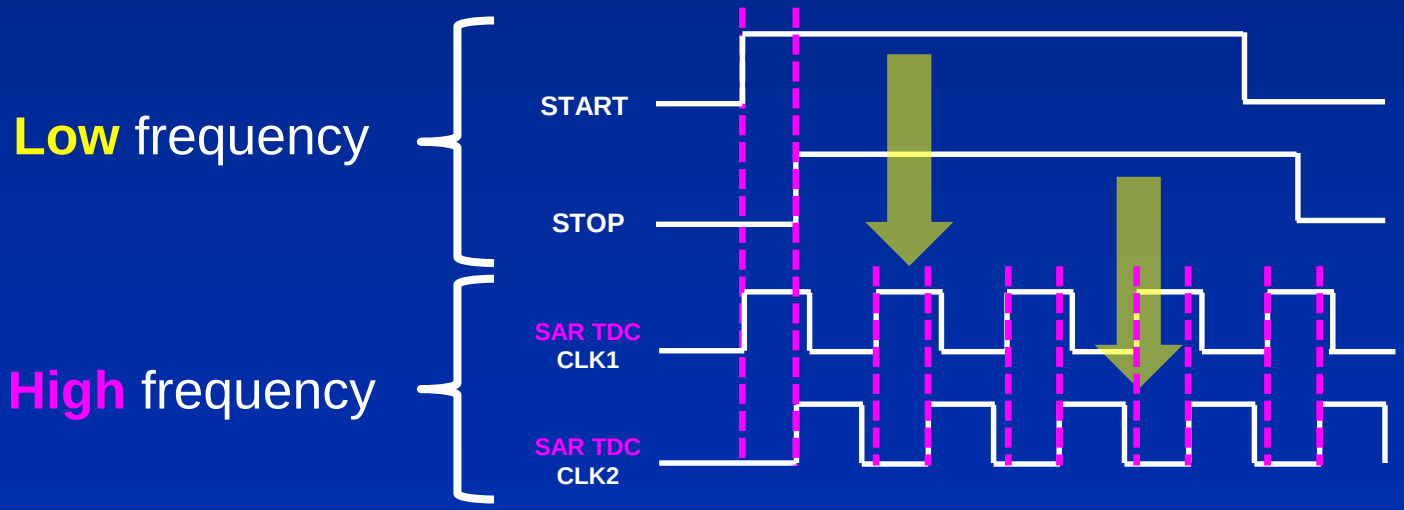


Example $\Delta T = 4.3\ \tau$



Low Frequency Clock Measurement

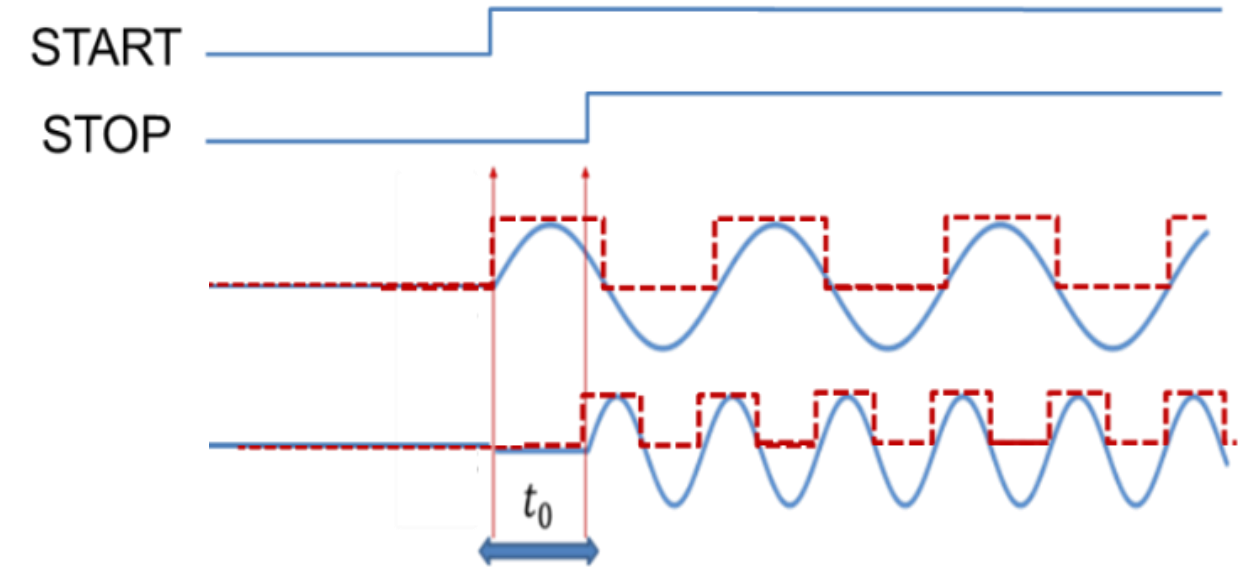




Short testing time for low frequency repetitive timing

Verner Oscillation TDC

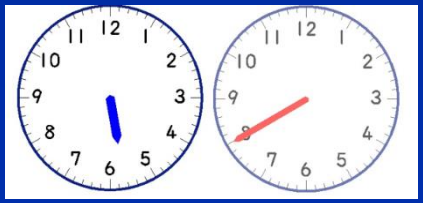
What about using different frequencies ?



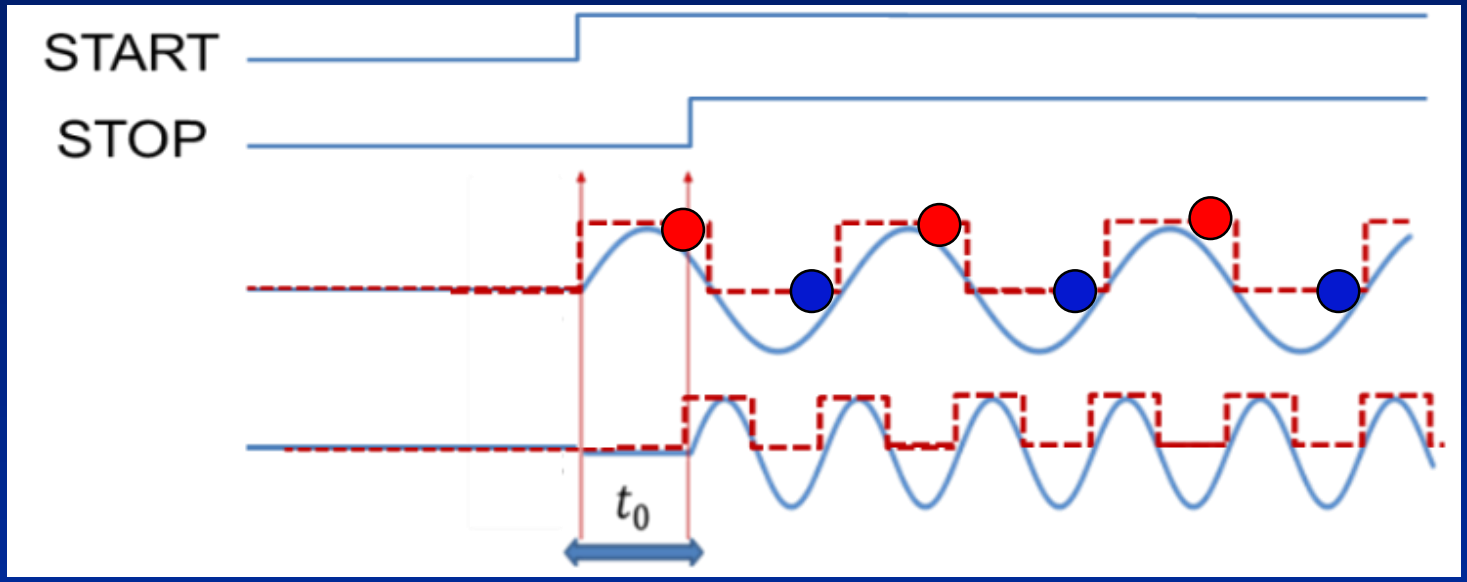
f_1: known

f_2: known

Start oscillation f_1 at START edge
f_2 at STOP edge



Verner Oscillation TDC Operation



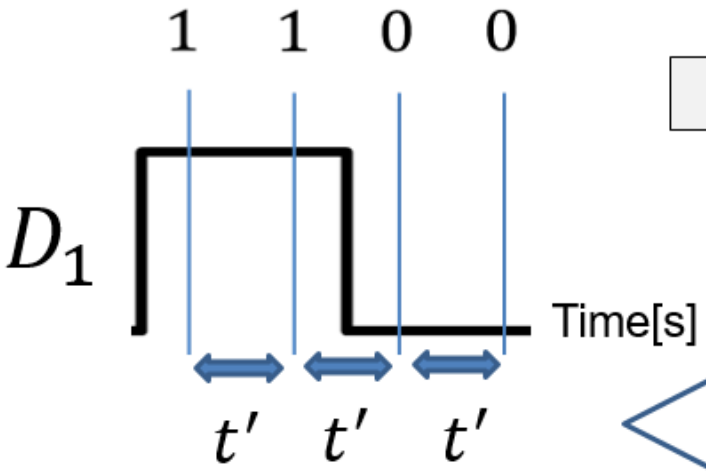
$t_0 = f$ (f_1, f_2, number of ●, ● …, number of ●, ● …)

$f1 \fallingdotseq f2$

Time resolution

$$t' = \left| \frac{1}{f_2} - \frac{1}{f_1} \right|$$

Usage of Different but Close Frequencies



time resolution = $t'[s]$

Different Frequencies

$$t' = \left|\frac{1}{f_2} - \frac{1}{f_1}\right| \qquad f_1 = 1[MHz] \quad f_2 = 0.9999[MHz]$$

$$t' \cong 1 \times 10^{-10}[s]$$

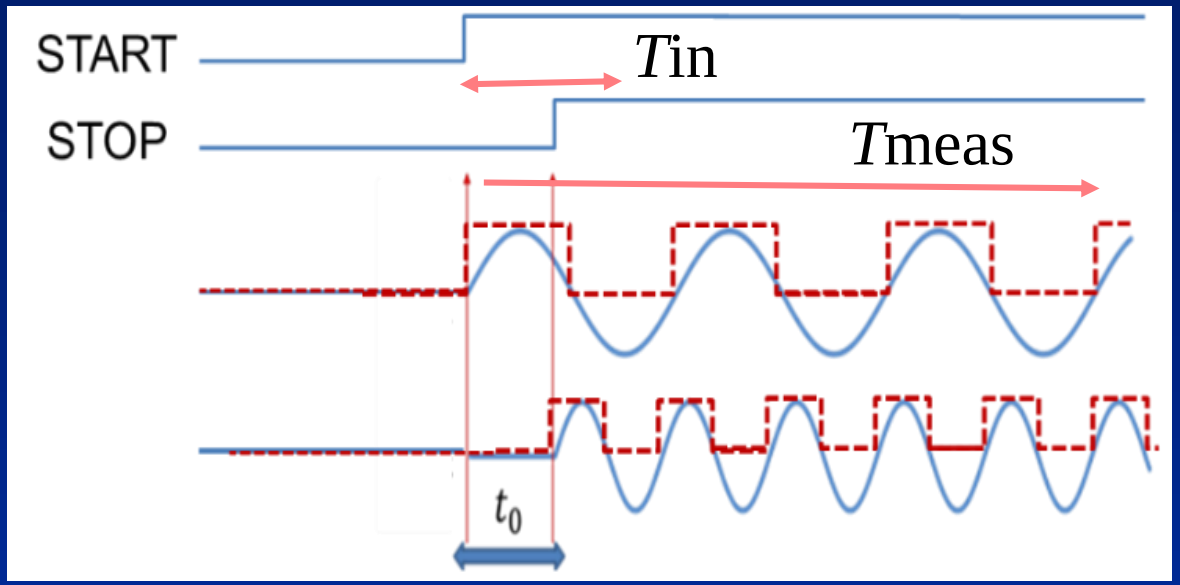
Equivalent Sampling

$f1 \fallingdotseq f2$

Different frequencies →**Fine time resolution** ⟺ **Long measurement time**

Trade off

Design Tradeoff



f_1

f_2

Fine time resolution $t' = \left| \frac{1}{f_2} - \frac{1}{f_1} \right|$

$Tin = 1/f_1, 1/f_2$ ⟷ $Tmeas = Tin \times Tin / t'$

Wide input time range

Long Measurement time

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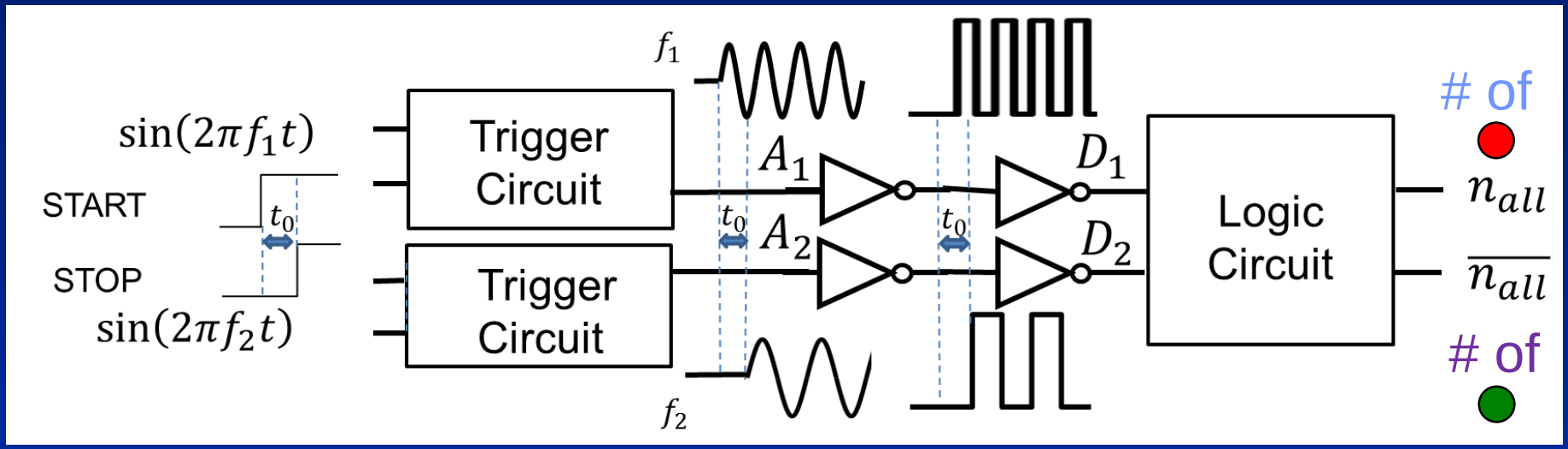
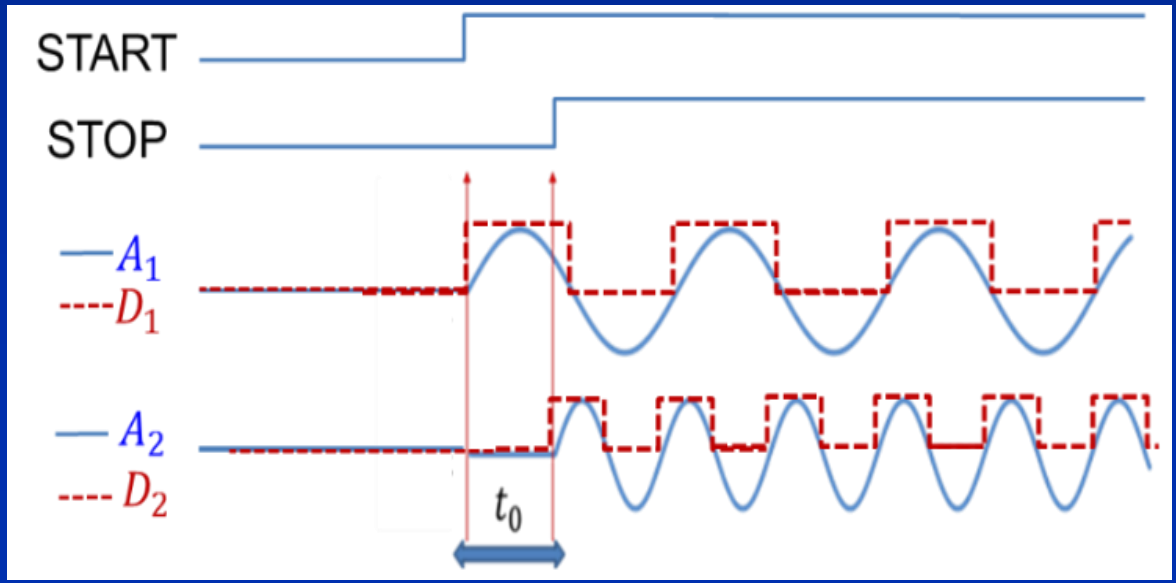
Proposed TDC Architecture

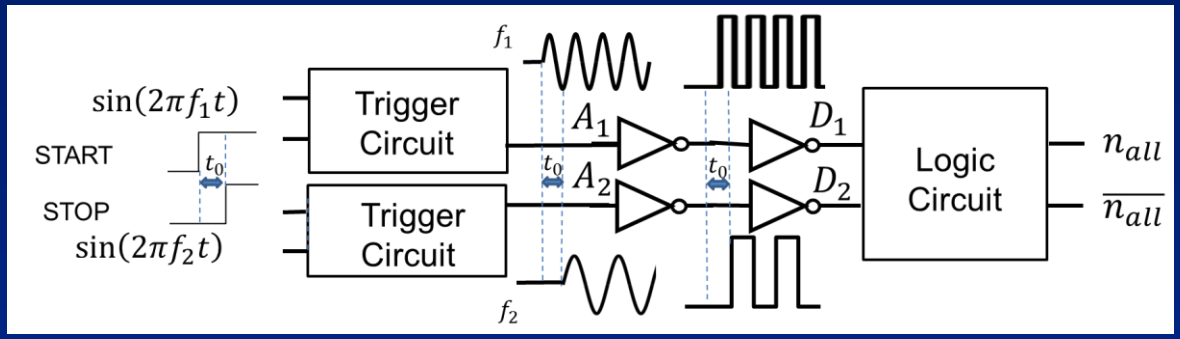


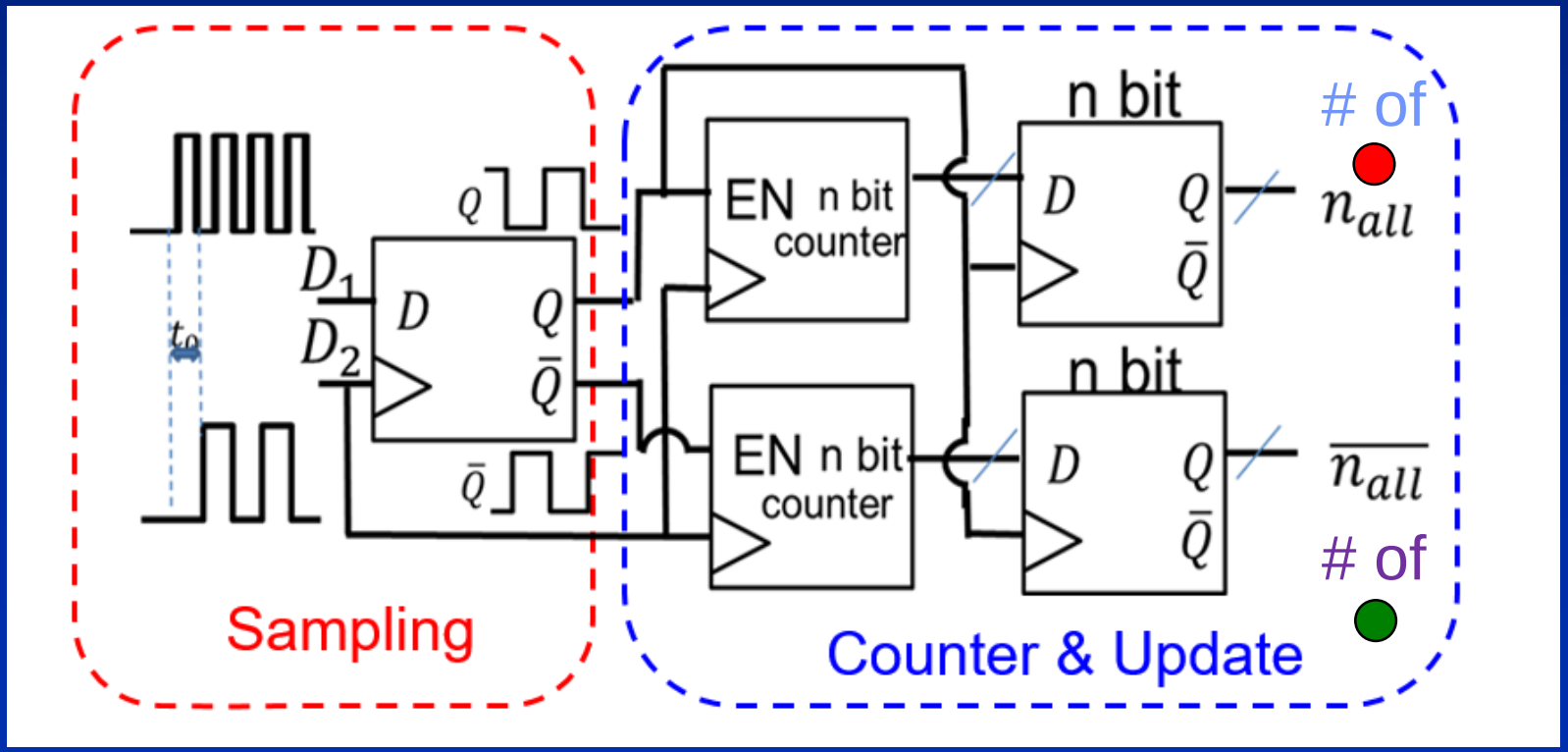
f_1: known

f_2: known

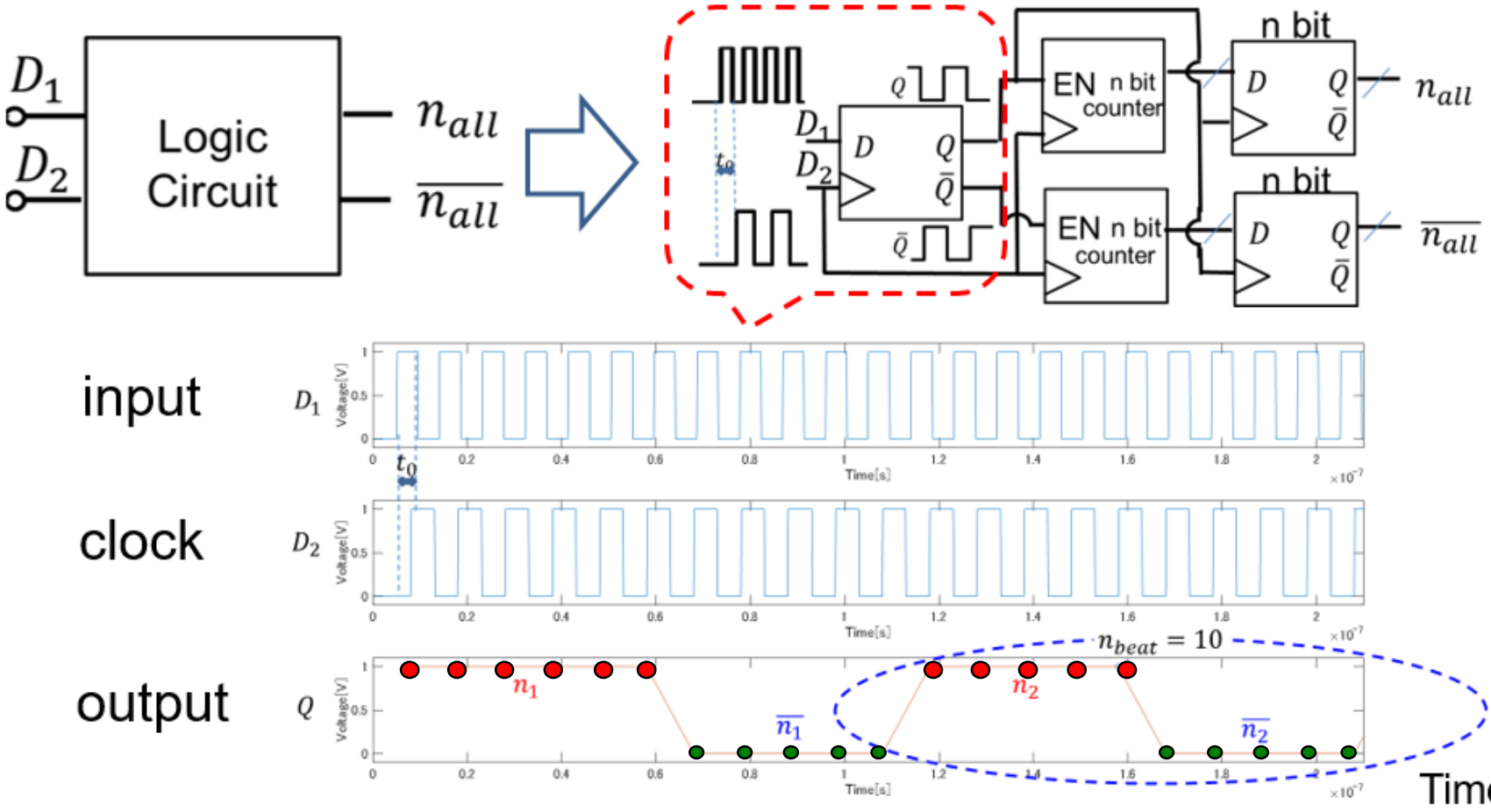


Logic Circuit for Time Measurement





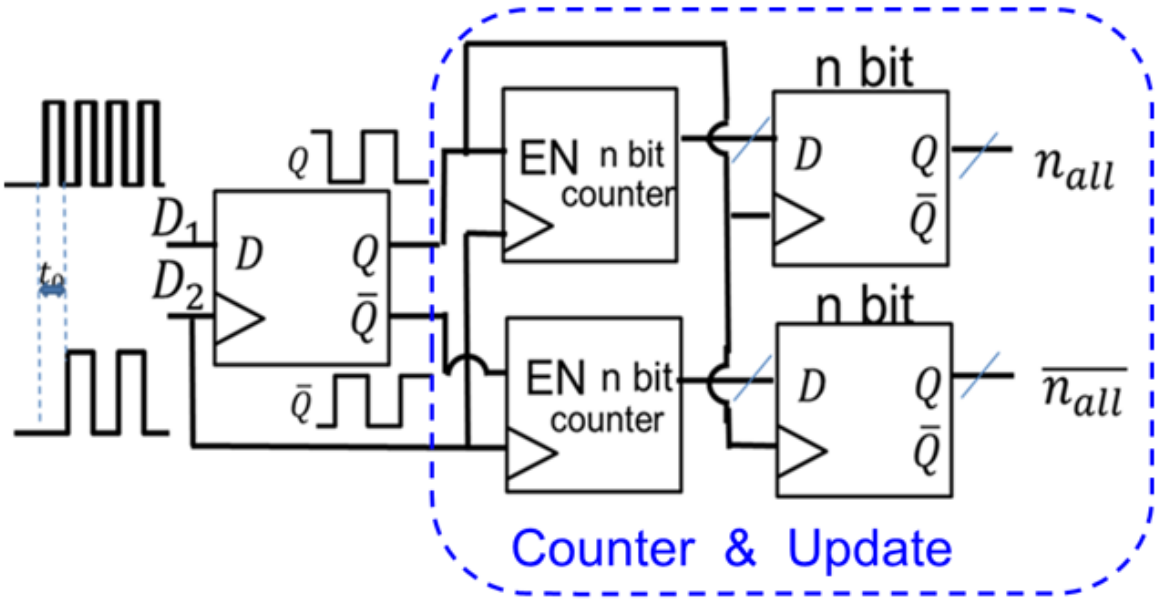
D1 Sampling by D2

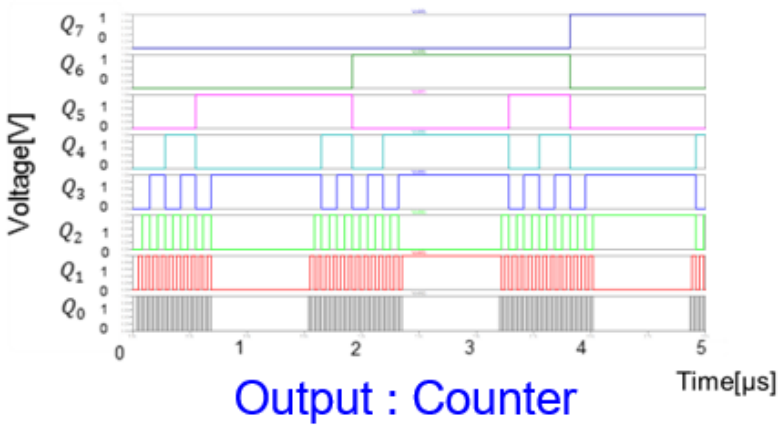


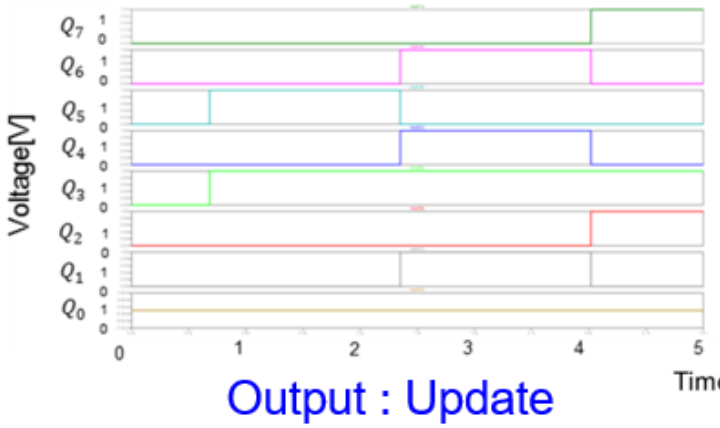
$$n_{all}(= n_1 + n_2 \dots) \qquad \overline{n_{all}}(= \overline{n_1} + \overline{n_2} \dots)$$

$$n_{beat} = n_2 + \overline{n_2} = n_3 + \overline{n_3} = \cdots = \frac{f_2}{|f_2 - f_1|}$$

Counter & Update



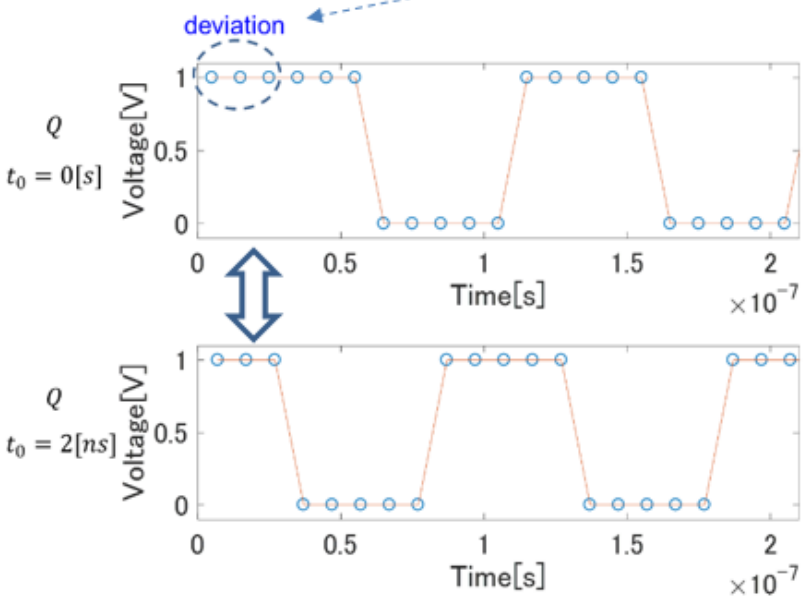




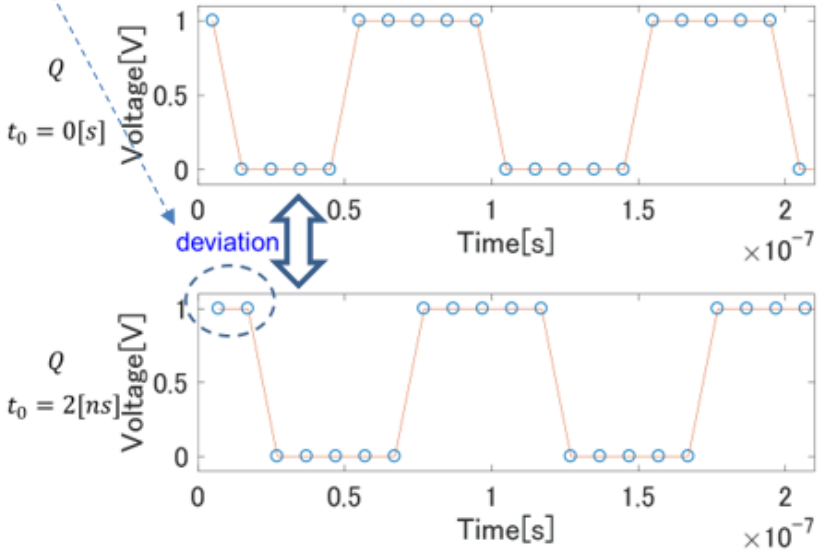
Digital value

Deviation Points by Time Difference

- Timing difference t_0 generates **deviation**



$(a) f_1 > f_2$



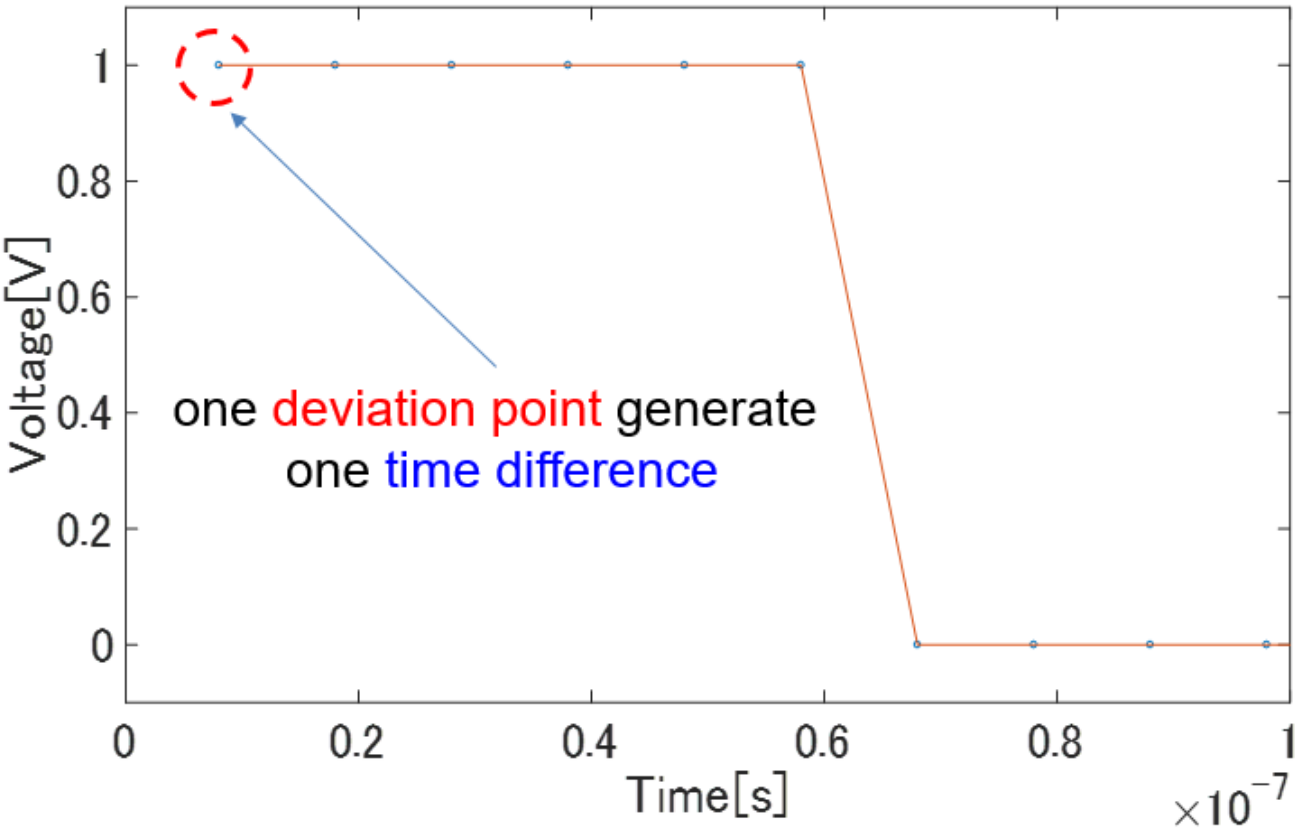
$(b) f_1 < f_2$

$$\textbf{deviation} = \begin{cases} (\overline{n_{all}} - n_{all}) & (\textbf{in case } f_1 > f_2) \\ \{n_{beat}/2 - (\overline{n_{all}} - n_{all})\} & (\textbf{in case } f_1 < f_2) \end{cases}$$

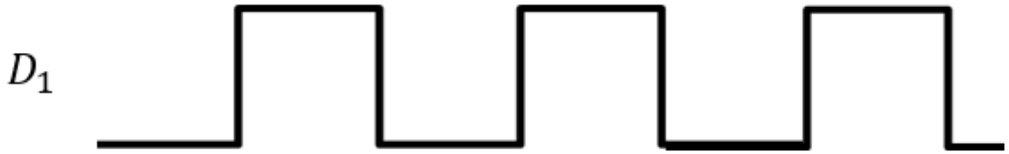
Deviation and Time Resolution

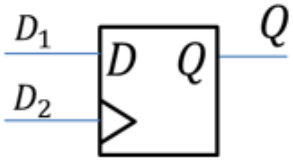
$$t_0 = \begin{cases} (\overline{n_{all}} - n_{all})t' & (\text{in case } f_1 > f_2) \\ \{n_{beat}/2 - (\overline{n_{all}} - n_{all})\}t' & (\text{in case } f_1 < f_2) \end{cases}$$

Q



Equivalent Time Sampling



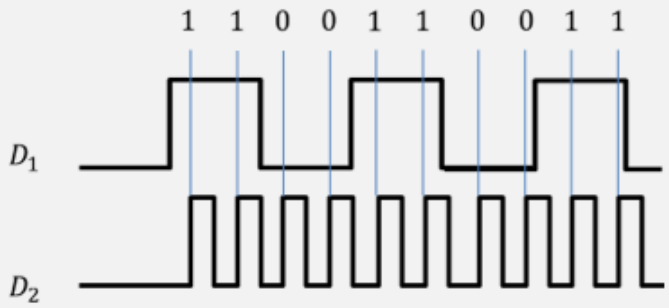


Sampling D_1 by clock D_2

$$t' = \left|\frac{1}{f_2} - \frac{1}{f_1}\right|$$

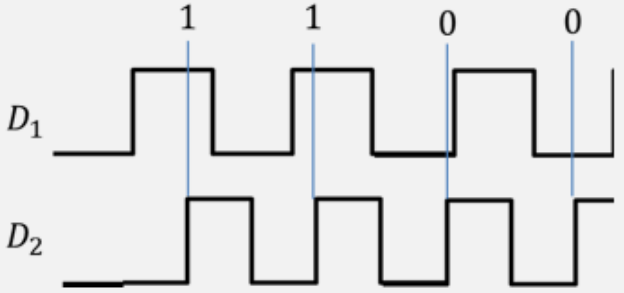
t'=1/f2

$(in\ case\ f_1 \ll f_2)$



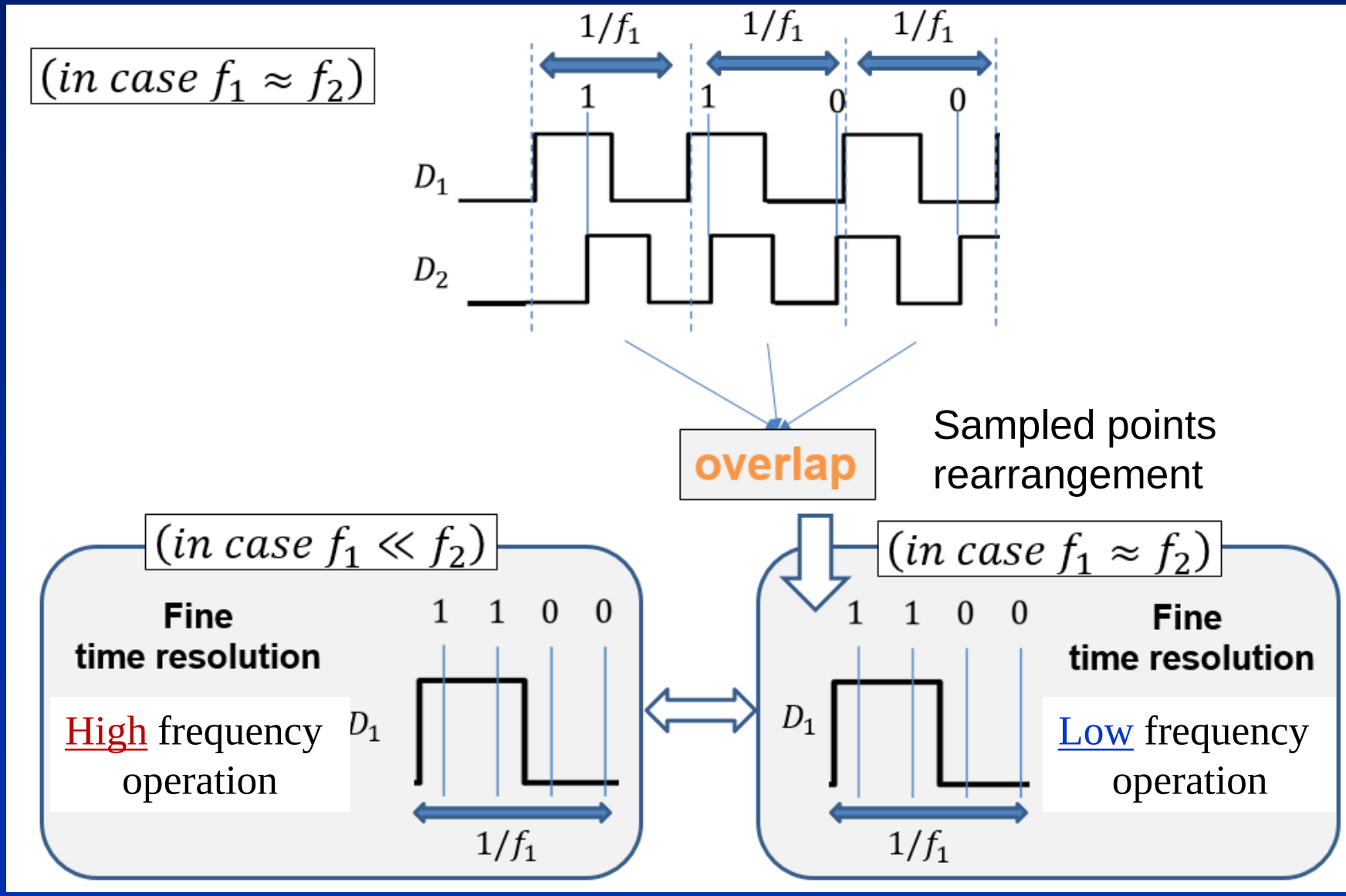
Fine time resolution

$(in\ case\ f_1 \approx f_2)$



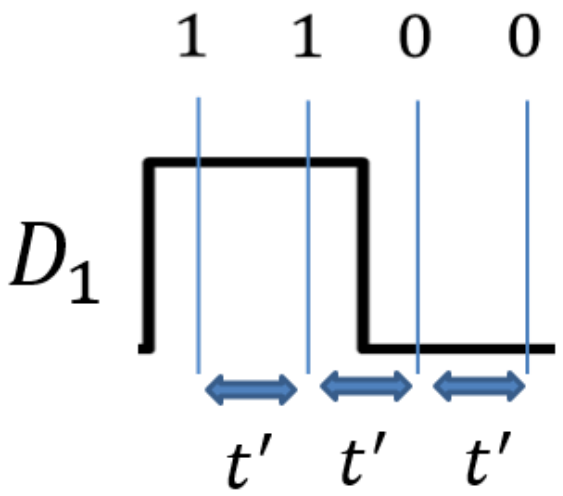
Coarse time resolution ?

Waveform Reconstruction



Measurement Time Resolution

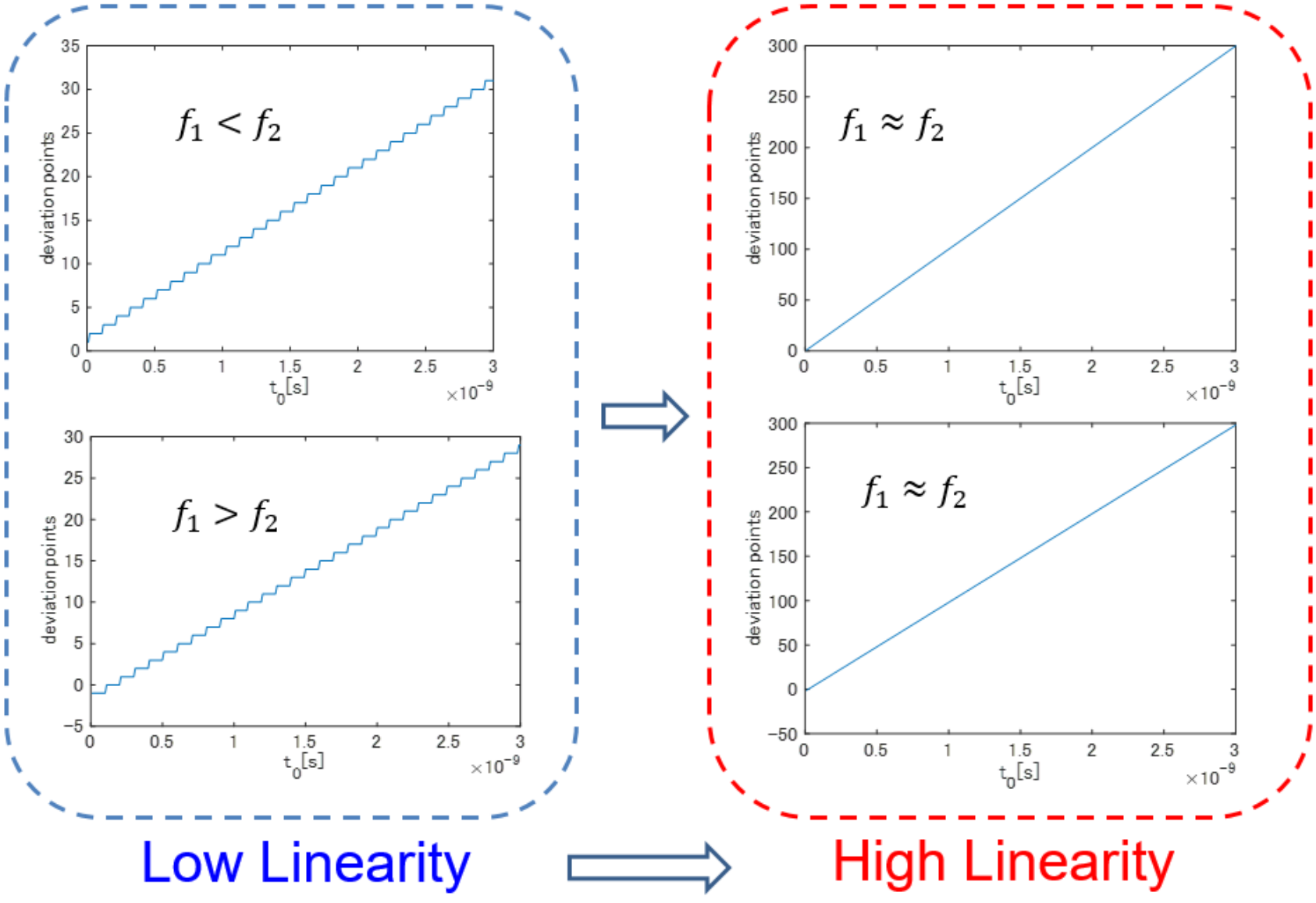
After overlap $(in\ case\ f_1 \approx f_2)$



Time resolution = t'

$$t' = \left|\frac{1}{f_2} - \frac{1}{f_1}\right| = \left|\frac{f_1 - f_2}{f_1 f_2}\right| \Rightarrow \lim_{f_1 \to f_2} t' = \text{Fine time resolution}$$

Proposed TDC Linearity

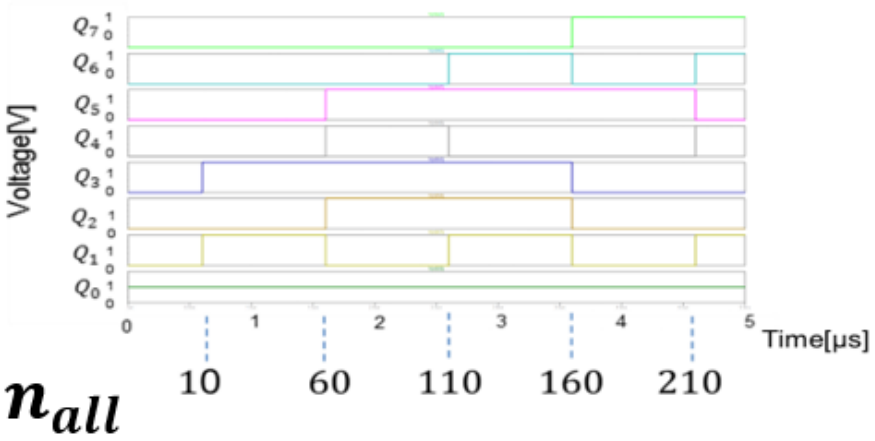


Simulation Verification of Proposed TDC

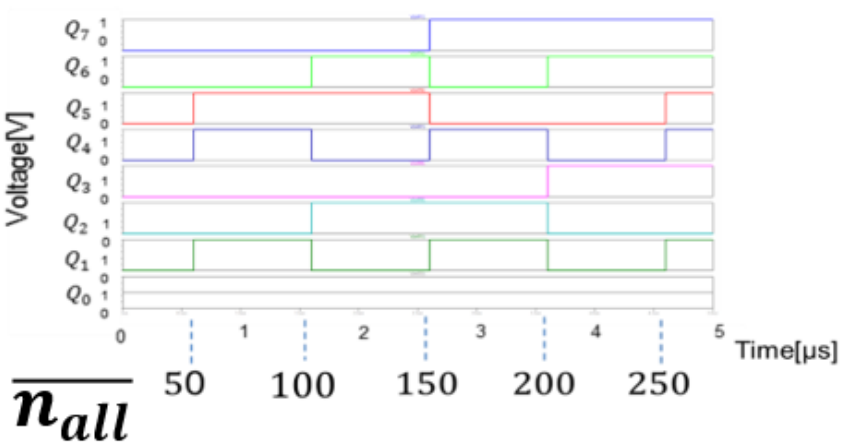
◆ Simulation Conditions

$$f_1 = 99[MHz], f_2 = 100[MHz], t_0 = 1[ns]$$

◆ SPICE Simulation Results



n_{all}



$\overline{n_{all}}$

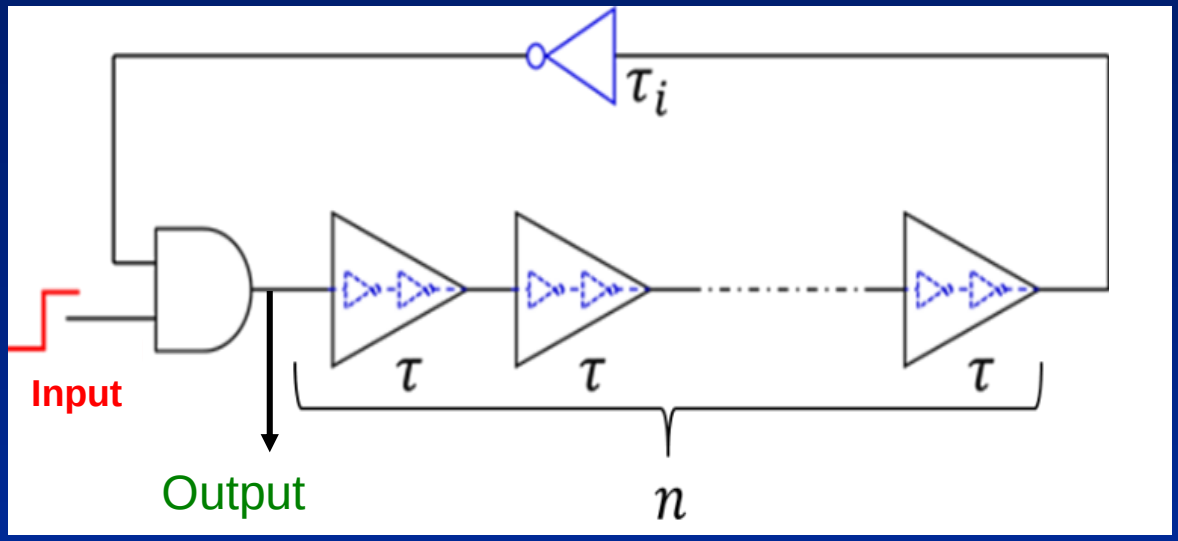
At 5[μs] $n_{all} = 210$, $\overline{n_{all}} = 250$

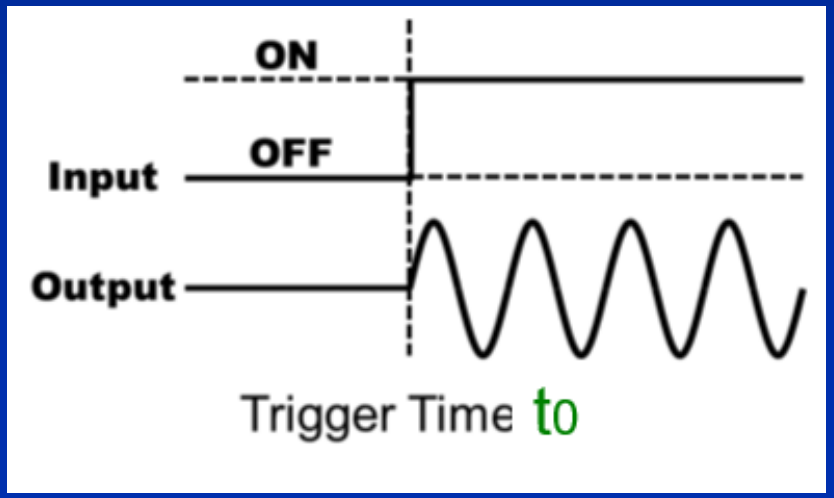
$t_0 = 1.01$[ns] Error is **1**[%]

Outline

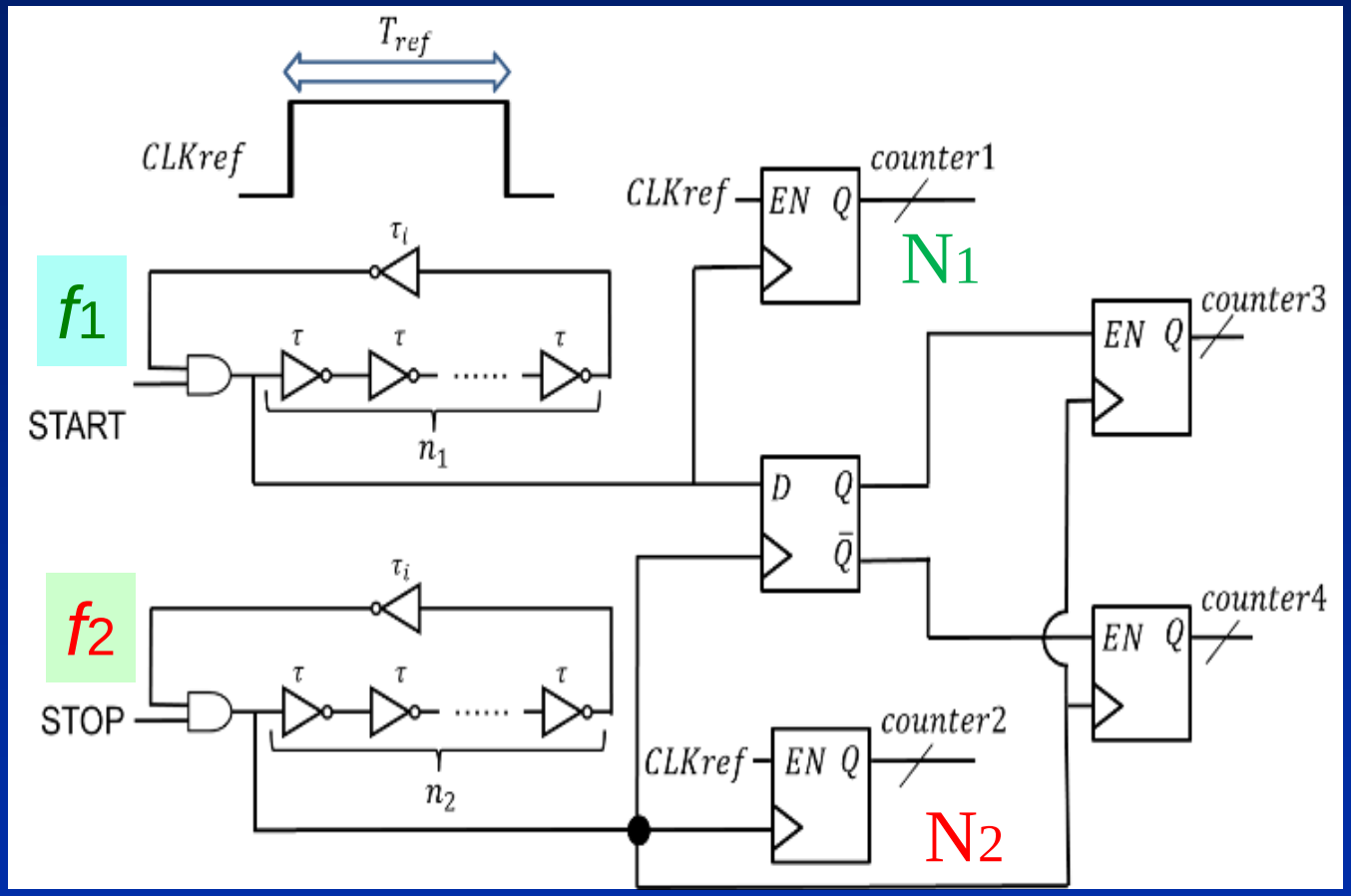
- Research Background
- Measurement Principle
- Analog Centric TDC
- Digital Centric TDC
- Discussion & Conclusion

Ring Oscillator with Start





Digital Centric TDC



Ring oscillator frequencies

f_1 ≒ Counter 1 output N1 / reference time Tref

f_2 ≒ Counter 2 output N2 / reference time Tref

Outline

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TDC Architecture Comparison

	Clocks Under Test	Measurement Time	Time Resolution	Circuit	FPGA	
Flash-type	Single event ○	Short ○	Coarse ✕	Large ✕	Digital ○	
Gray code based	Single event ○	Short ○	Coarse ✕	Small ○	Digital ○	
SAR-type	Repetitive clock △	Middle △	Middle △	Small ○	Digital ○	
Delta-Sigma type	Repetitive clock △	Long ✕	Fine ○	Small ○	Small Analog △	
Integral type	Single event ○	Long ✕	Fine ○	Small ○	Small Analog △	Oscillators
Verner Oscillator	Single event ○	Long ✕	Fine ○	Small ○	Small Analog △	Oscillators

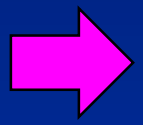
○ Excellent △ Good ✕ Bad

Comparison of Time and Voltage

- Dynamic range of time domain signal can be infinite.
- Time flows in one direction.
- Ring oscillator can be often used for time domain signal processing.
- Exact frequency division is possible, whereas exact voltage division is difficult.
- Frequency is a stable signal.
- Jitter is a difficult problem.
- Time as well as voltage can be held.
- Time as well as voltage can be amplified.
- New TDC architectures can be inspired by existing ADC architectures.

Conclusion

- Verner Oscillator TDC architectures
  - Analog centric and digital centric ones
  - Using two oscillators with different frequencies



Can be shared among multi-channel TDCs
  - No delay line
  - No self-calibration required
  - Design tradeoff
    - Measurement time
    - Time resolution
    - Input time range

Time is very important !

光阴似箭

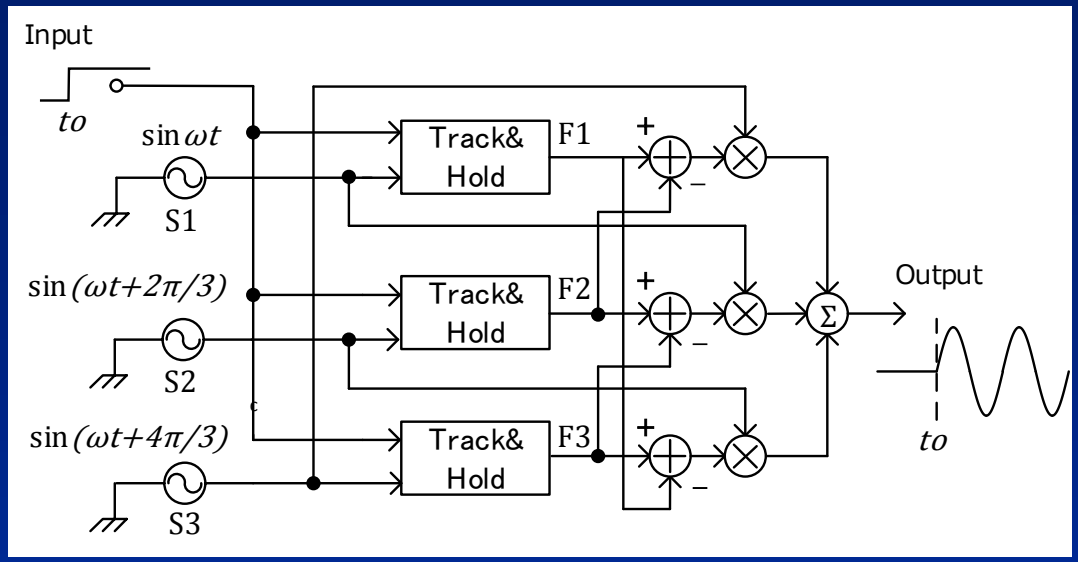
Effective executives know that time is the limiting factor of the other resources.

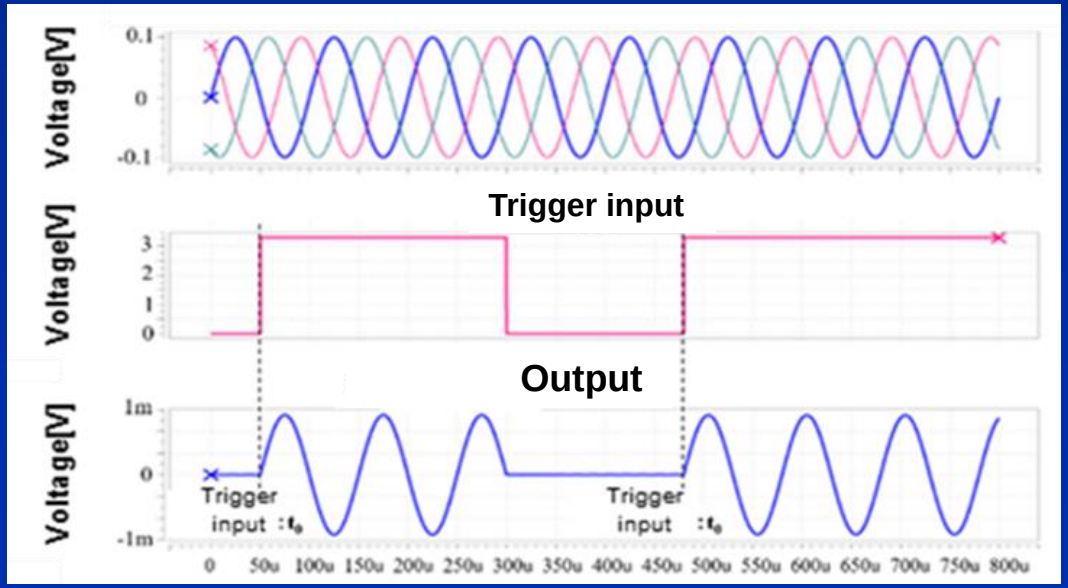
Peter Drucker

Appendix :
N-Stage Trigger Circuit

S. Sakurai, H. Kobayashi, et. al.,
“Study OF Multi-Stage Oscilloscope Trigger Circuit,”
IEEE ISPACS, Xiamen, (Nov. 2017)

Three-stage Trigger Circuit





Analysis of Three-stage Trigger Circuit

Signal source

$$S_1 = \sin \omega t\ ,\ S_2 = \sin\left(\omega t + \frac{2\pi}{3}\right),\ S_3 = \sin\left(\omega t + \frac{4\pi}{3}\right)$$

Triggered T/H circuit output

$$F_1 = \sin \omega t_0\ ,\ F_2 = \sin\left(\omega t_0 + \frac{2\pi}{3}\right),\ F_3 = \sin\left(\omega t_0 + \frac{4\pi}{3}\right)$$

・Track mode

$$Vo_{track} = S_1(S_2 - S_3) + S_2(S_3 - S_1) + S_3(S_1 - S_2)$$

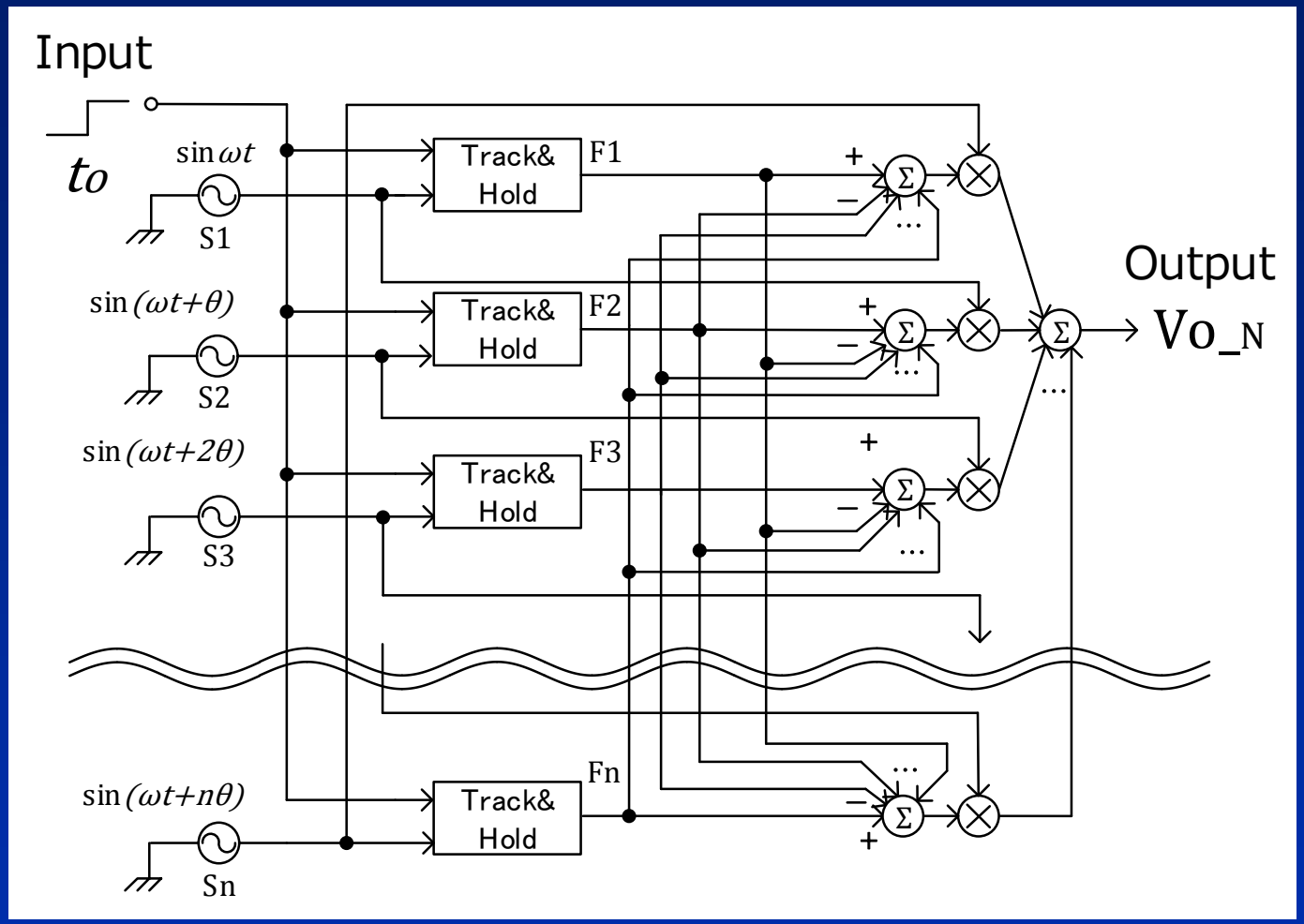
$$= 0 \qquad \textbf{(Constant)}$$

・Hold mode

$$Vo_{hold} = S_1(F_2 - F_3) + S_2(F_3 - F_1) + S_3(F_1 - F_2)$$

$$= \frac{3\sqrt{3}}{2}\sin(\omega(t - t_0))$$

N-Stage Trigger Circuit



Trigger circuit is a key !

Trigger circuit for TDC ⟺ T/H circuit for ADC.