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S38-1　Data Converters II
15:45-16:15 PM
Nov. 2, 2018 (Fri)

Performance Improvement of Delta-Sigma ADC/DAC/TDC Using Digital Technique

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GUNMA UNIVERSITY

Contents

- Objective of This Paper
- What is DWA ?
- LP, HP DWA
- Multi-Bandpass DWA
- Multi-Bandpass Complex DWA
- Second-Order DWA
- Application to Multi-bit ΔΣ TDC
- Conclusion

Contents

Objective of This Paper

- Review the research results of authors' group

  in the area of DWA: Data Weighted Averaging .

  ADC/ DAC performance improvement
  with simple digital techniques

- Consider their application to TDC

- Consider to unify the DWA algorithms and establish their design methodology.

Contents

Calibration Techniques Classification

ADC/DAC/TDC digital calibration techniques
prevail in nano-CMOS era.

- Error Correction
  - No measurement of errors
  - Redundancy usage

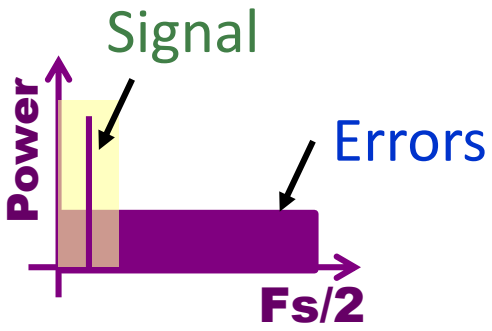
- Self-Calibration
  - Error measurement
  - Compensation
  - Reference
    - Voltage
    - Current
    - Time (frequency)
    - Linearity

DWA Techniques

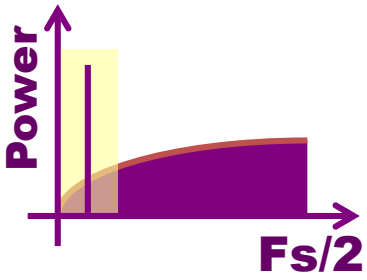
- Error Correction
  - No measurement of errors
  - Redundancy usage
    Time averaging of errors
    Spectrum shaping of errors

DWA: Data Weighted Averaging

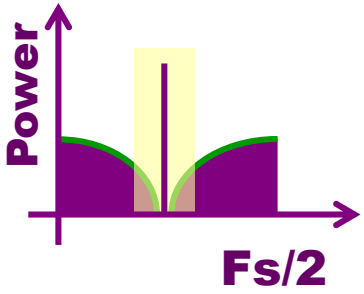
DEM: Dynamic Element Matching



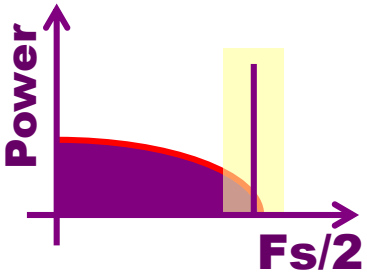
W/O DWA



LP DWA



BP DWA

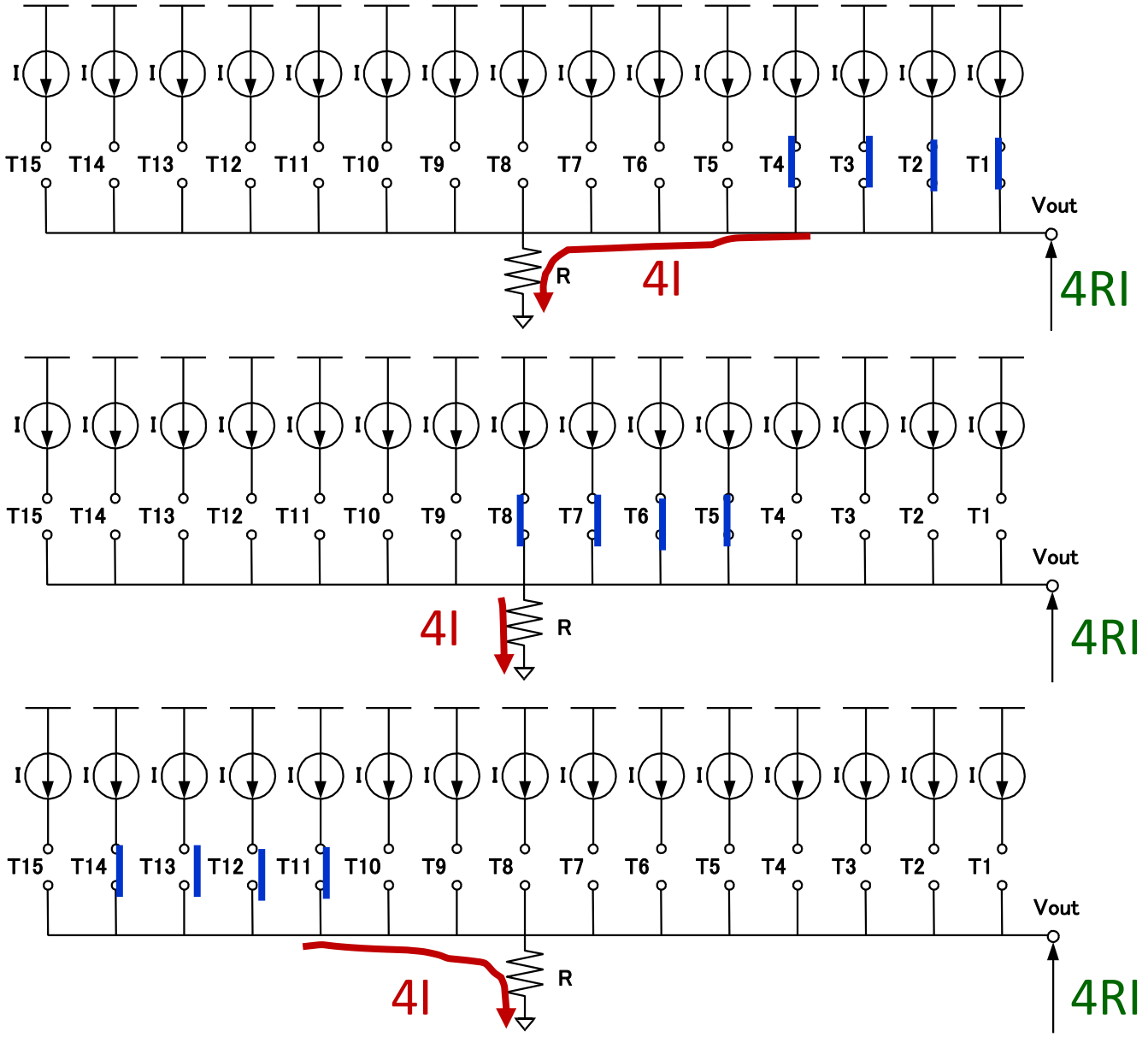


HP DWA

Segment DAC with Redundancy

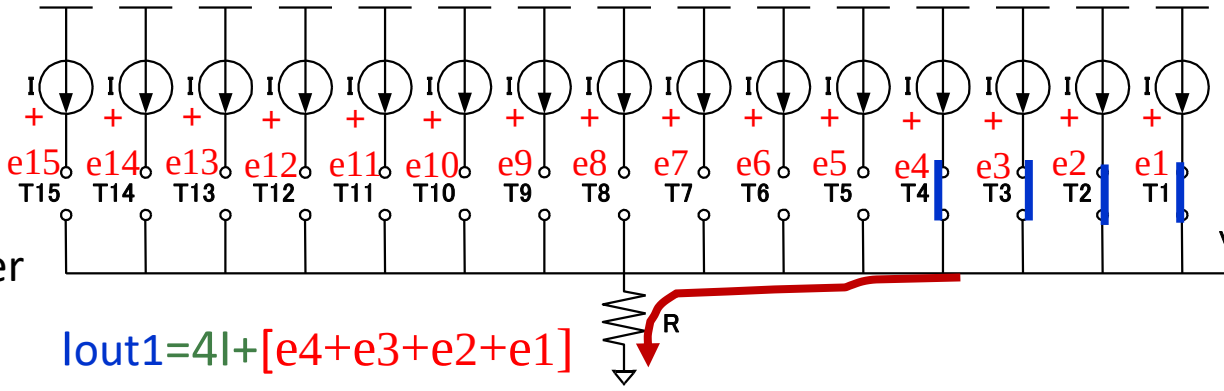
Digital input = 4

Multiple realization configurations



Unit Cell Mismatches

Current mismatches e15, e14,…,e1 spectrum shaping by cell selection order

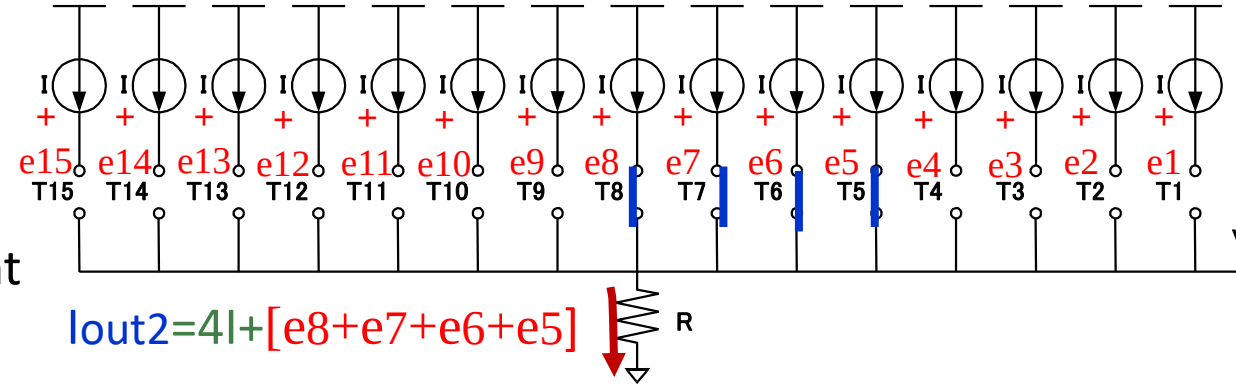


Iout1=4I+[e4+e3+e2+e1]

4RIout1

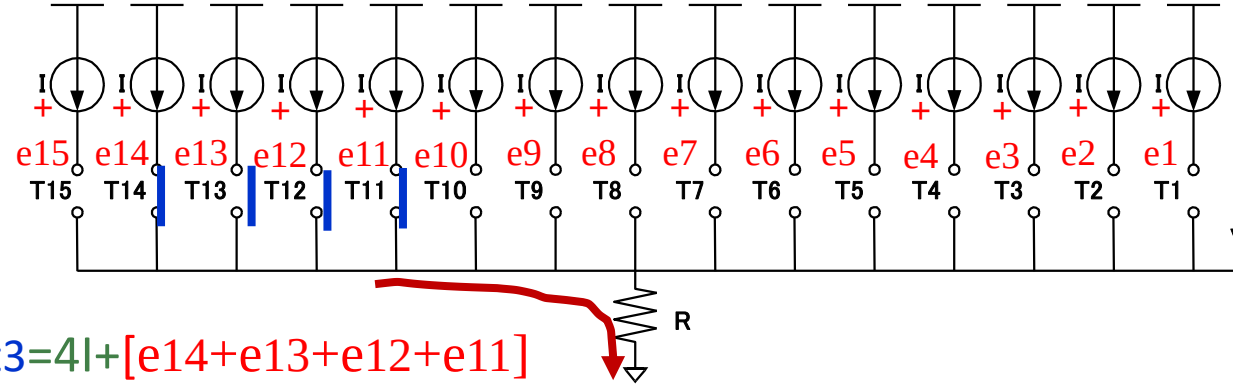
DWA algorithm

No measurement of e15, e14,…,e1



Iout2=4I+[e8+e7+e6+e5]

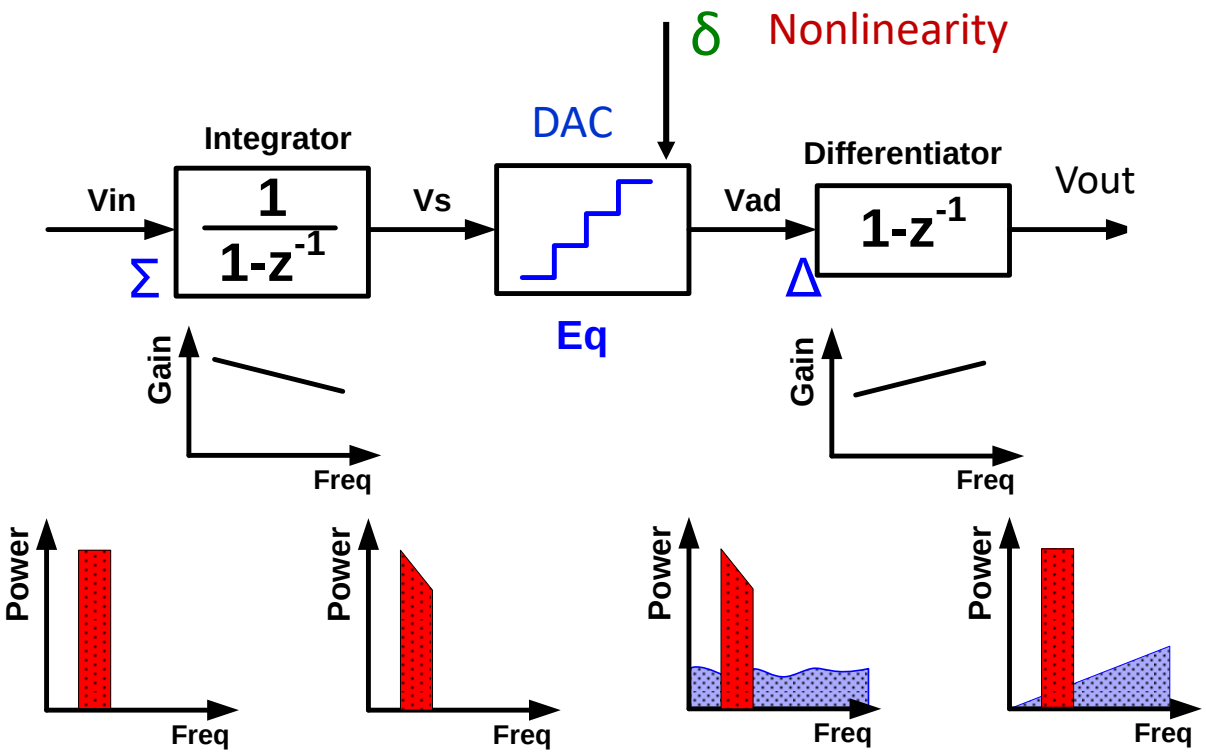
4RIout2



Iout3=4I+[e14+e13+e12+e11]

4RIout3

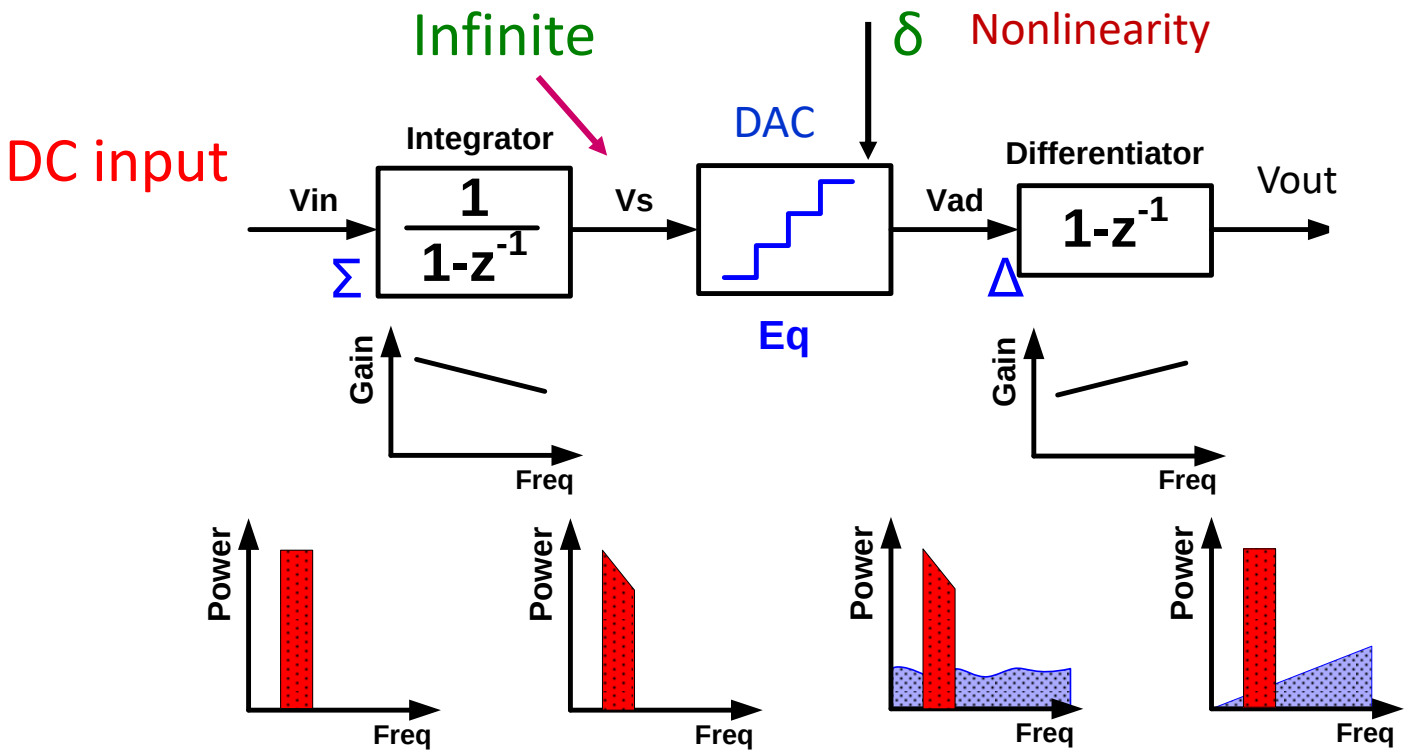
ΔΣ Modulation and DWA



$$Vout(z) = Vin(z) + (1 - z^{-1}) \cdot \delta(z)$$

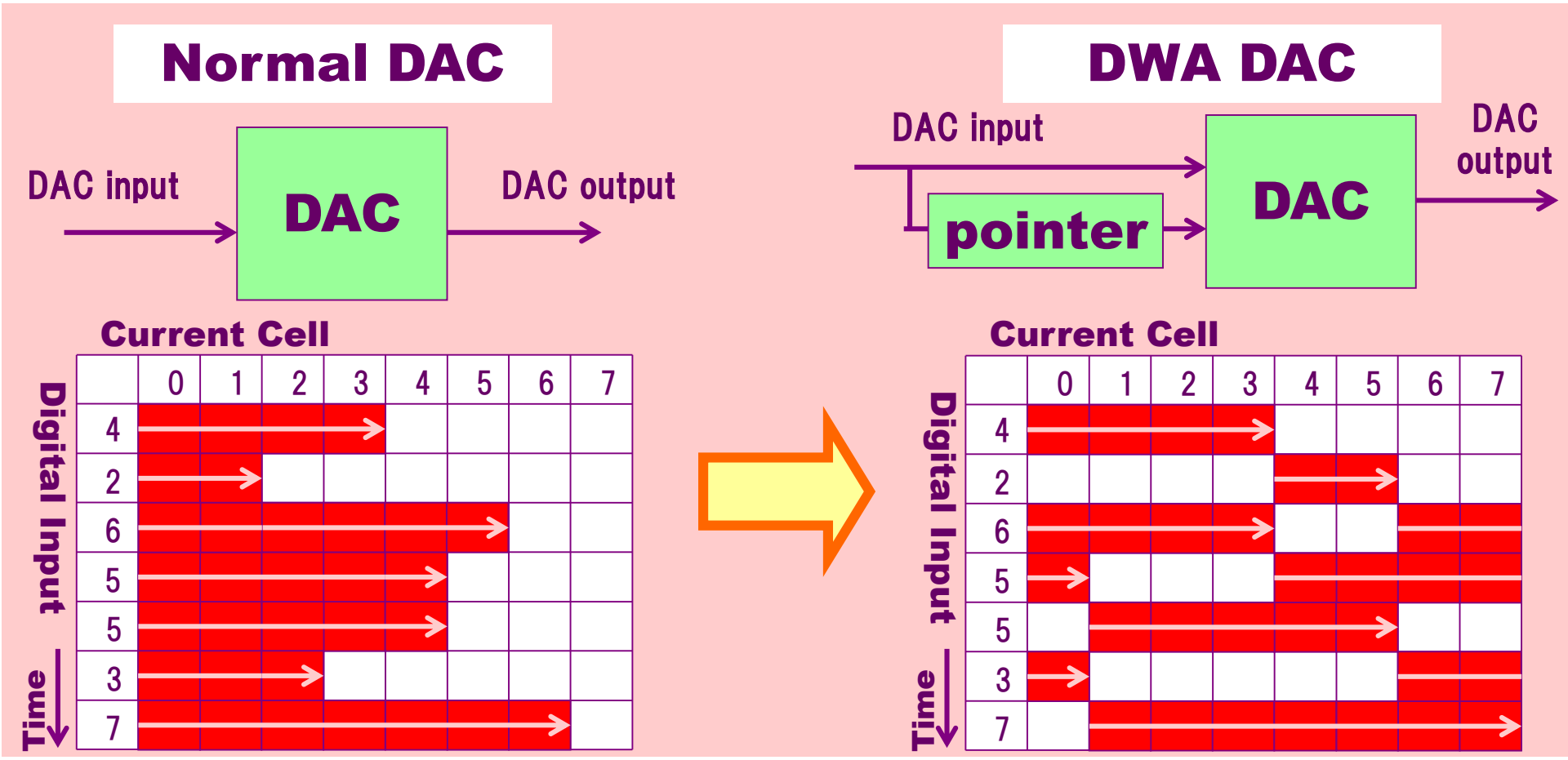
DAC nonlinearity δ(z) is first-order noise-shaped.

ΔΣ Modulation and DWA



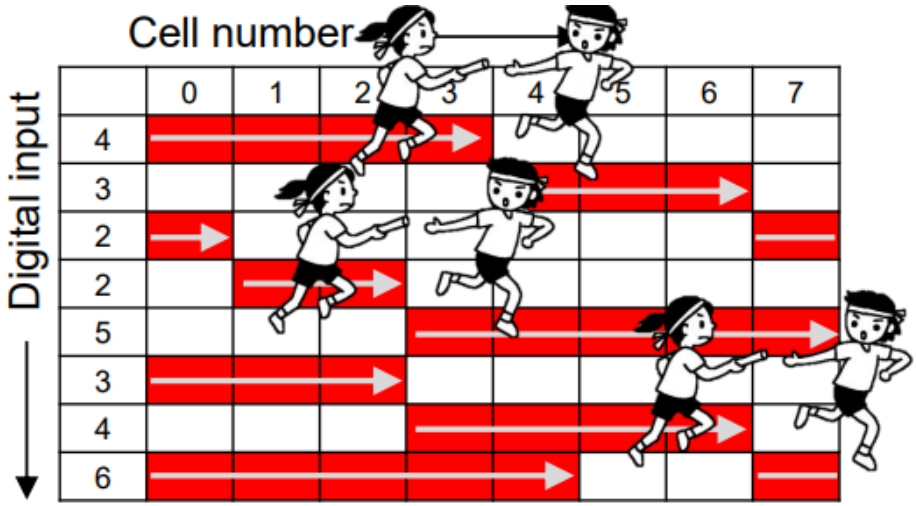
This configuration can NOT be implemented !

Equivalent Operation Using DWA to ΔΣ Modulation



"Infinite" is equivalently realized with wrap-around

DWA Operation is a fun !



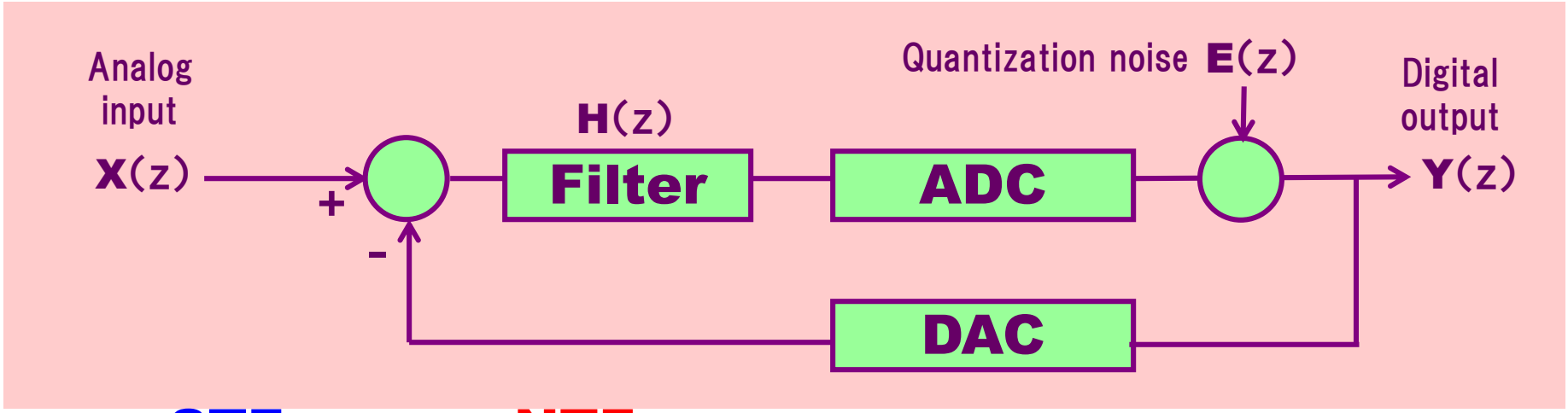
Passing a baton in relay race !

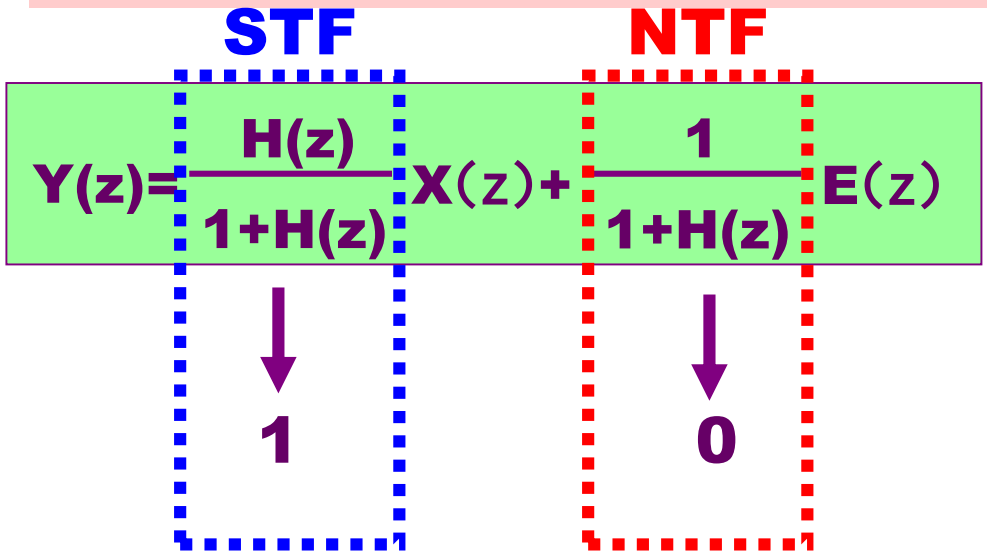
Contents

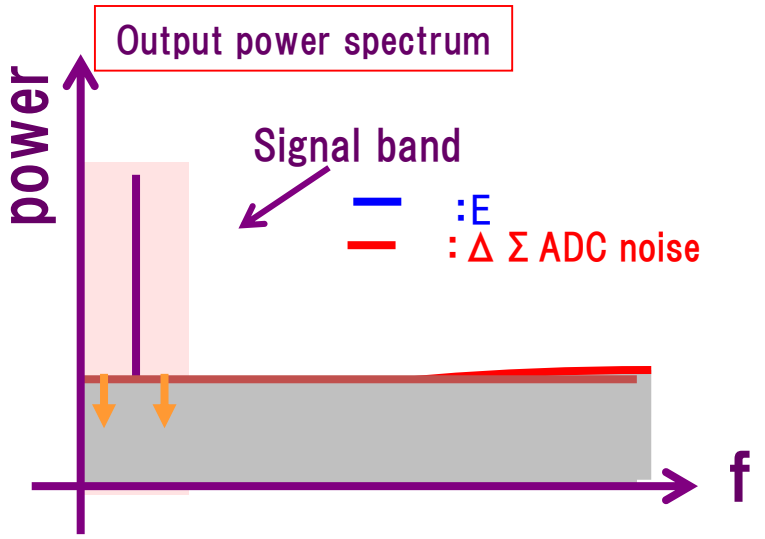
LP: Low Pass

HP: High Pass

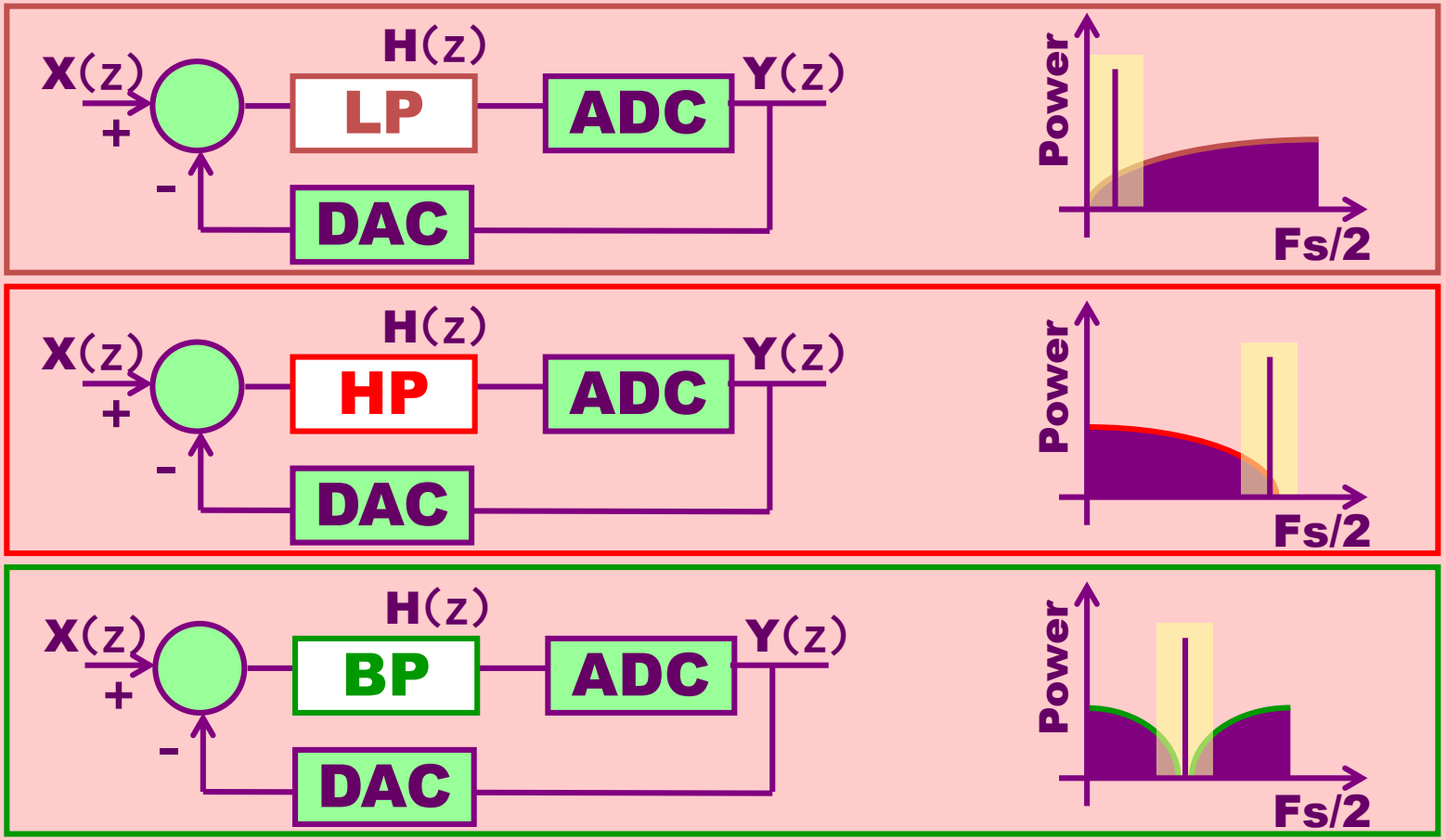
LP ΔΣAD Modulator



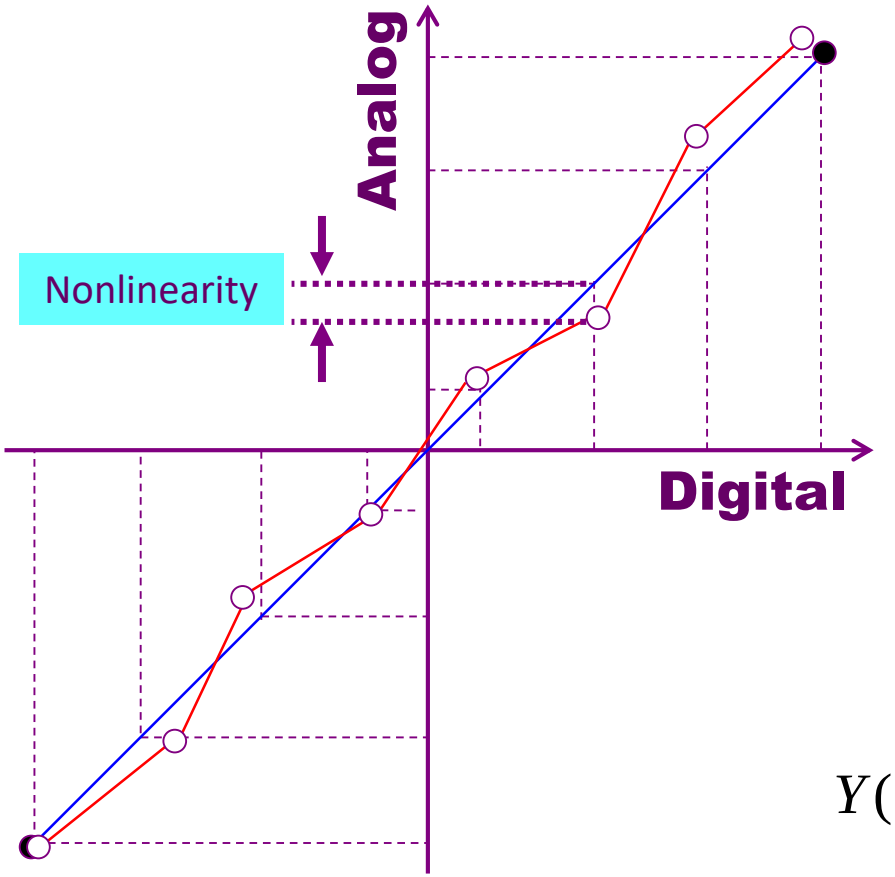




Varieties of ΔΣAD Modulators

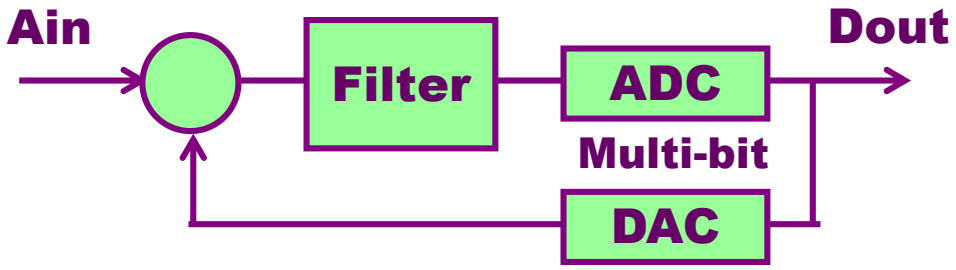


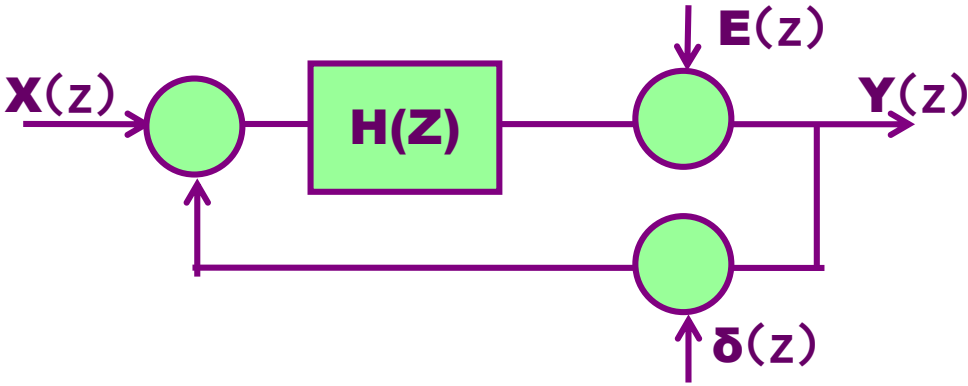
Multi-bit DAC Nonlinearity



● :Single-bit Output

○ :Multi-bit Output



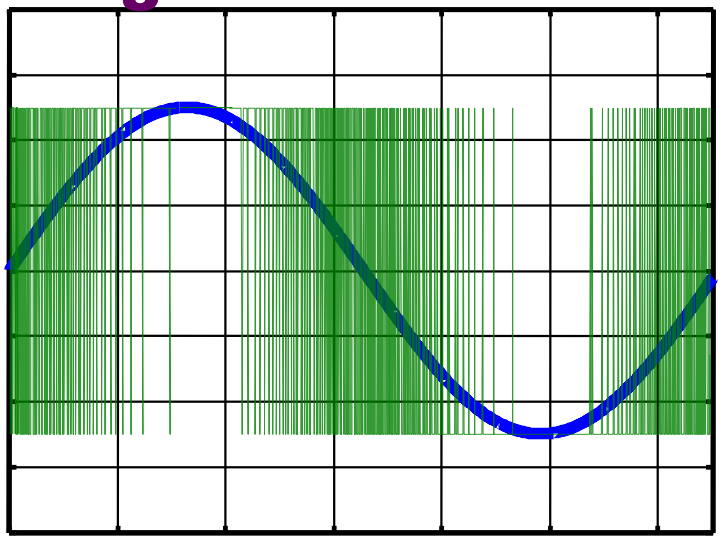


$$Y(z) = \frac{H(z)}{1+H(z)}\{X(z) - \delta(z)\} + \frac{1}{1+H(z)}E(z)$$

δ(z) is NOT noise-shaped

Why Multi-bit ADC/DAC inside ΔΣ AD Modulator ?

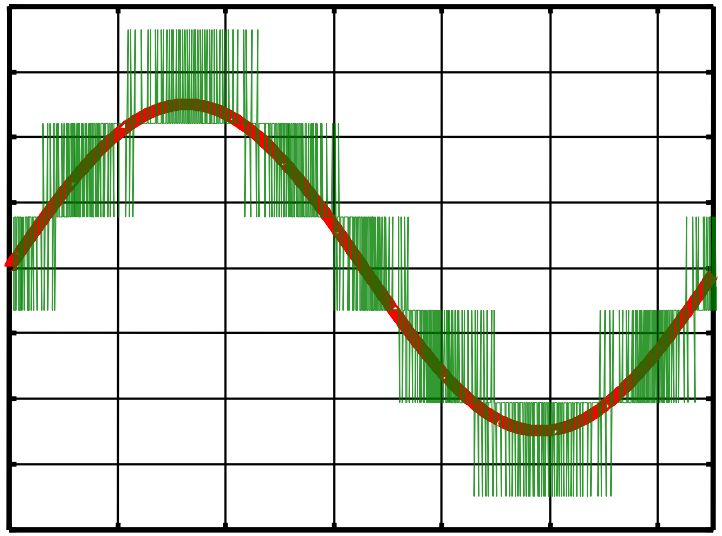
Single-Bit



- High slew-rate of opamp

⇨ Large power

Multi-Bit



- Low slew-rate of opamp

⇨ Small power

- Problem:

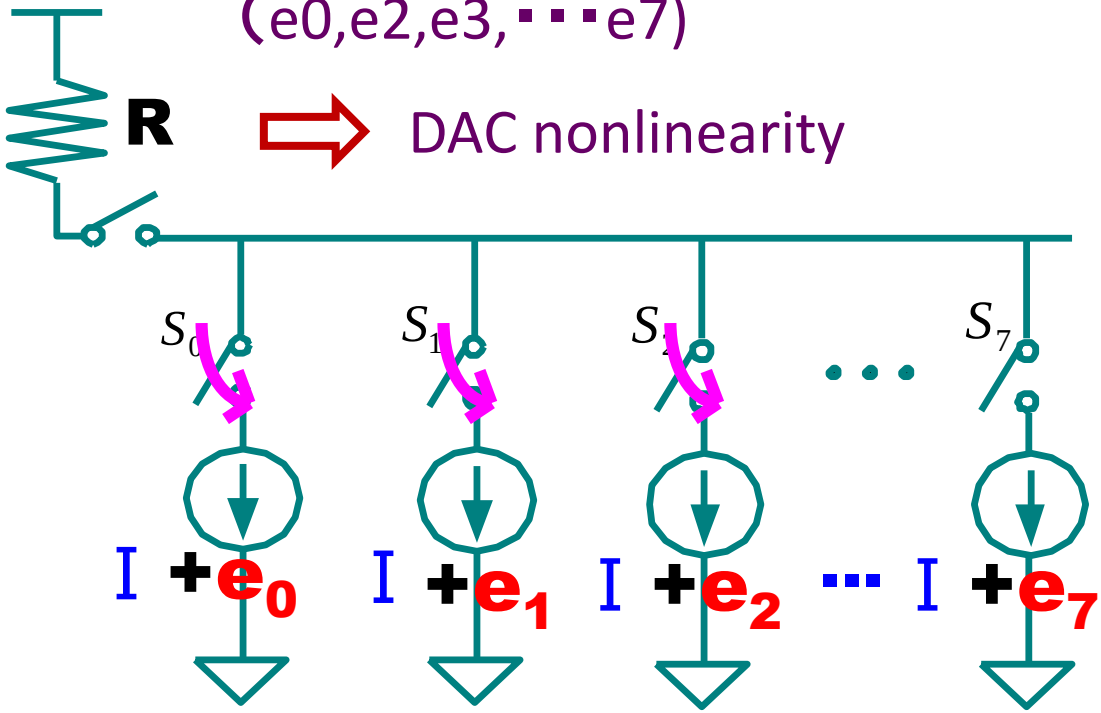
Multi-bit DAC nonlinearity

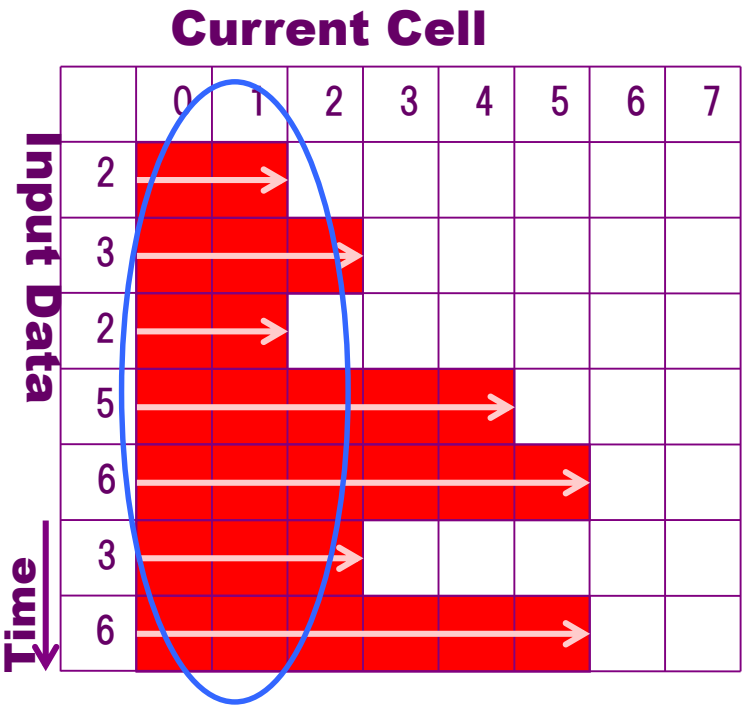
Unit Cell Mismatches

Segment DAC

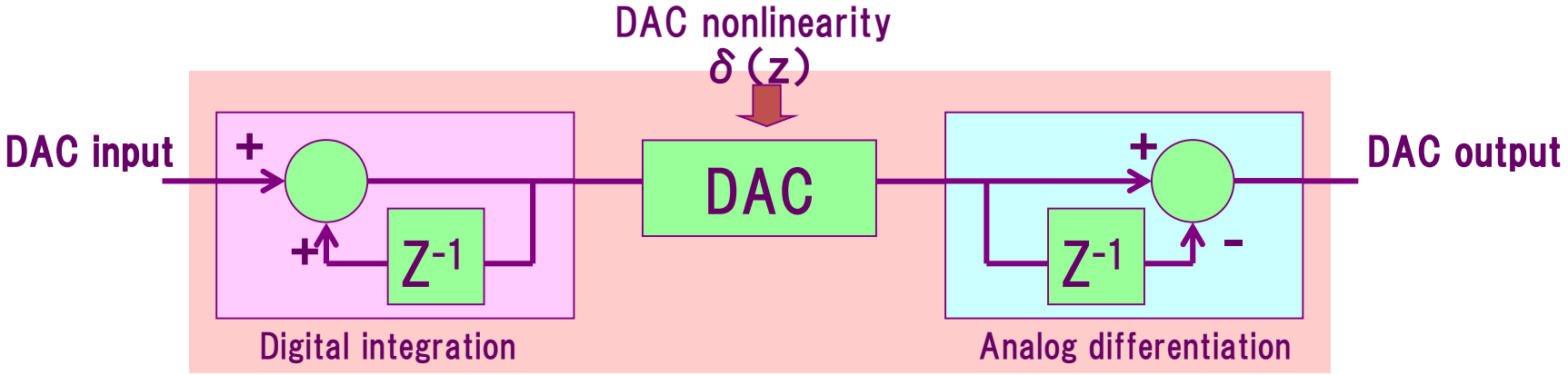
Current Cell Mismatch
(e0,e2,e3,···e7)

Errors of specific current cells are accumulated

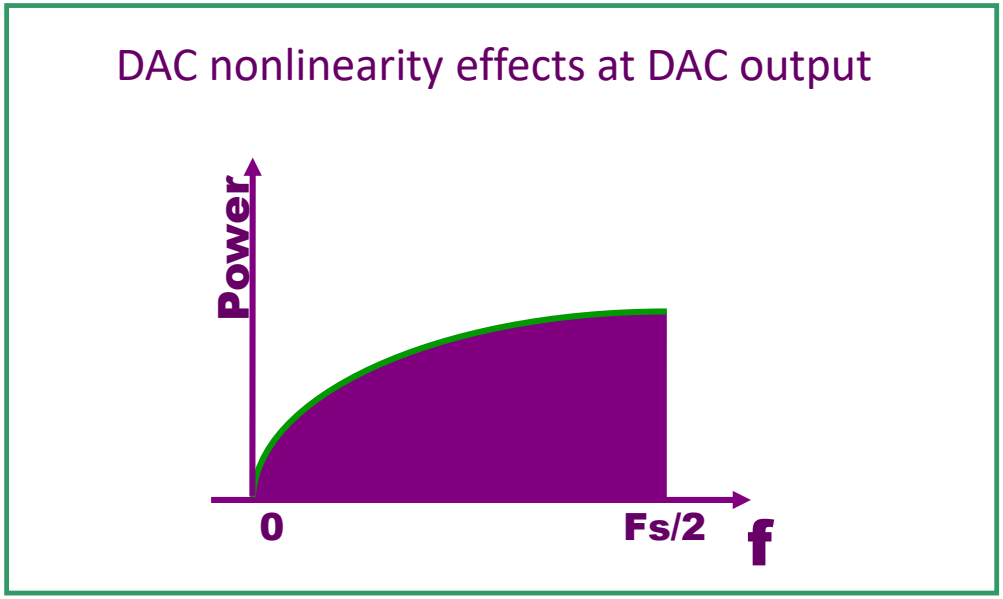




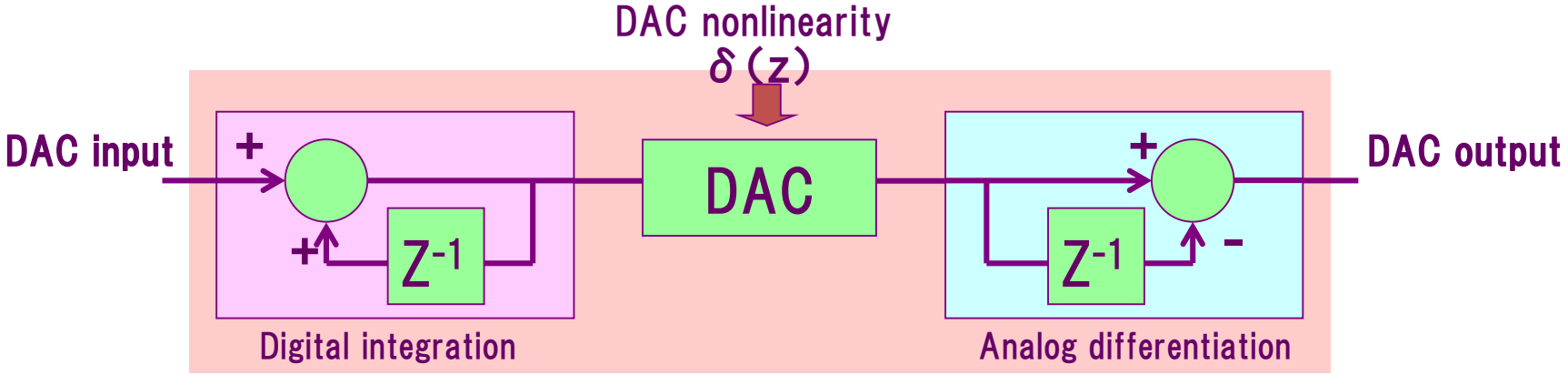
Equivalent LP DWA Algorithm

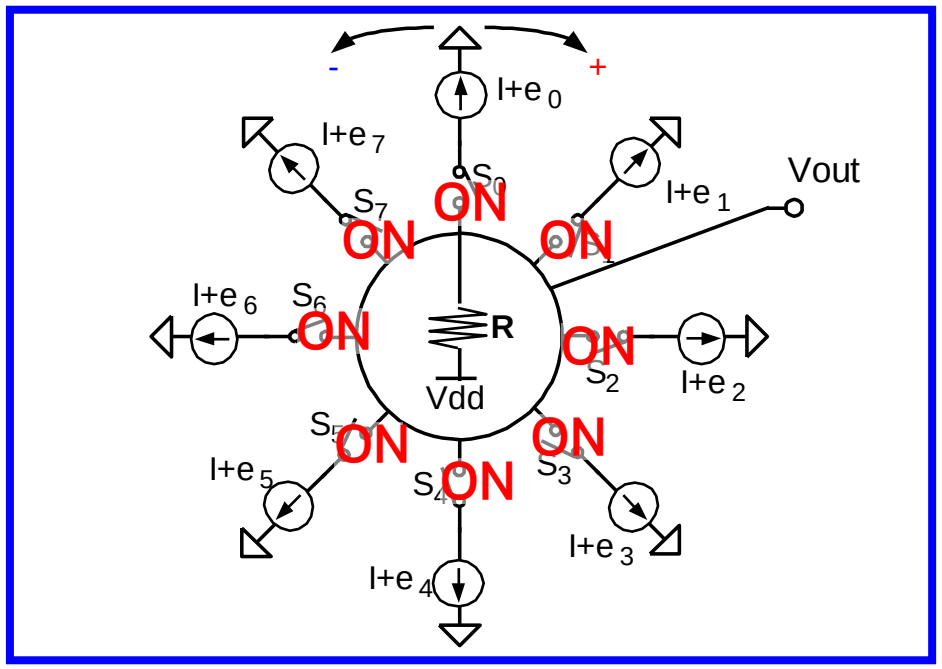


- Signal →Integration x Differentiation＝Flat
- DAC Nonlinearity →Differentiation（High Pass）

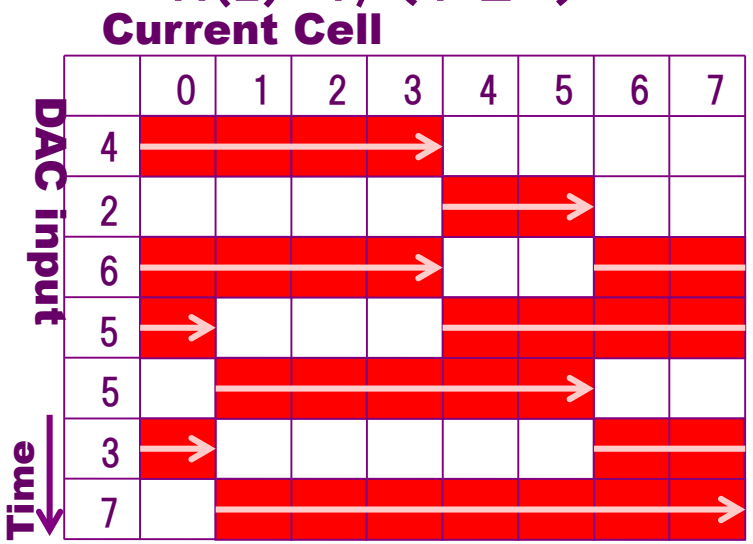


LP DWA Algorithm Realization

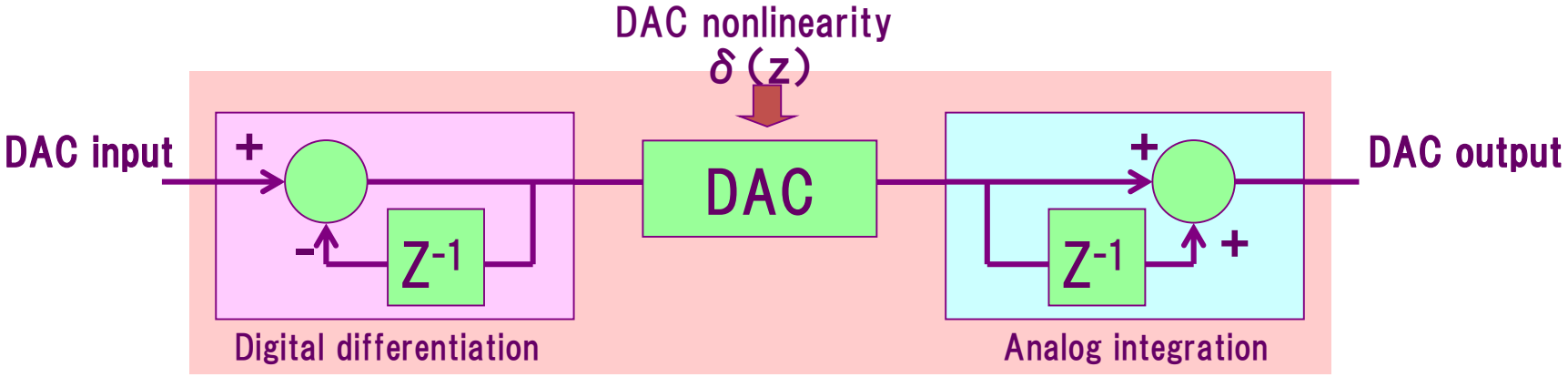




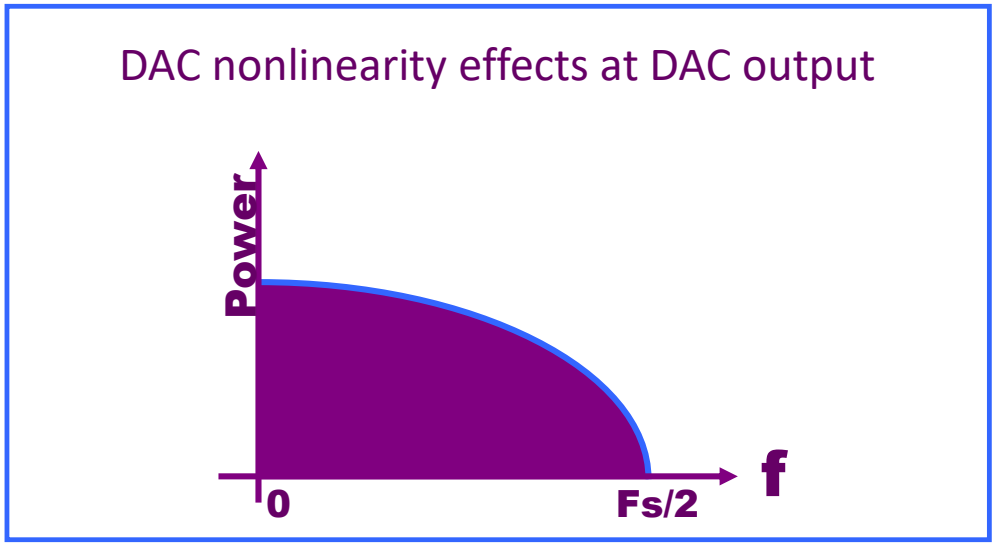
$H(z)=1/(1-Z^{-1})$



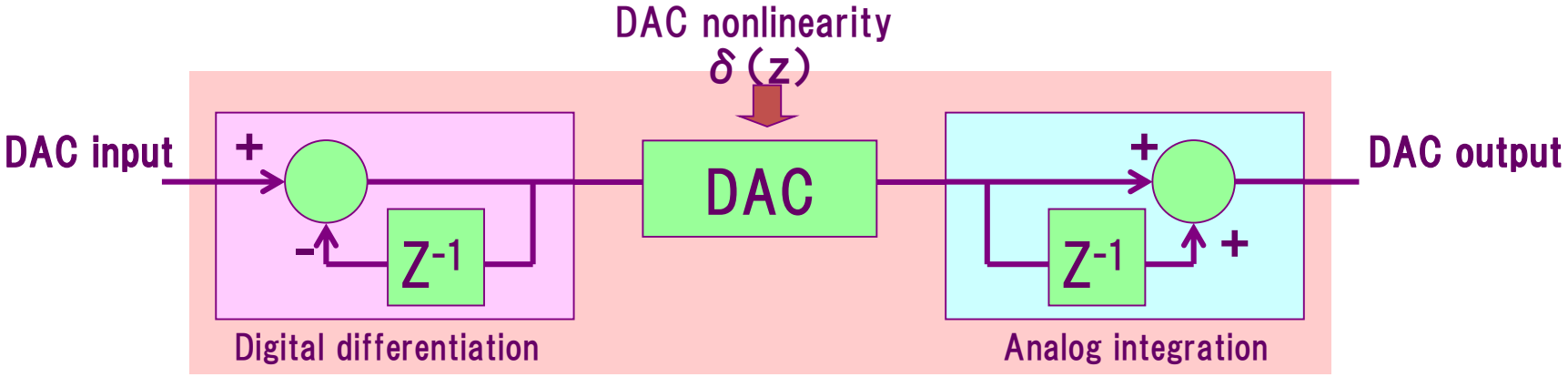
Let's Consider HP DWA Algorithm

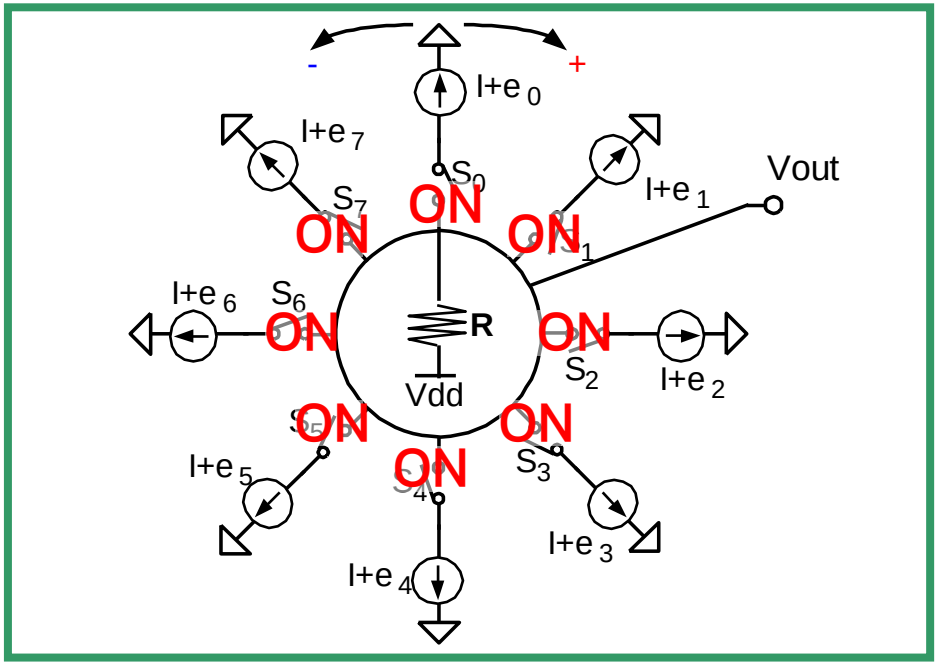


- Signal → Differentiation x Integration＝Flat
- DAC Nonlinearity →Integration（Low Pass）

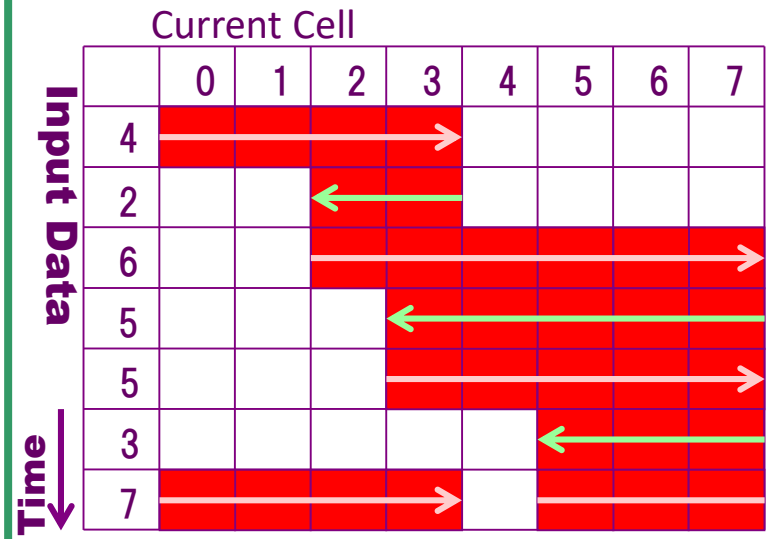


HP DWA Algorithm Realization





$H(z)=1/(1+Z^{-1})$



Back and forth

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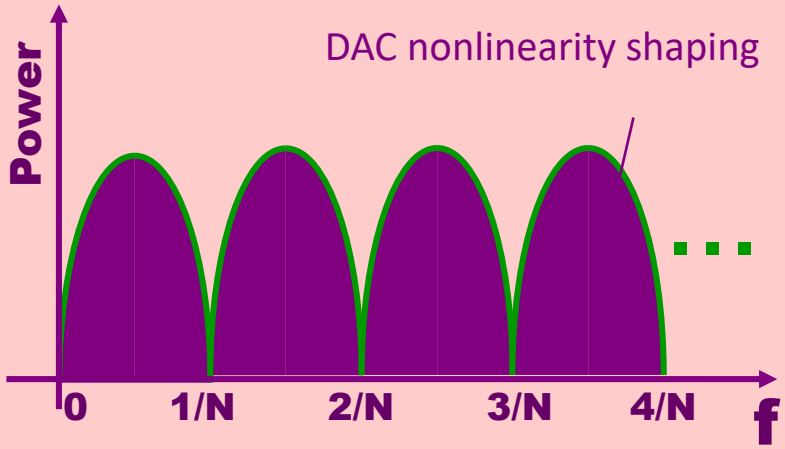
- What is DWA ?
- LP, HP DWA
- **Multi-Bandpass DWA**
- Multi-Bandpass Complex DWA
- Second-Order DWA
- Application to Multi-bit ΔΣ TDC
- Conclusion

[1] A. Motozawa, H. Kobayashi, et. al.,
"Multi-BP ΔΣ Modulation Techniques and Their Applications",
IEICE Tran, J90-C(Feb. 2007).

Multi-Bandpass DWA

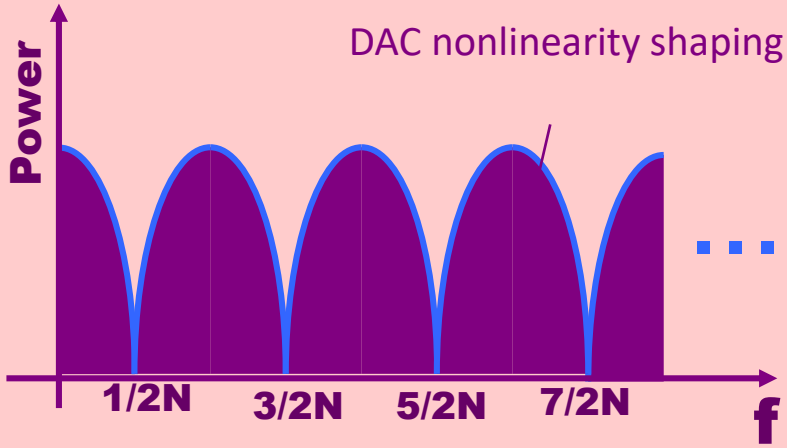
Type I DWA

- **N pointers**
- **N-channel interleave of LP DWA algorithm**



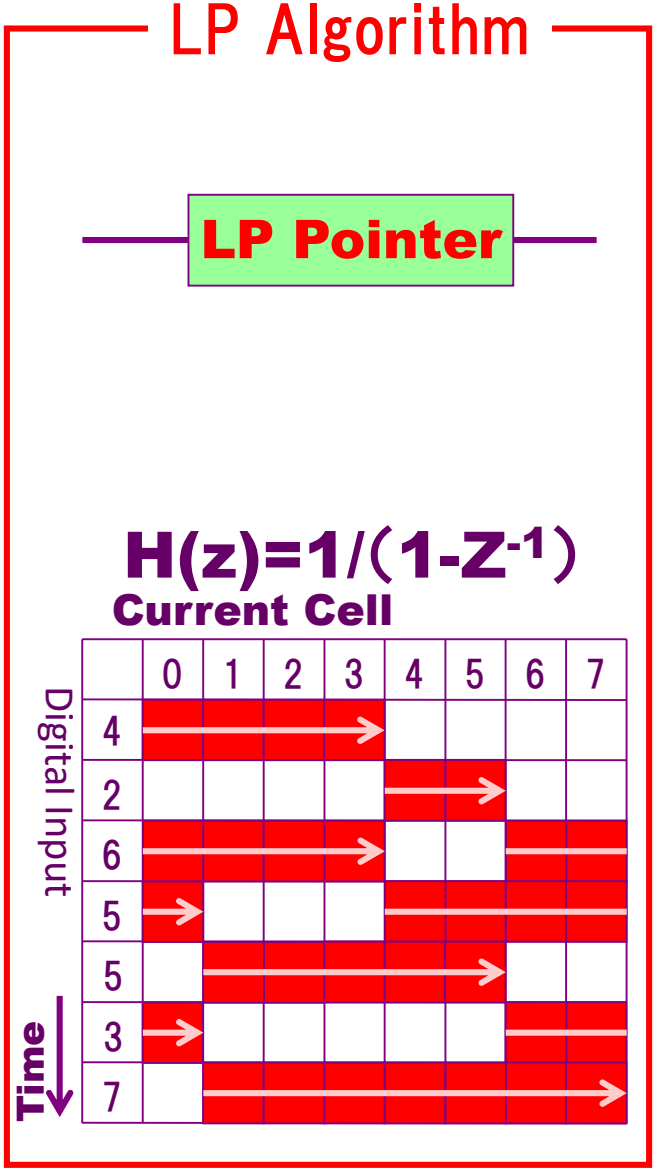
Type II DWA

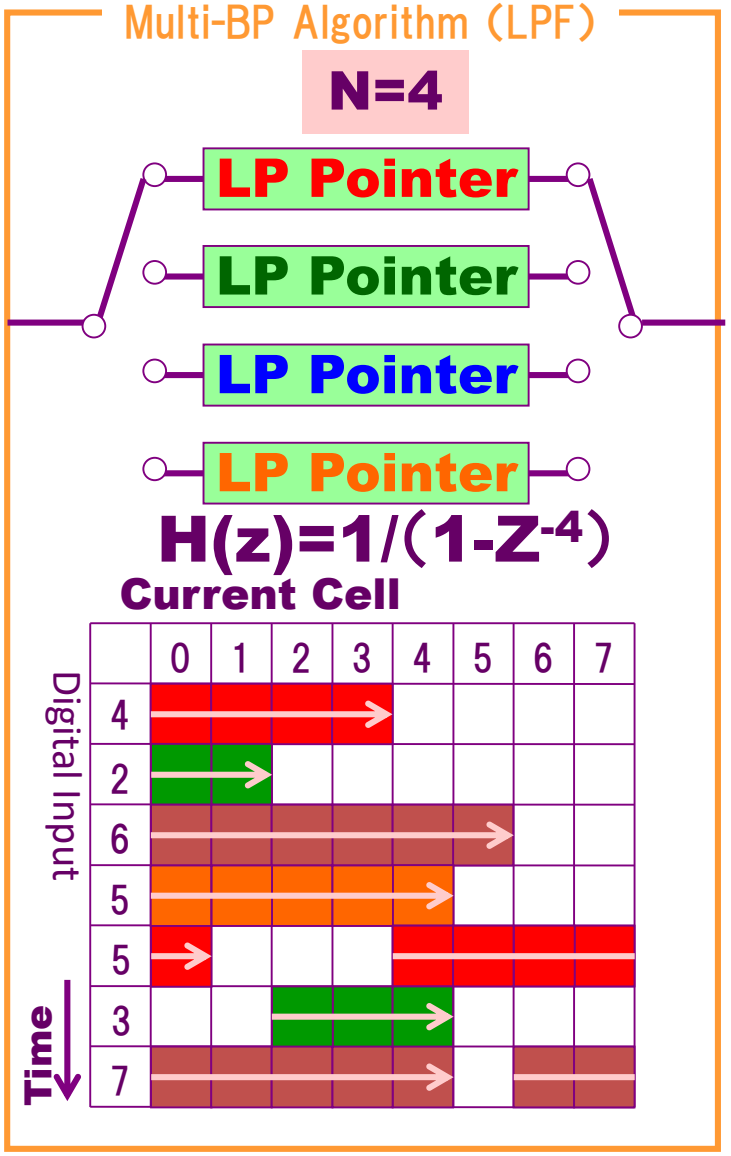
- **N pointers**
- **N-channel interleave of HP DWA algorithm**



Type I

LP ⇒ Multi-BP





Type Ⅱ

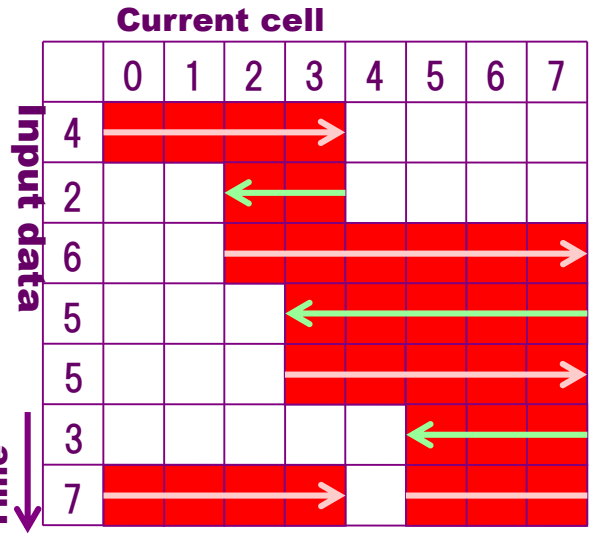
HP ⇒ BP ⇒ Multi-BP

HP Algorithm

HP Pointer

$H(z)=1/(1+Z^{-1})$

Back and forth



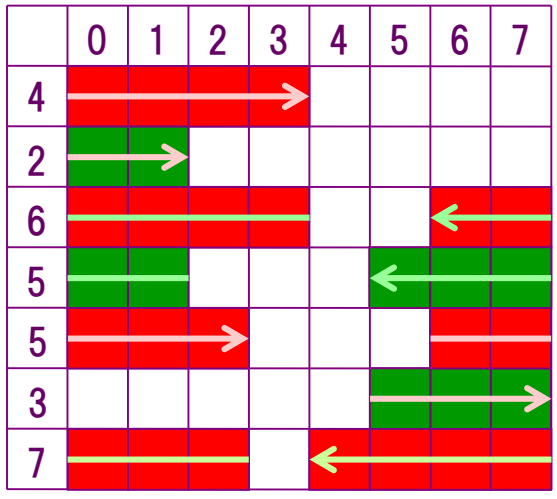
BP Algorithm

N=2

HP Pointer

HP Pointer

$H(z)=1/(1+Z^{-2})$



Multi-BP Algorithm

N=4

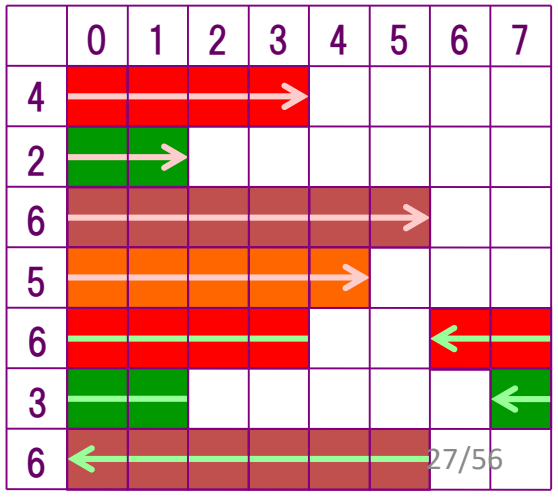
HP Pointer

HP Pointer

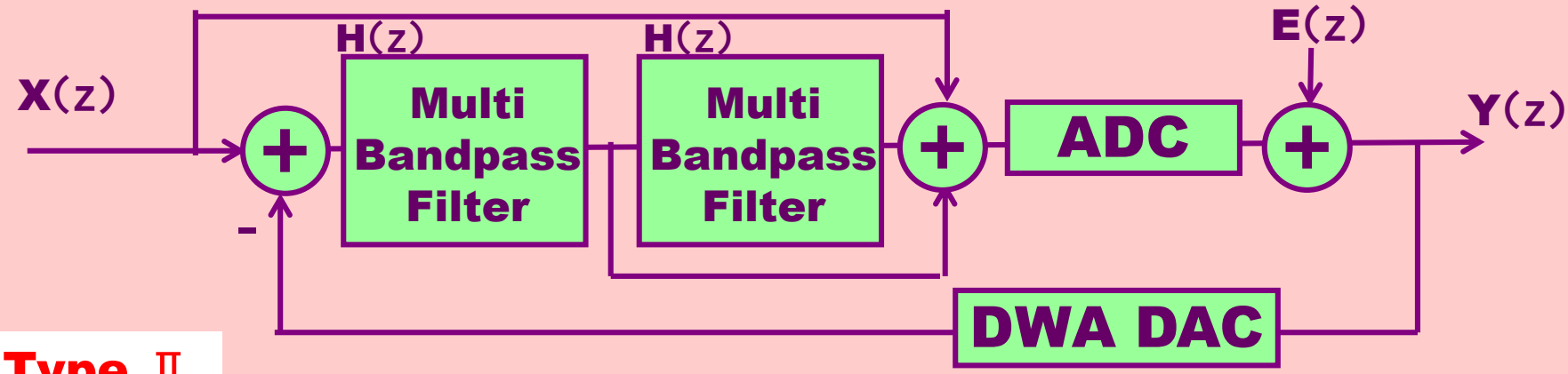
HP Pointer

HP Pointer

$H(z)=1/(1+Z^{-4})$



Multi-BP Type Ⅱ N=4



$$H(z) = \frac{-Z^{-4}}{1+Z^{-4}}$$

$$STF = -Z^{-4}$$

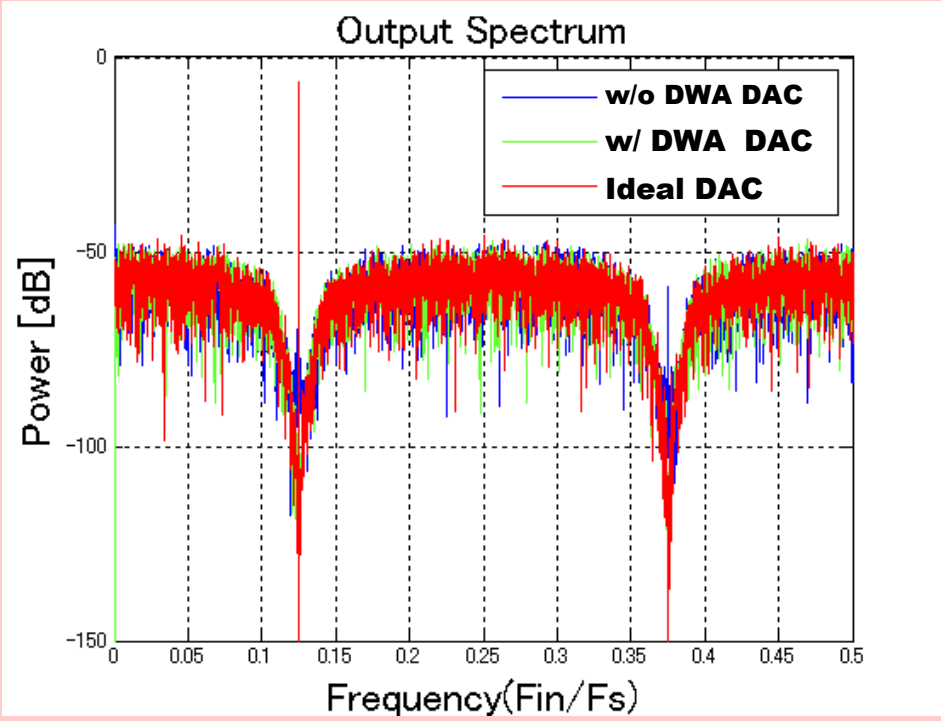
$$NTF = (1+Z^{-4})^2$$

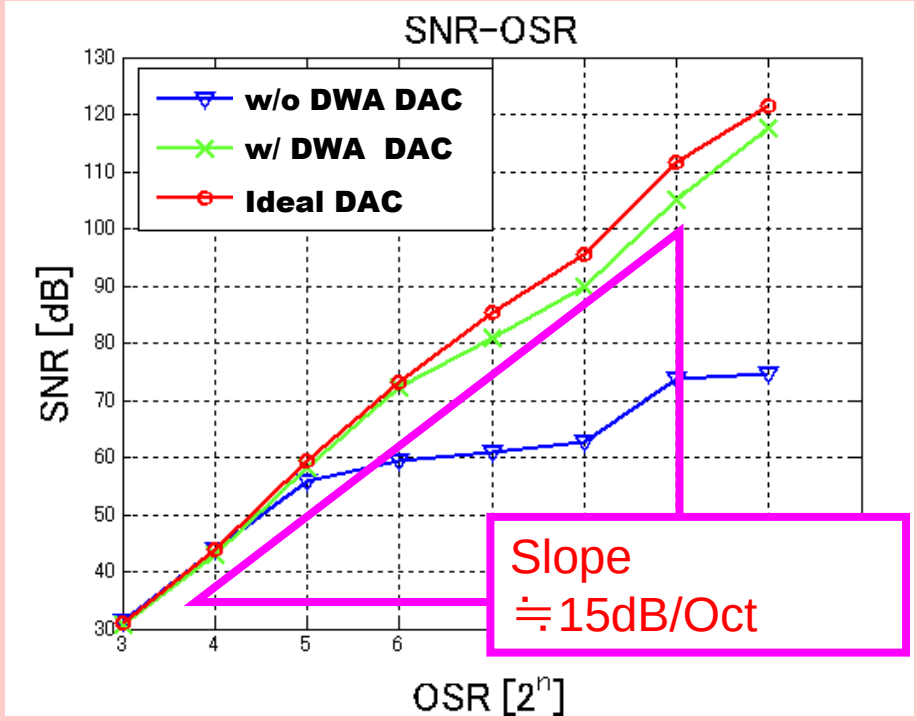
Signal Bands

1/8, 3/8

X Fs

Multi-BP Type Ⅱ N=4 Simulation Results





Multi-BP DWA algorithm is effective

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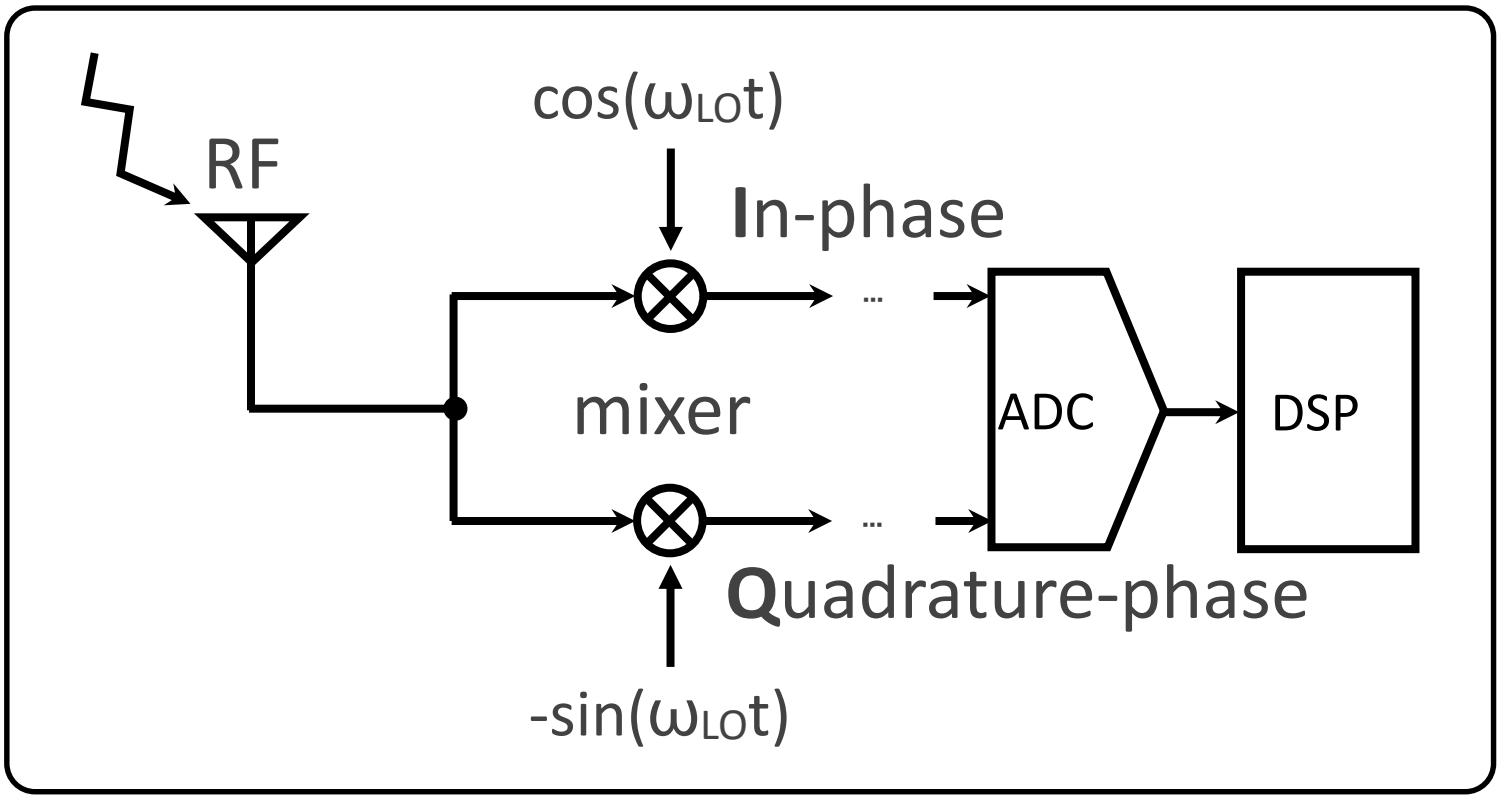
[1] M. Murakami, H. Kobayashi, et.al.,
"I-Q Signal Generation Techniques for Communication IC Testing and ATE Systems", IEEE International Test Conference (Nov. 2016).

[2] H. San, H. Kobayashi, et. al., "A Second-Order Multi-bit Complex Bandpass ΔΣ AD Modulator With I, Q Dynamic Matching and DWA Algorithm", IEICE Trans. Electron, (June 2007).

Necessity of I,Q signal

RF analog front-end of Receiver IC



Need testing!

Necessity of Multi-Tone Signal

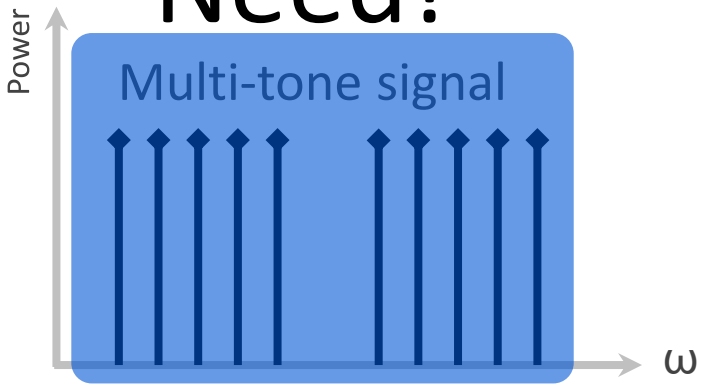
Linearity testing of

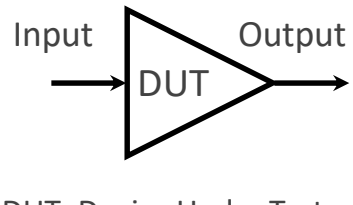
- ✓ Mixer
- ✓ Up/Down converter
- ✓ Radio communication system , etc.

⇩

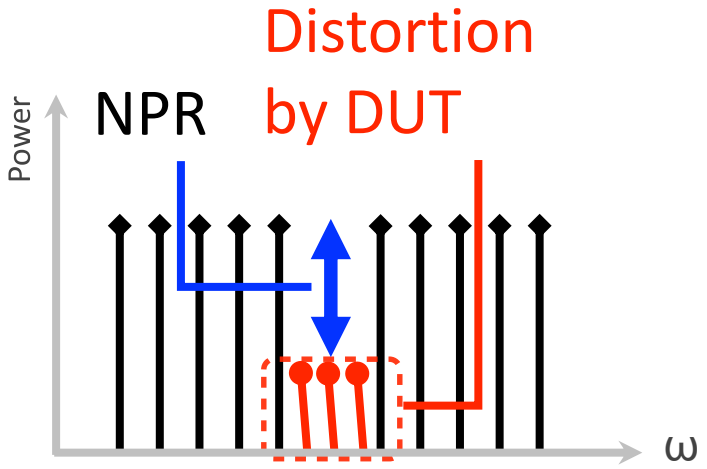
Noise Power Ratio （NPR）

Need!

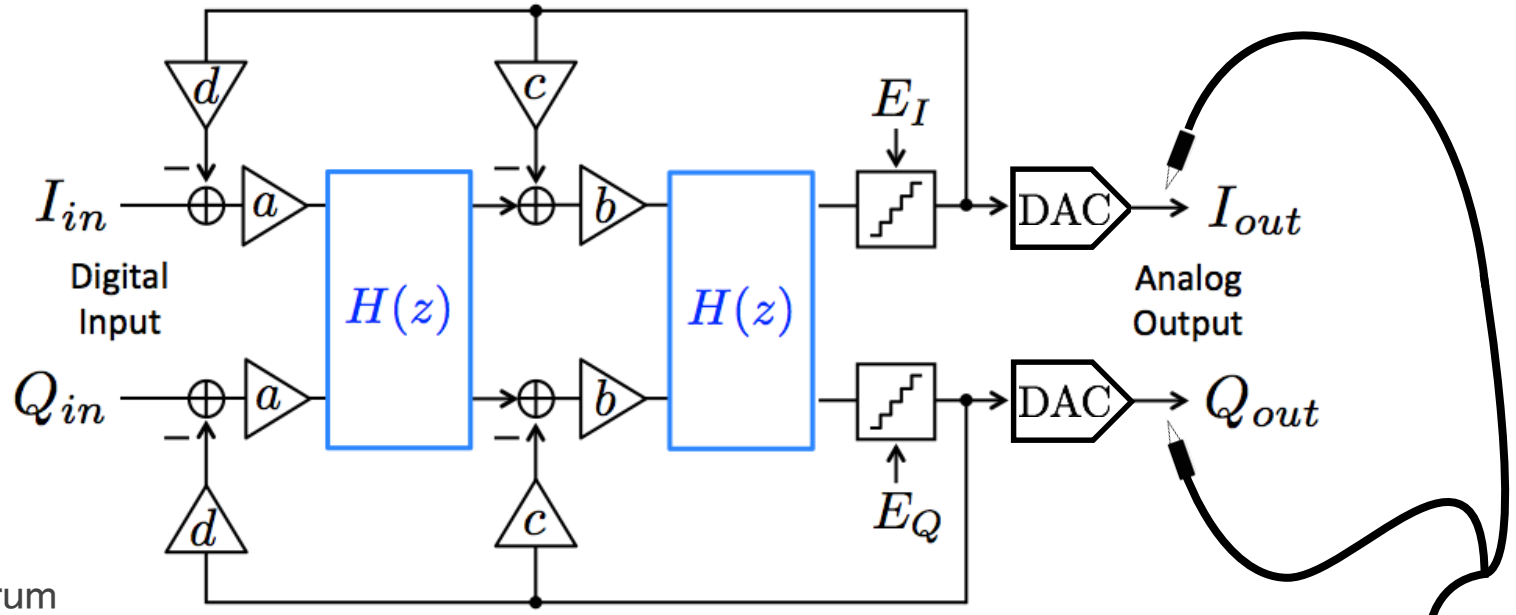




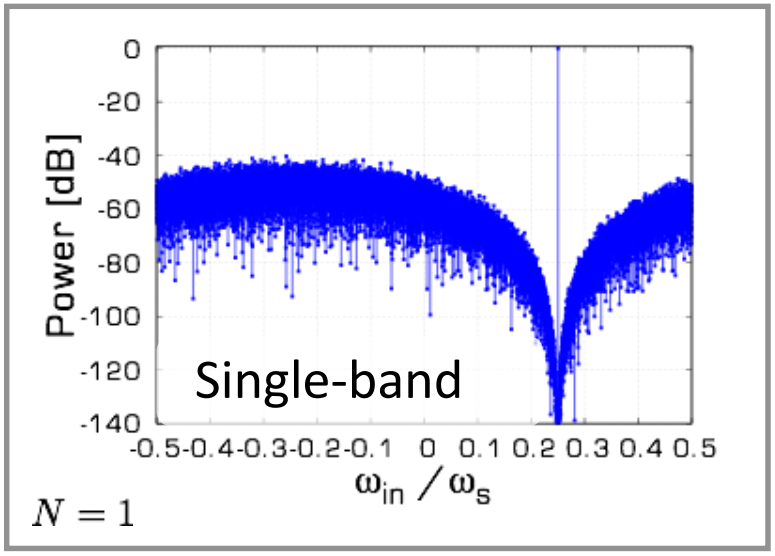
DUT : Device Under Test

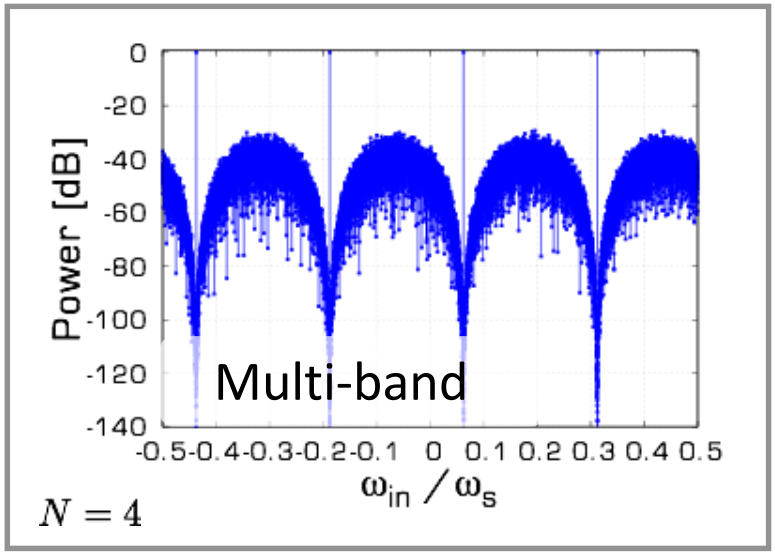


2nd-order Complex Multi-BP ΔΣ DAC

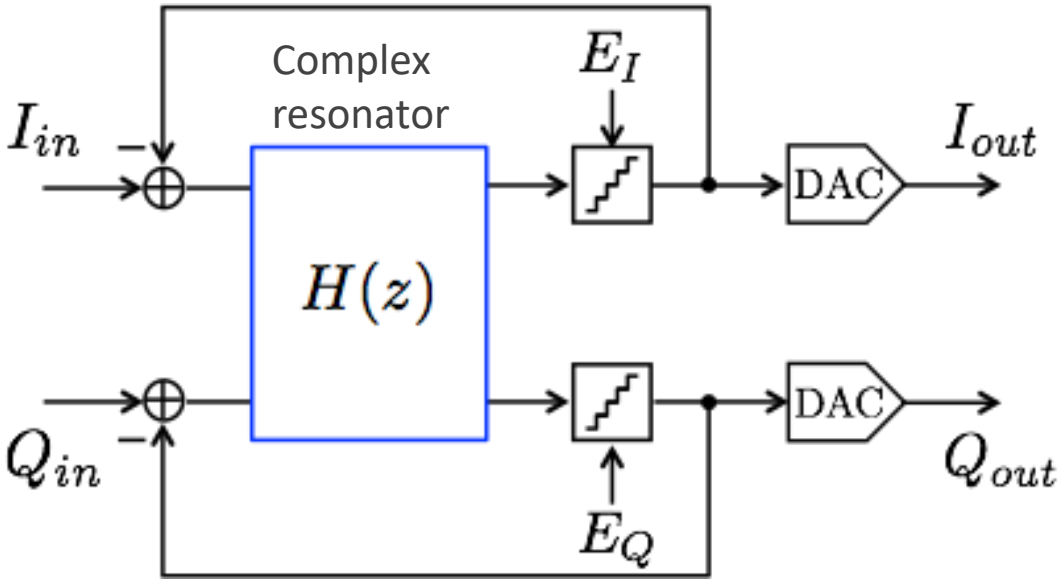


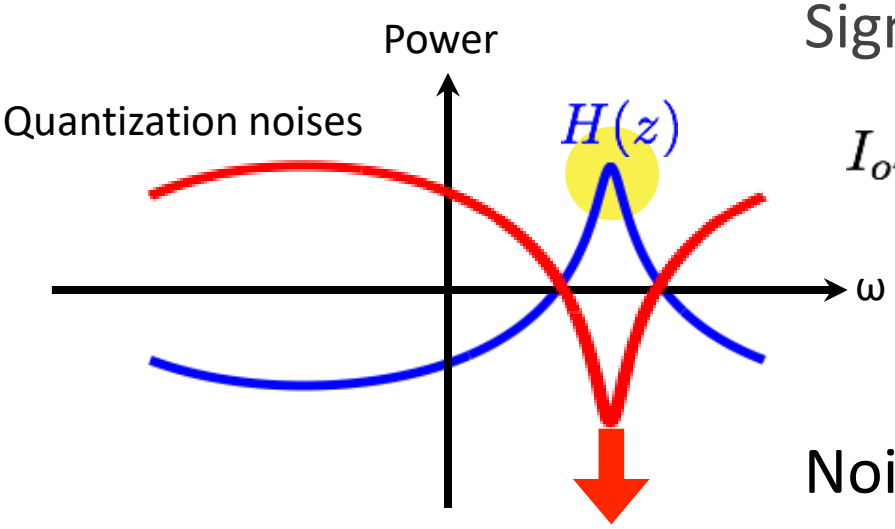
Output spectrum





Principle of Complex BP Noise Shape





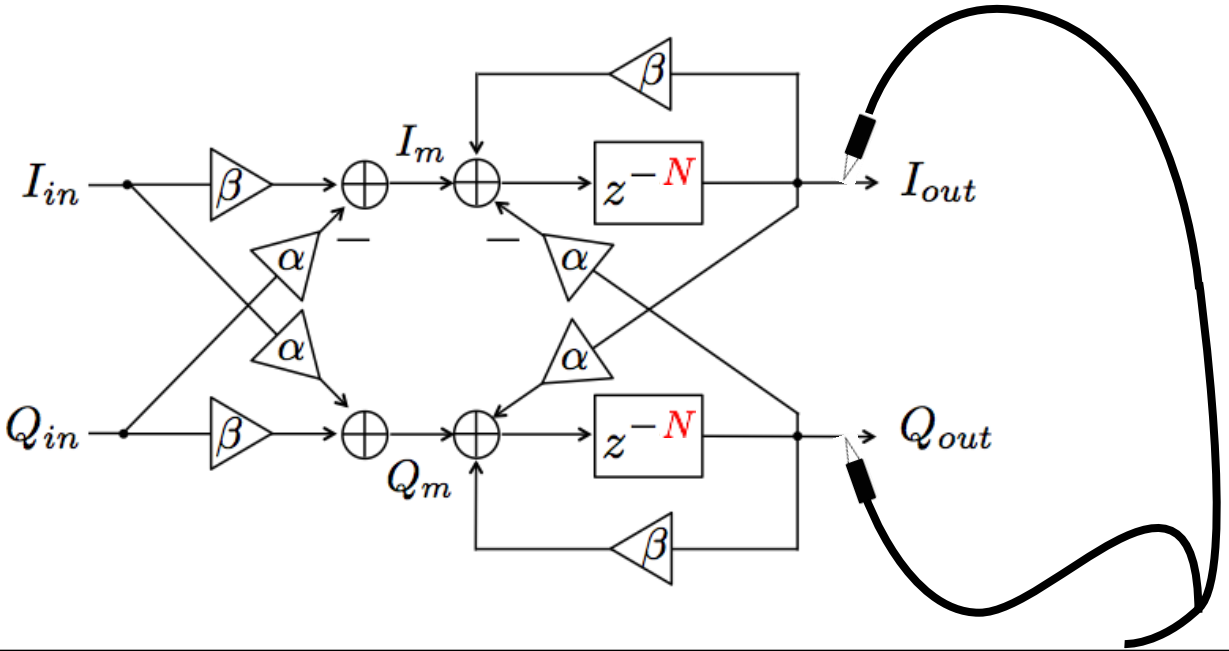
Signal Transfer Function = 1

$$I_{out} + jQ_{out} = \boxed{1}(I_{in} + jQ_{in})$$

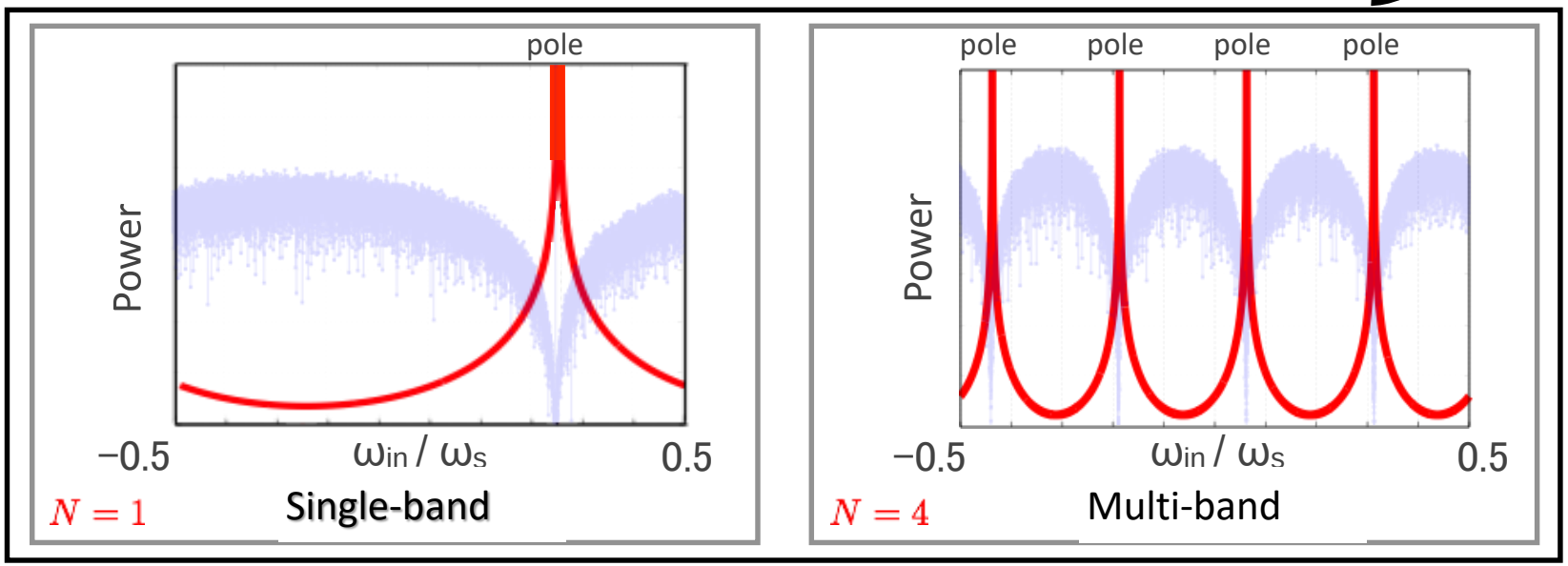
$$+ \boxed{0}(E_I + jE_Q)$$

Noise Transfer Function = 0

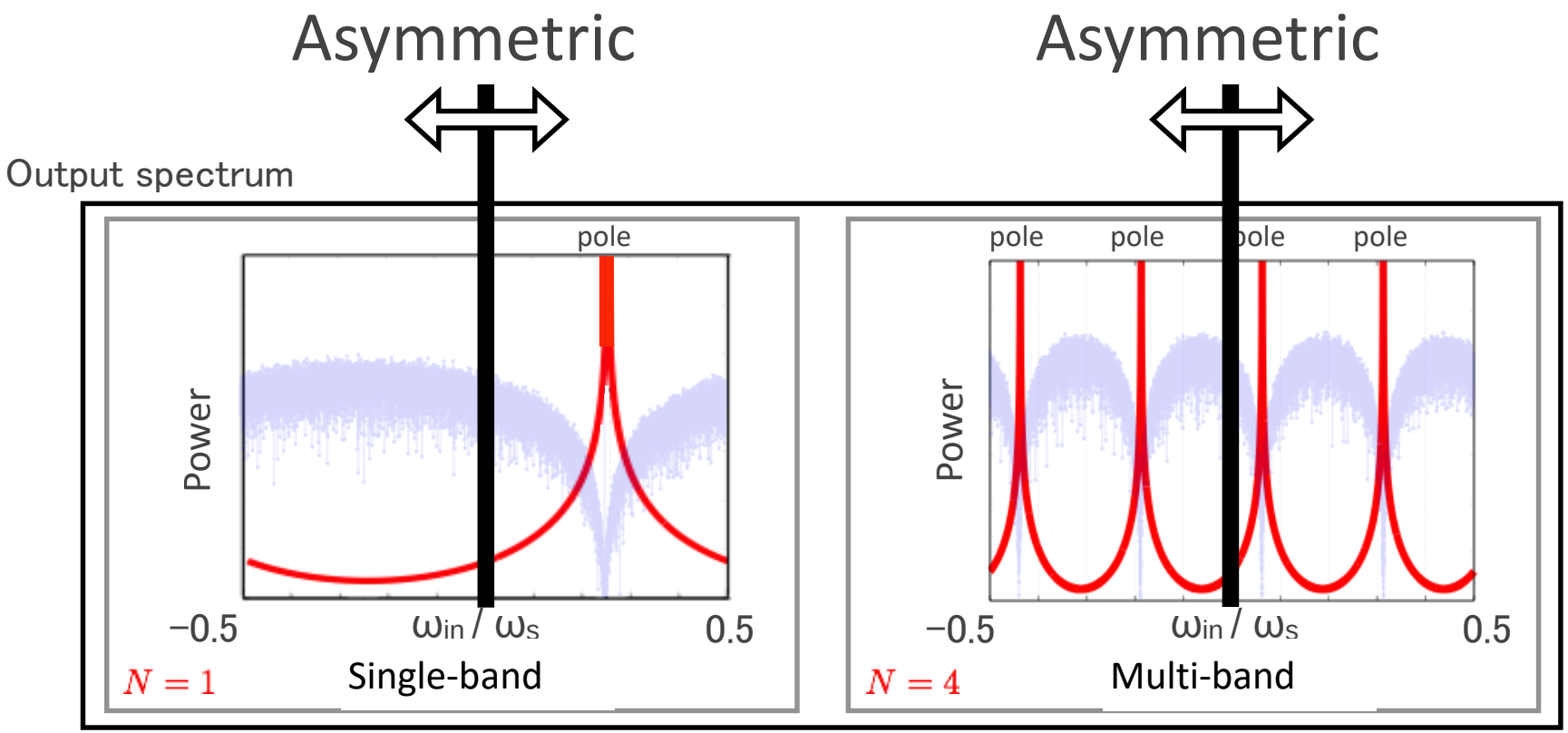
Complex Resonator



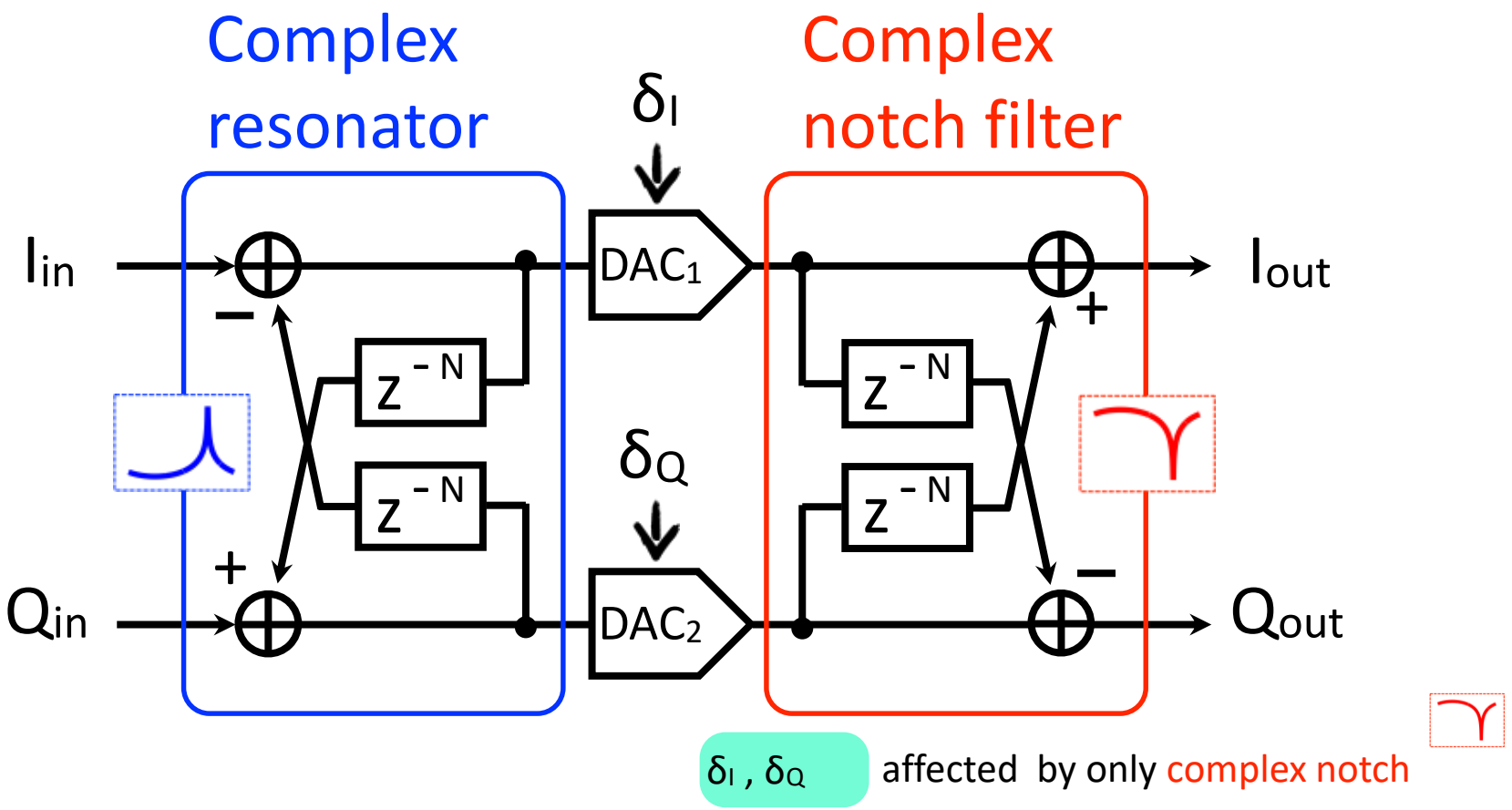
Output spectrum



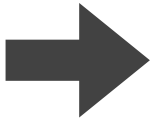
Complex Resonator



Equivalent Circuit of Complex DWA

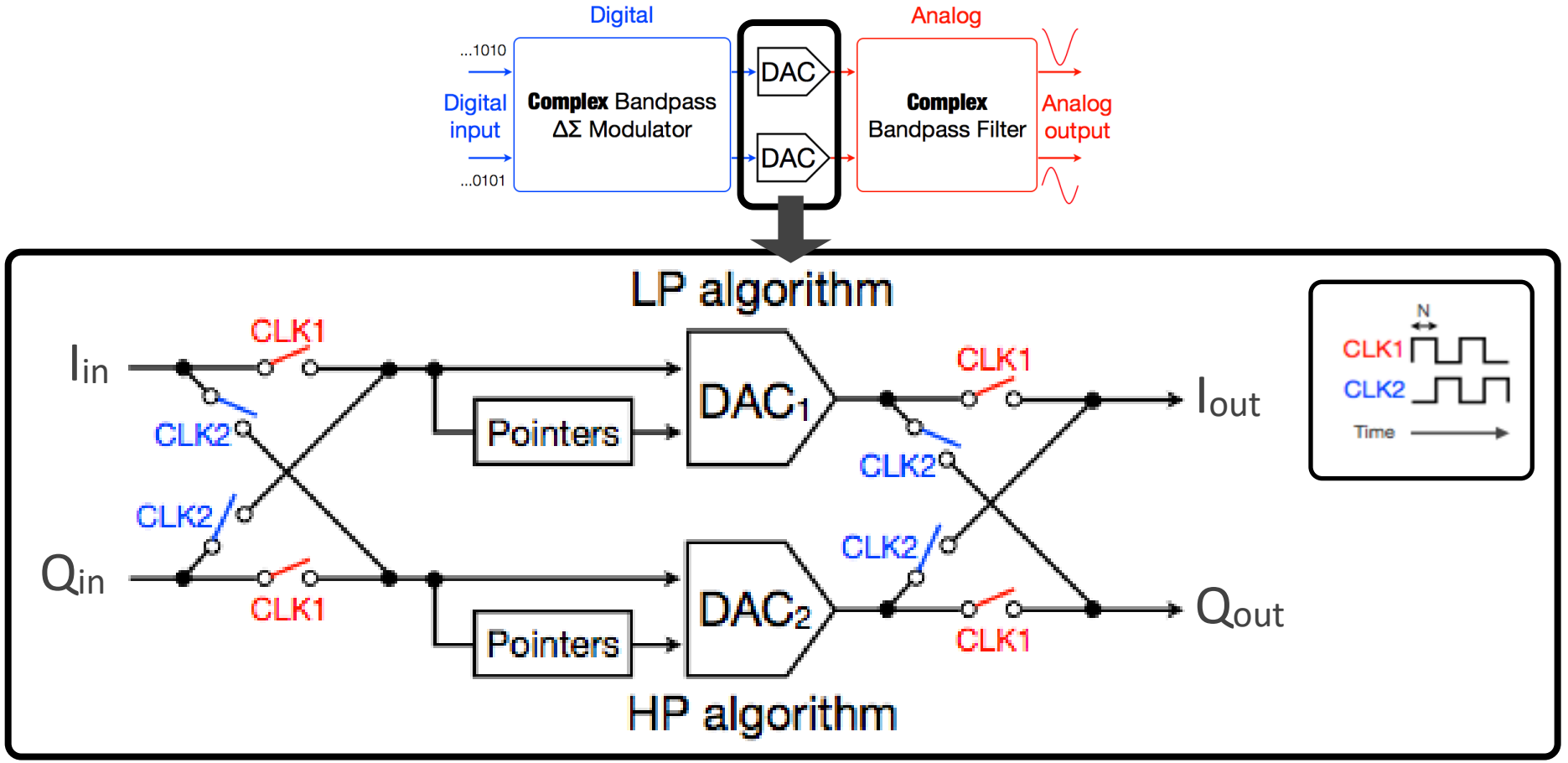


DAC input can be ∞ 



Can’t be realized directly

Equivalent Circuit Implementation

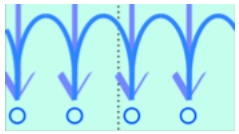


- ✦ Attach pointers
- ✦ Exchange upper-path and lower-path every N clock

➡ Complex DWA is realized.

Complex Multi-Bandpass DWA Algorithm

N = 4（four zero points）



DAC$_1$（**LP** operation）　　DAC$_2$（**HP** operation）

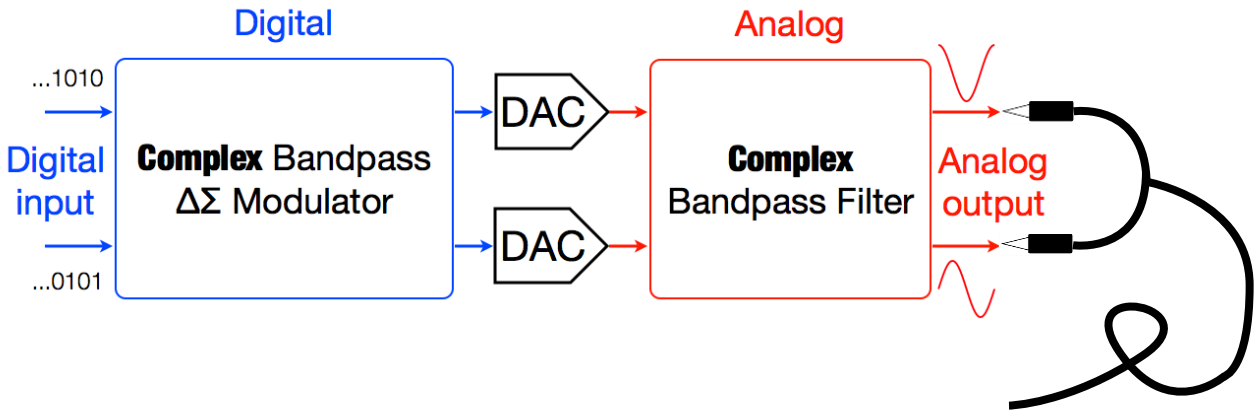
TIME

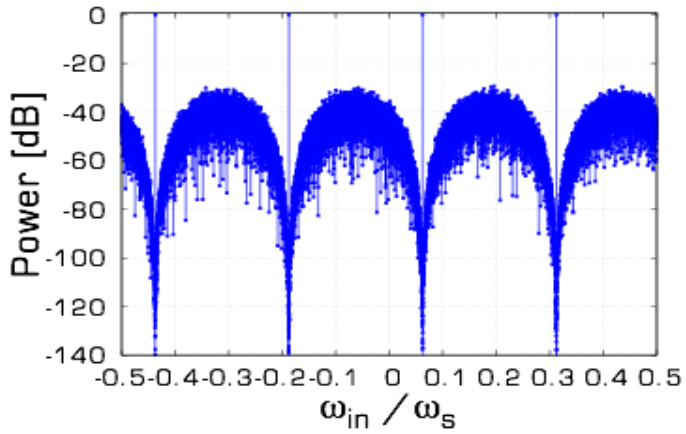
DAC Input;

I_{in}	Q_{in}	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
4	2								
3	2								
2	6								
2	1								
6	7								
1	5								
7	4								
5	3								

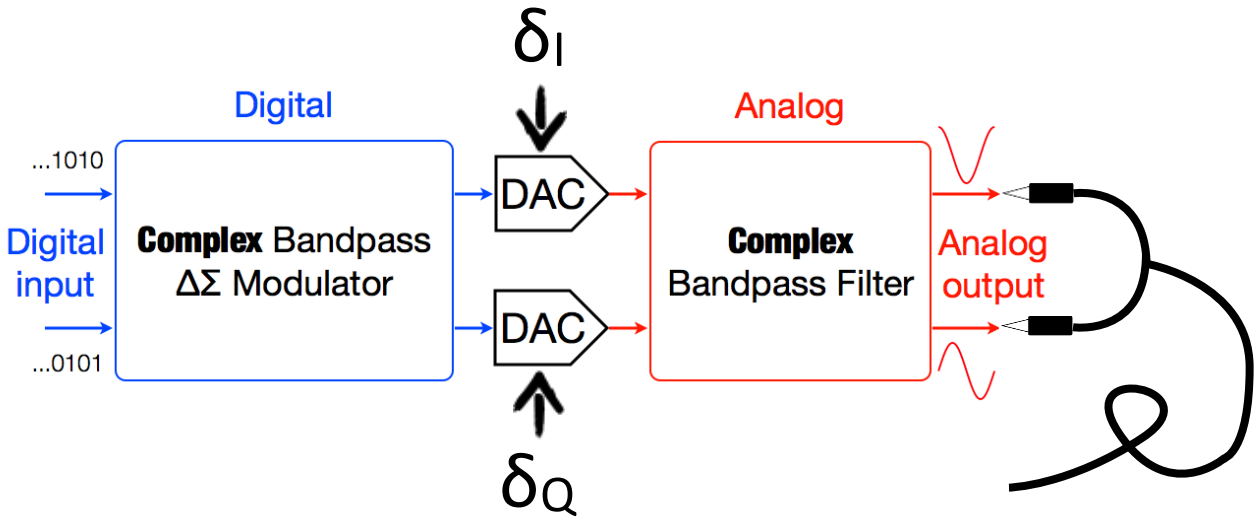
I_{in}	Q_{in}	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
4	2								
3	2								
2	6								
2	1								
6	7								
1	5								
7	4								
5	3								

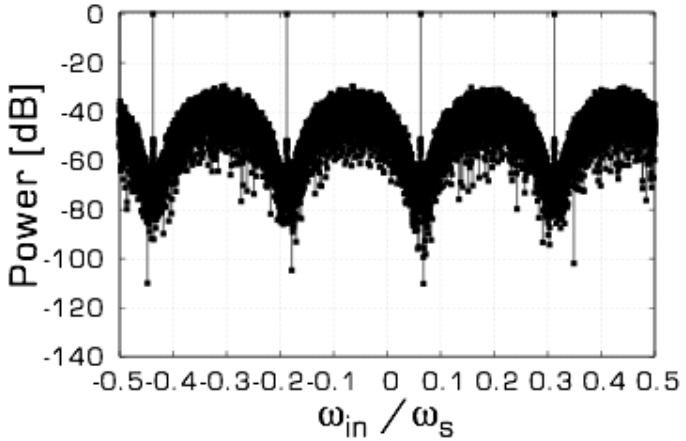
Simulation Result ~Ideal Linear DAC~





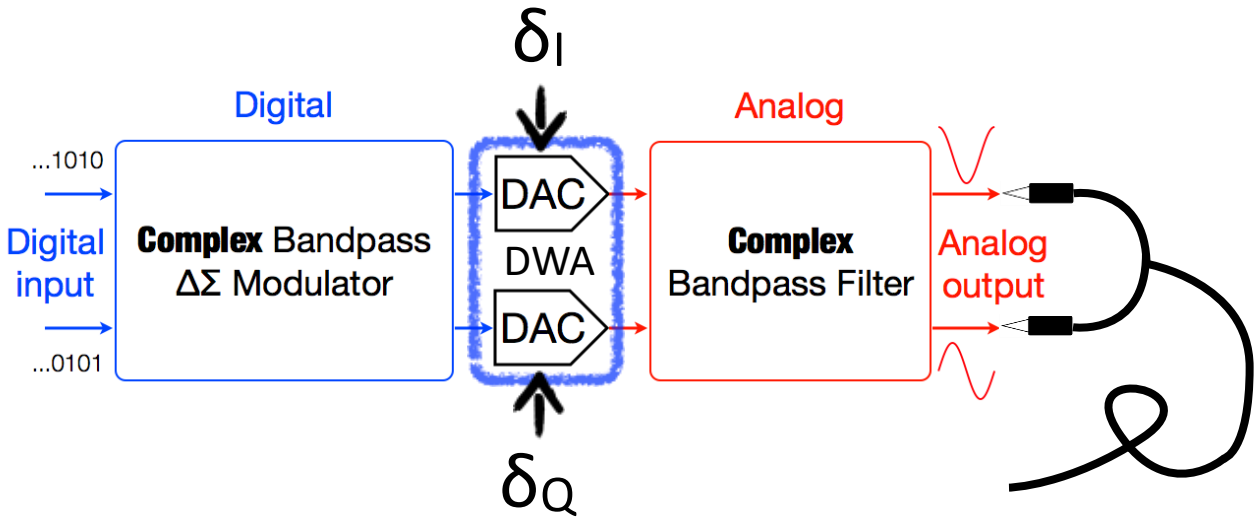
Simulation Result ~Actual Non-Linear DAC~

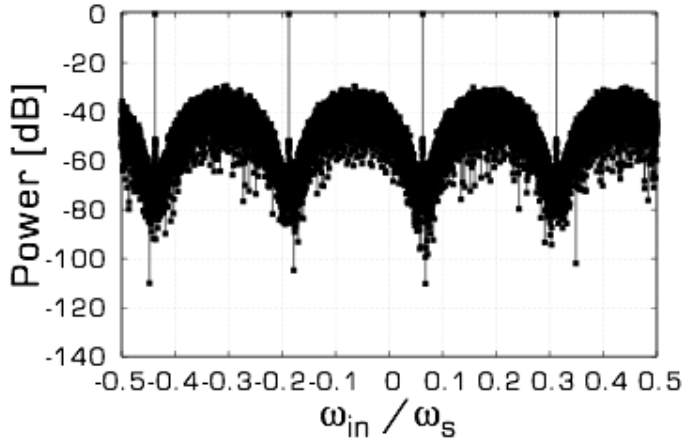




Notches filled with noise

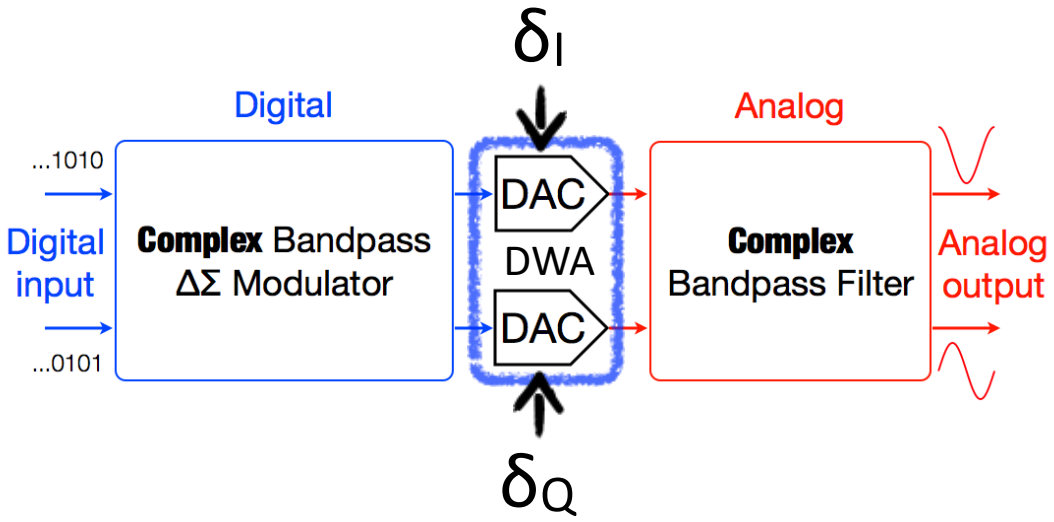
Simulation Result
~Actual Non-Linear DAC + DWA~

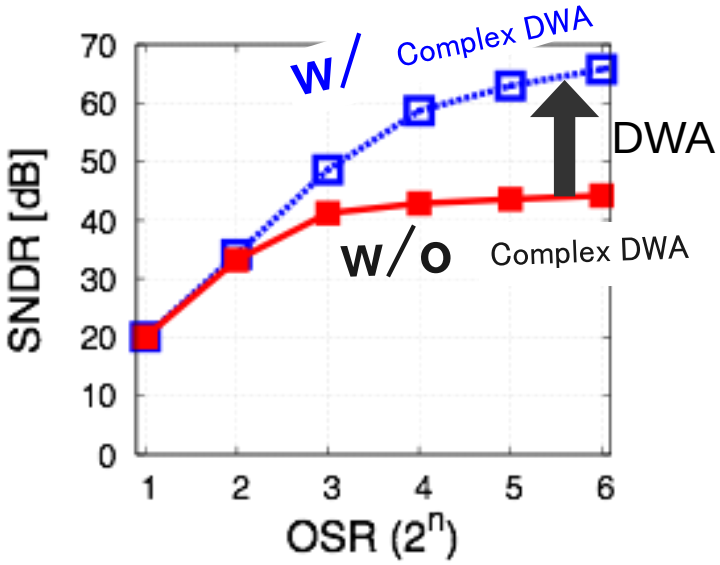


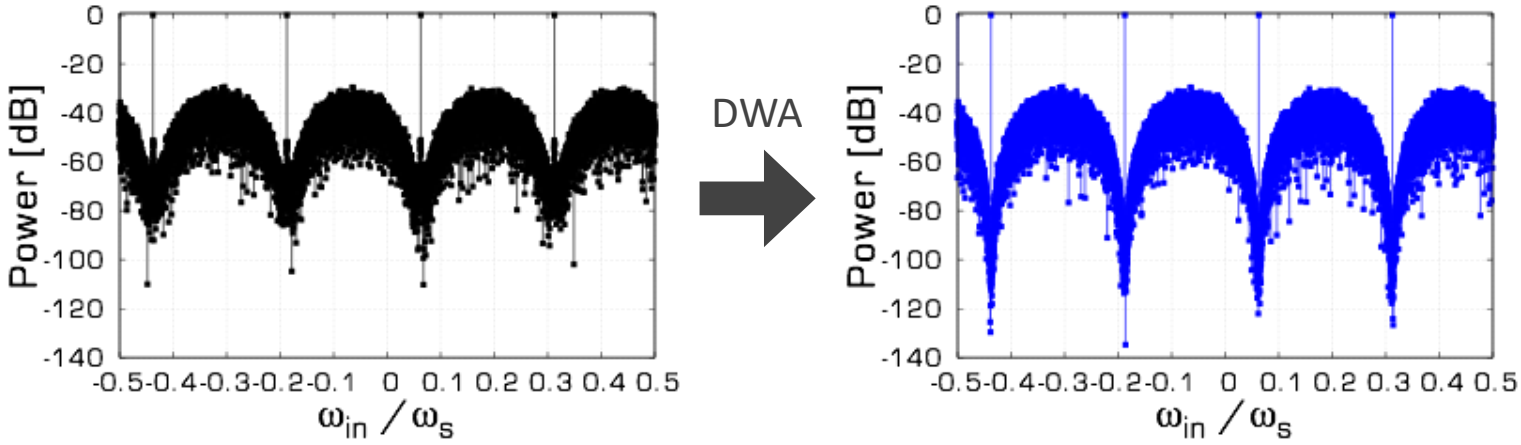


Notches filled with noise

Simulation Result
~Actual Non-Linear DAC + DWA~







Notches filled with noise → Steep Notches

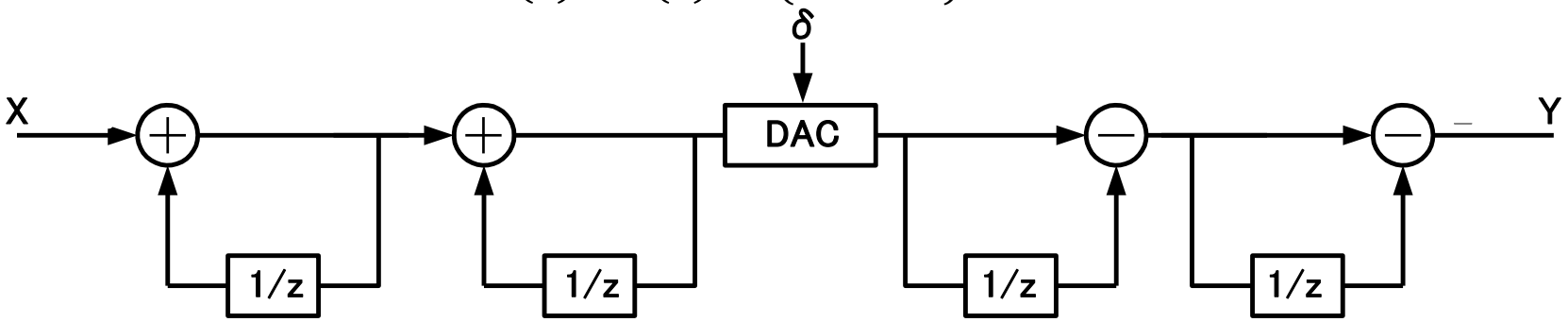
Contents

- Research Objective
- What is DWA ?
- LP, HP DWA
- Multi-Bandpass DWA
- Multi-Bandpass Complex DWA
- **Second-Order DWA**
- Application to Multi-bit ΔΣ TDC
- Conclusion

[1] H. Hagiwara, H. Kobayashi, et. al.,
"DA Converter Circuit Provided with DA Converter of
Segmented Switched Capacitor Type",
US Patent Application, Pub. No.: US 2005/0285768 A1 (Dec. 29, 2005).

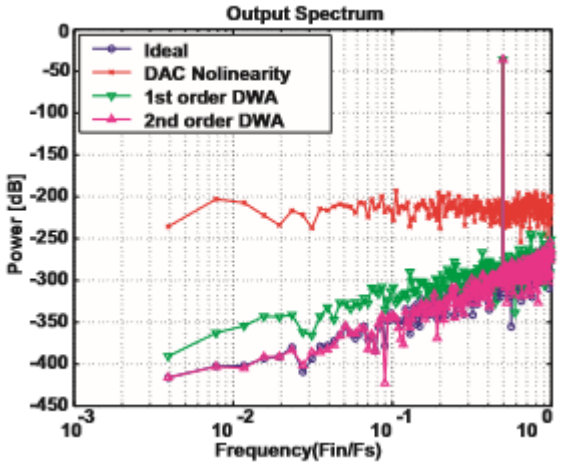
2nd-order DWA

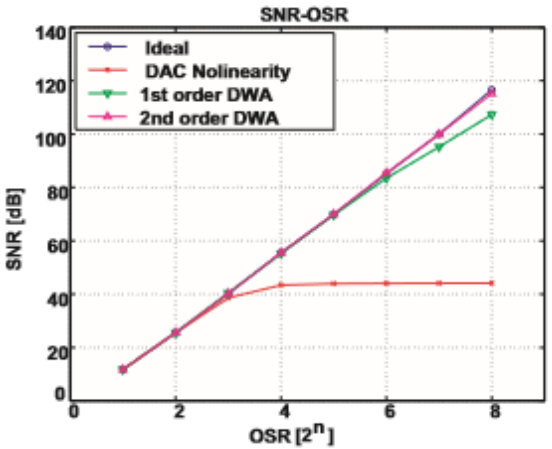
$$Y(z) = X(z) + (1 - z^{-1})^2 \delta(z)$$



2 integrators

2 differentiators





- 2nd-order DWA is more effective
- But its circuit/operation become complicated

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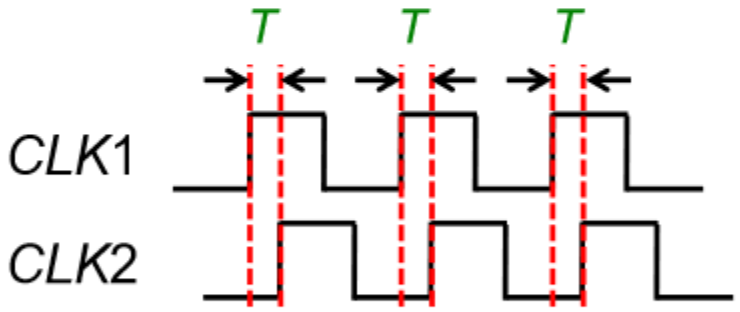
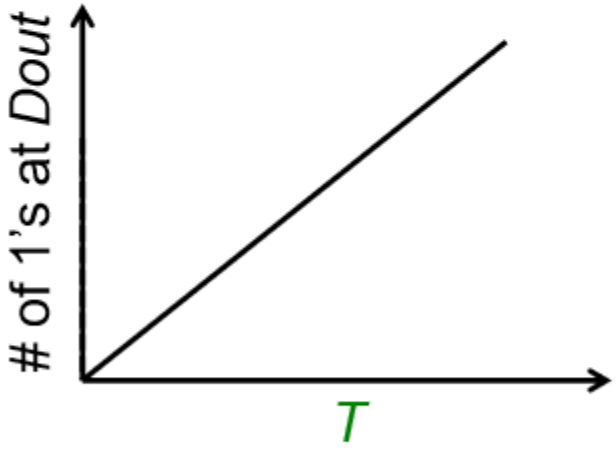
[1] T. Chujo, H. Kobayashi, et. al.,
"Timing Measurement BOST With Multi-bit Delta-Sigma TDC",
20th IEEE International Mixed-Signal Testing Workshop (June 2015).

ΔΣ TDC Features

Timing *T* measurement between CLK1 and CLK2

ΔΣ Time-to-Digital Converter (TDC)

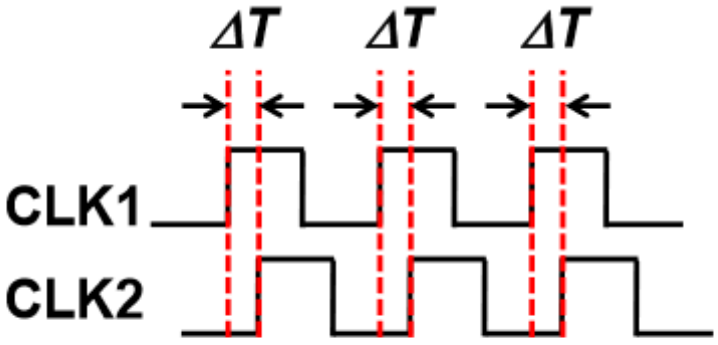




T ∝ # of 1' at *Dout*

- Simple circuit
- High linearity
- Measurement time → longer ⇒ time resolution → finer

Principle of ΔΣTDC



Dout # of 1's is proportional to ΔT

ΔT

# of 1's

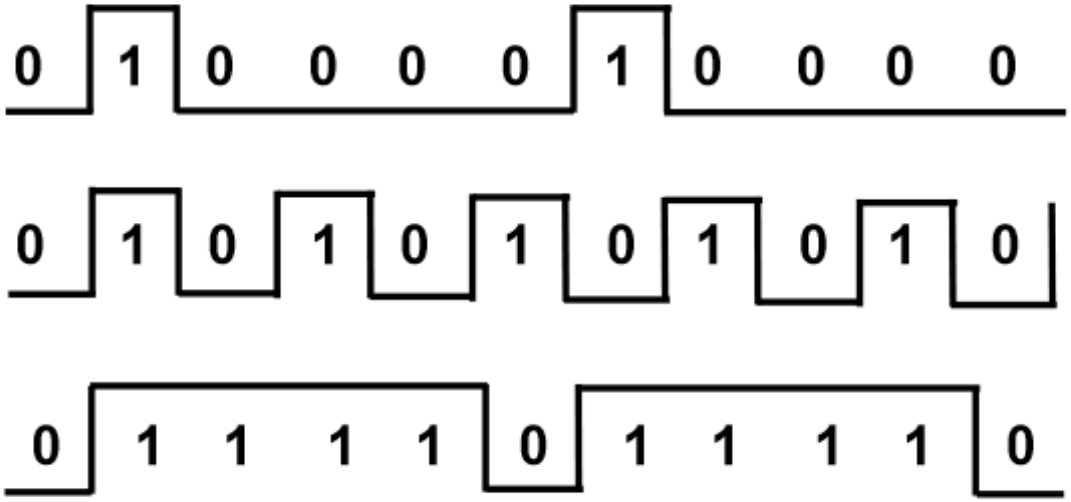
short

few

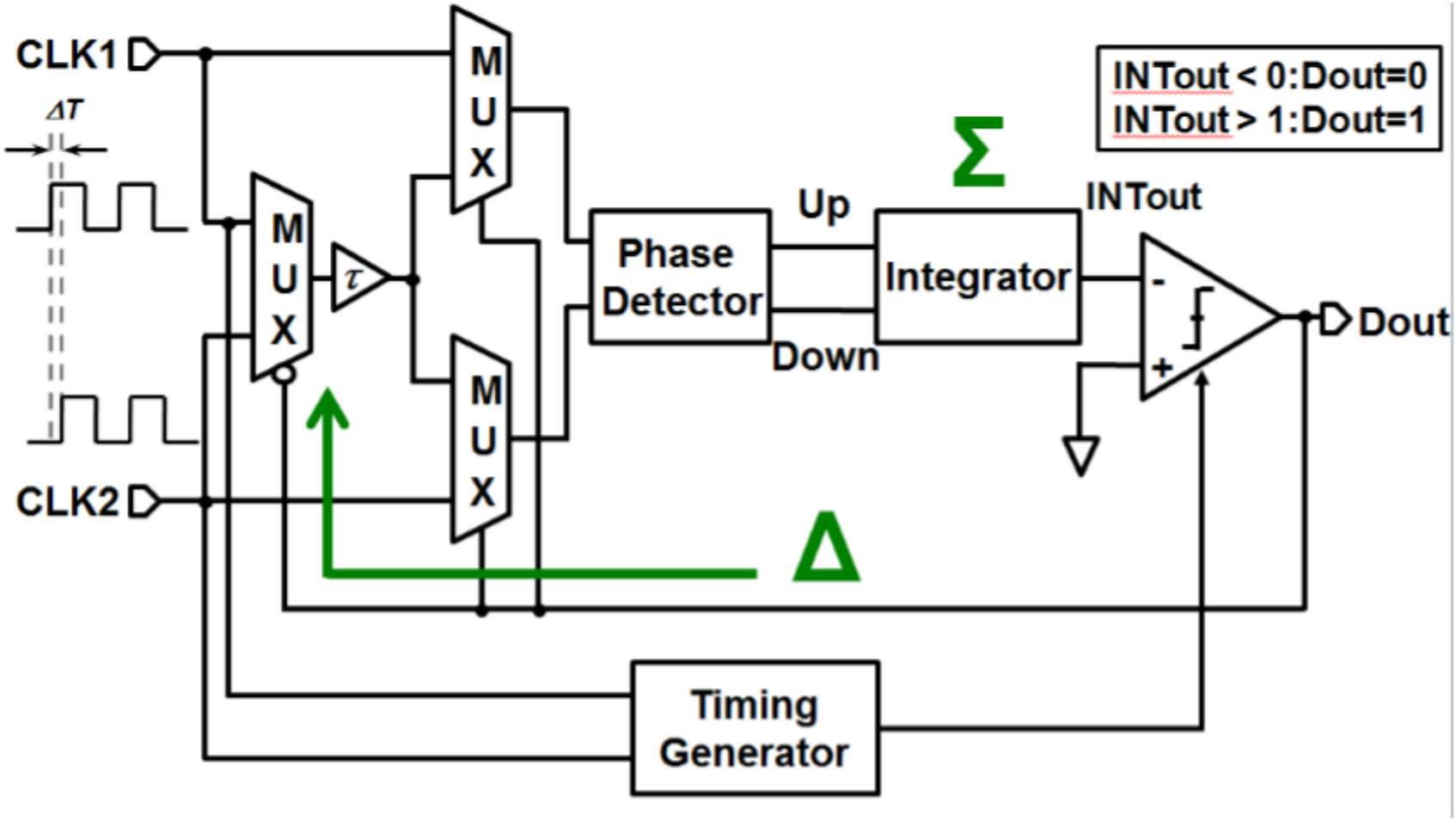
long

many

Dout



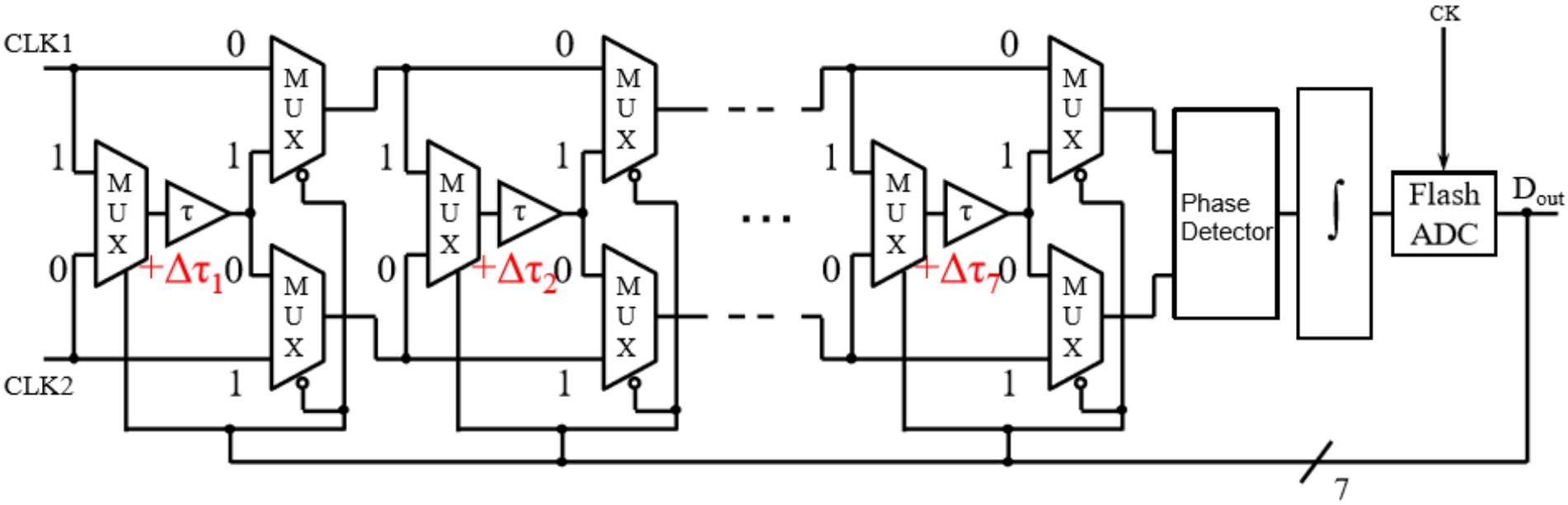
ΔΣTDC Configuration



[1] T. Chujo, H. Kobayashi, "Timing Measurement BOST With Multi-bit Delta-Sigma TDC", IEEE IMSTW (June 2015).

[2] Y. Osawa, H. Kobayashi, "Phase Noise Measurement Techniques Using Delta-Sigma TDC", IEEE IMS3TW (Sept. 2014).

Multi-Bit ΔΣ TDC



- 3-bit : 7 comparators and delays
- Fine time resolution with a given measurement time

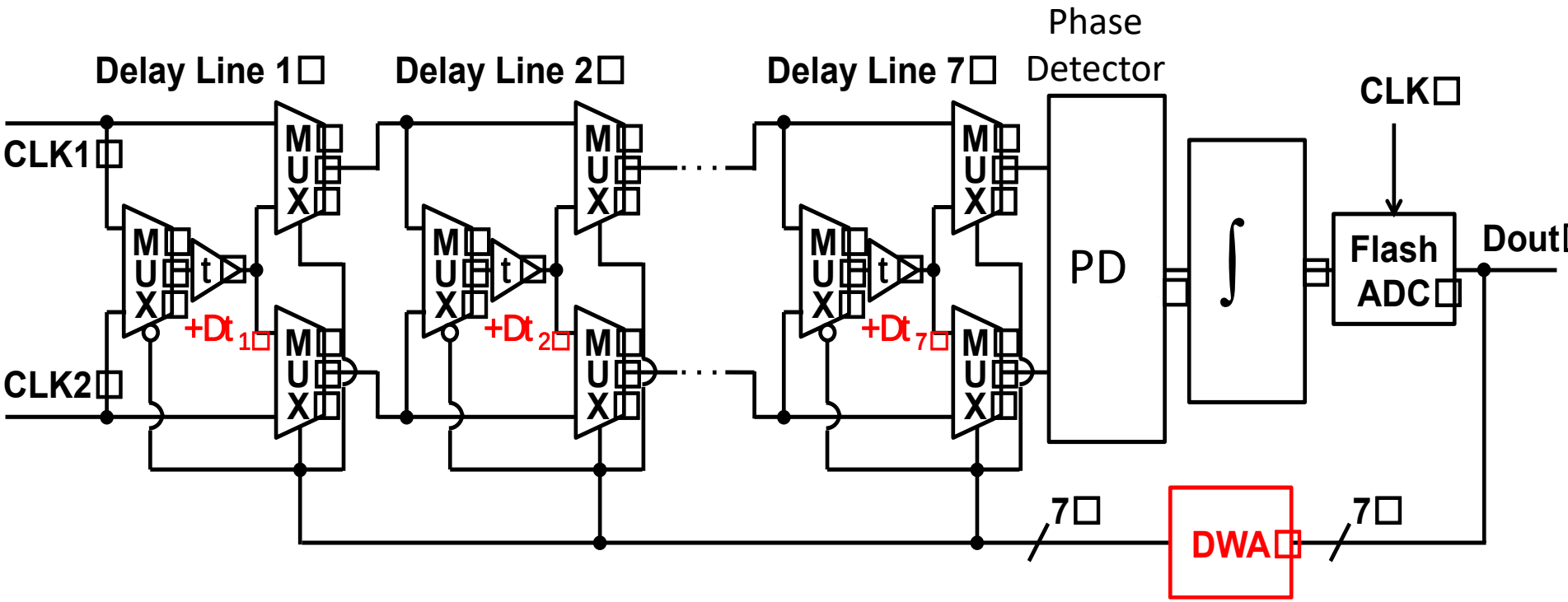
⇕

Shorter measurement time with a given time resolution

- TDC non-linearity due to mismatches among delay cells.

Multi-bit ΔΣ TDC with DWA

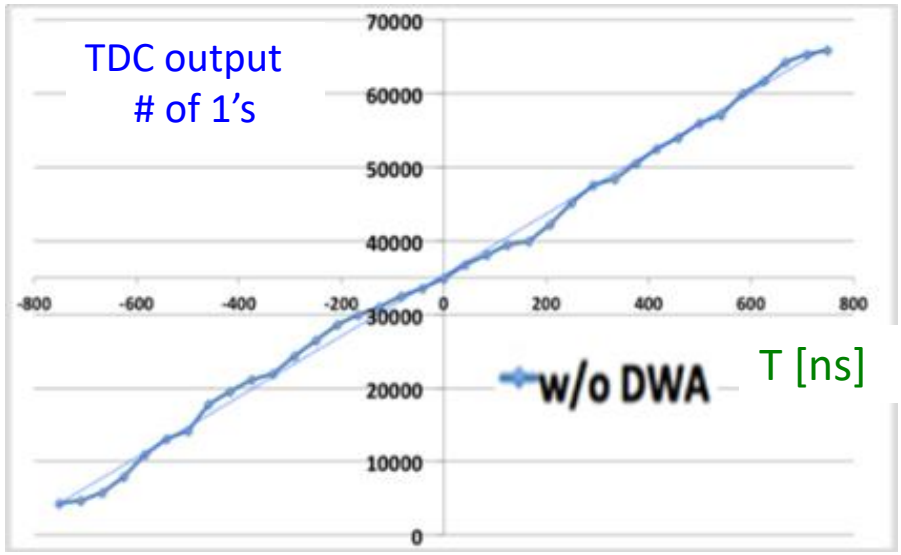
For short measurement time:

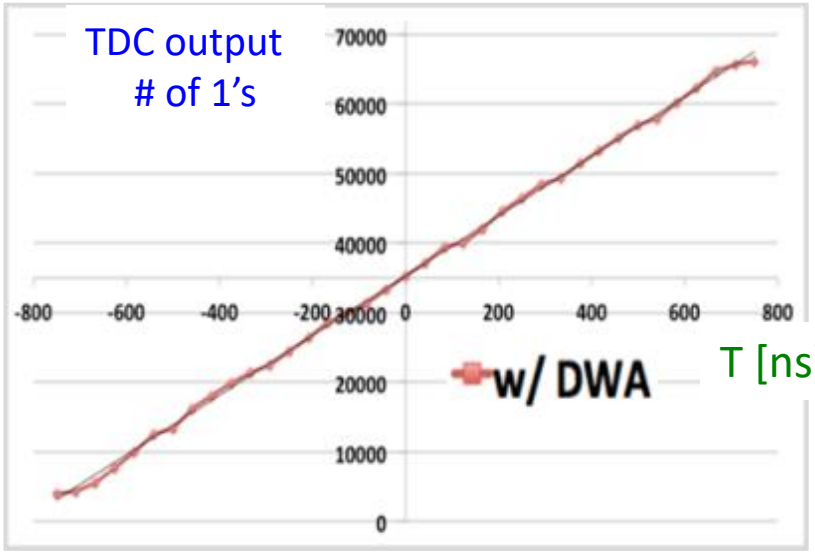


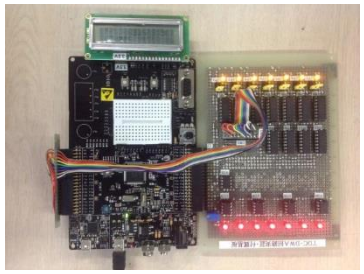
DWA: Data Weighted Averaging

DSP algorithm of compensation for mismatches among delays.

Measured Result

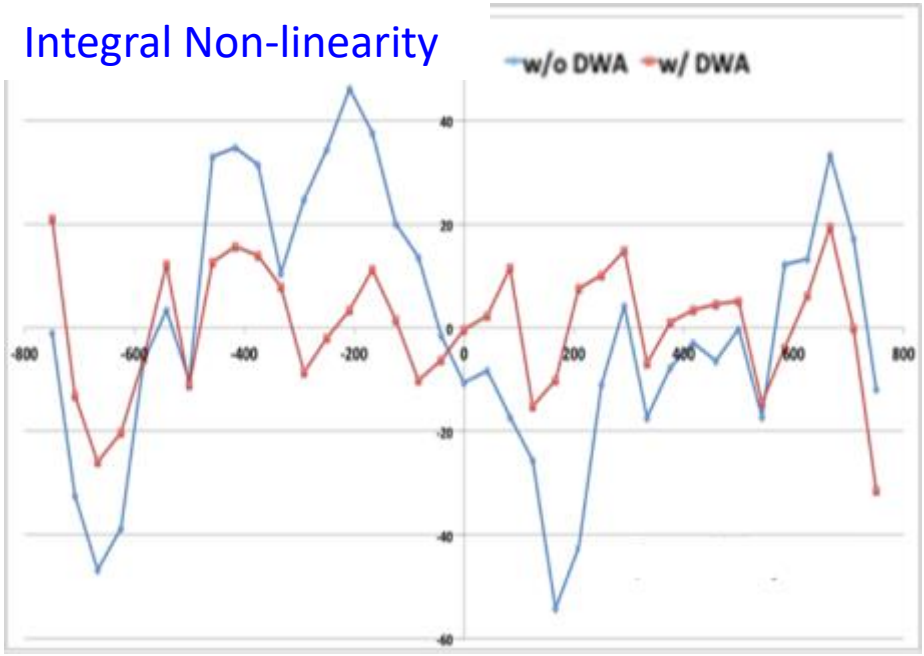






Analog FPGA Implementation

Integral Non-linearity



10,000 TDC output data are measured.

Contents

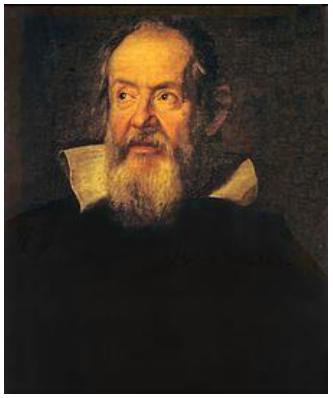
Conclusion

- Spectrum shaping of errors is possible
  with DWA algorithms.
  Their hardware implementation is simple.
- So far, DWA algorithm derivation is based on
  mathematical intuition of the researcher
  as well as simulation.

  There are no systematic or theoretical methods.
- There are still possibilities of new DWA algorithms.

Final Statement

Mathematics is the alphabet
with which God has written the Universe.



Galileo Galilei

Mathematics is the alphabet
with which the circuit designer writes his/her new idea.

Kobayashi Laboratory

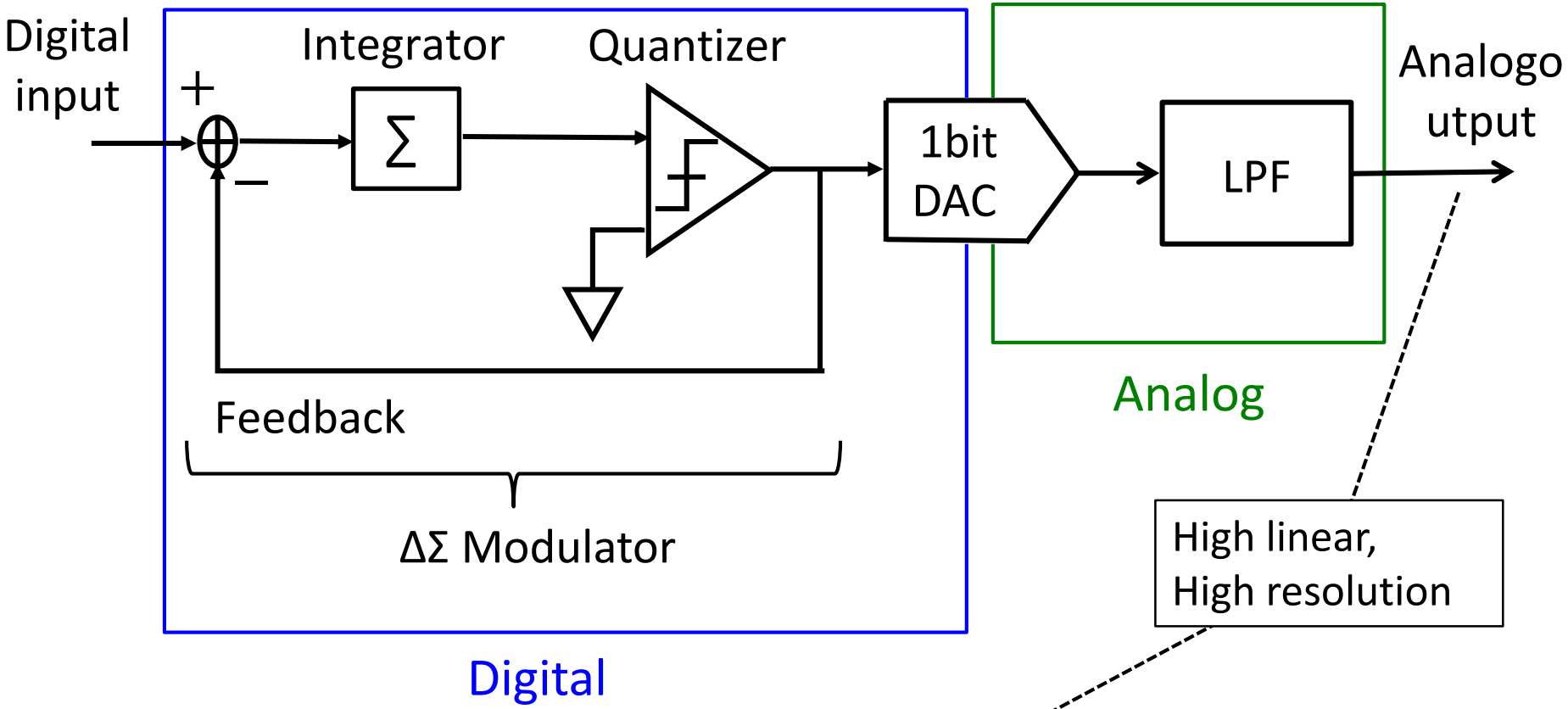
Contents

- Research Objective
- What is DWA ?
- LP, HP DWA
- Multi-Band DWA
- Multi-Band Complex DWA
- Second-Order DWA
- Application to Multi-bit ΔΣ TDC
- **Digital Dither for ΔΣ DAC**
- Conclusion

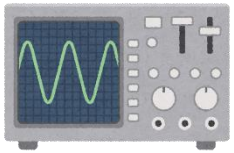
[1] J. Kojima, H. Kobayashi, et. al., “Limit Cycle Suppression Technique Using Digital Dither in Delta Sigma DA Modulator”, IEEE ICSICT (Nov. 2016).

[2] J. Wei, H. Kobayashi, et. al., “Limit Cycle Suppression Technique Using Random Signal in Delta-Sigma DA Modulator”, IEEE ICSICT (Nov. 2018).

ΔΣ DA Converter

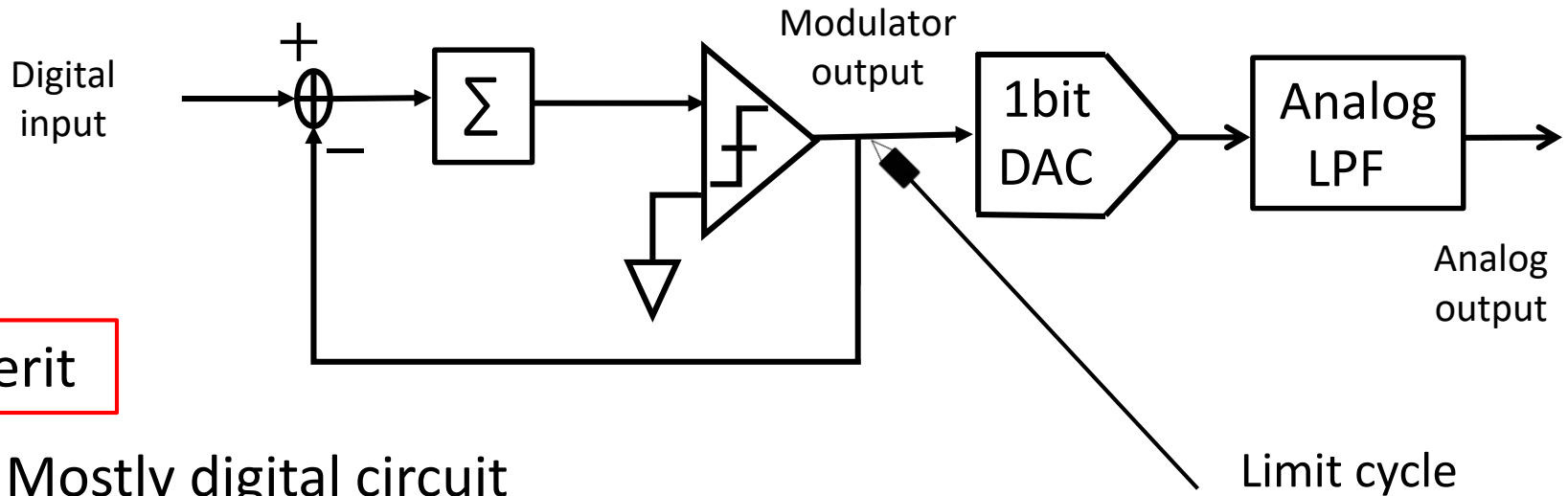


＜Usage＞



- Measurement
- Audio

Merits & Demerits of ΔΣ DAC



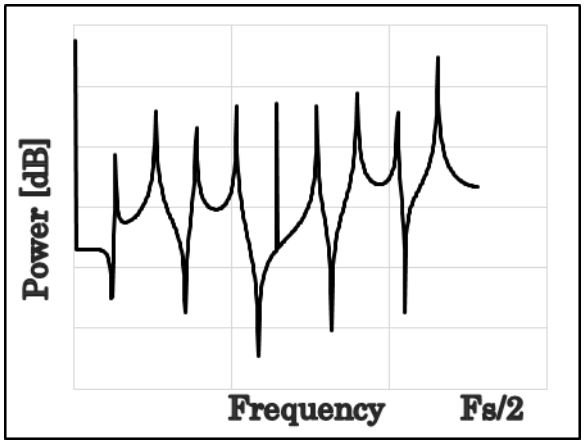
Merit

- Mostly digital circuit
- High linear & high resolution
  for low frequency signal generation

Demerit

- Limit cycle problem for small input

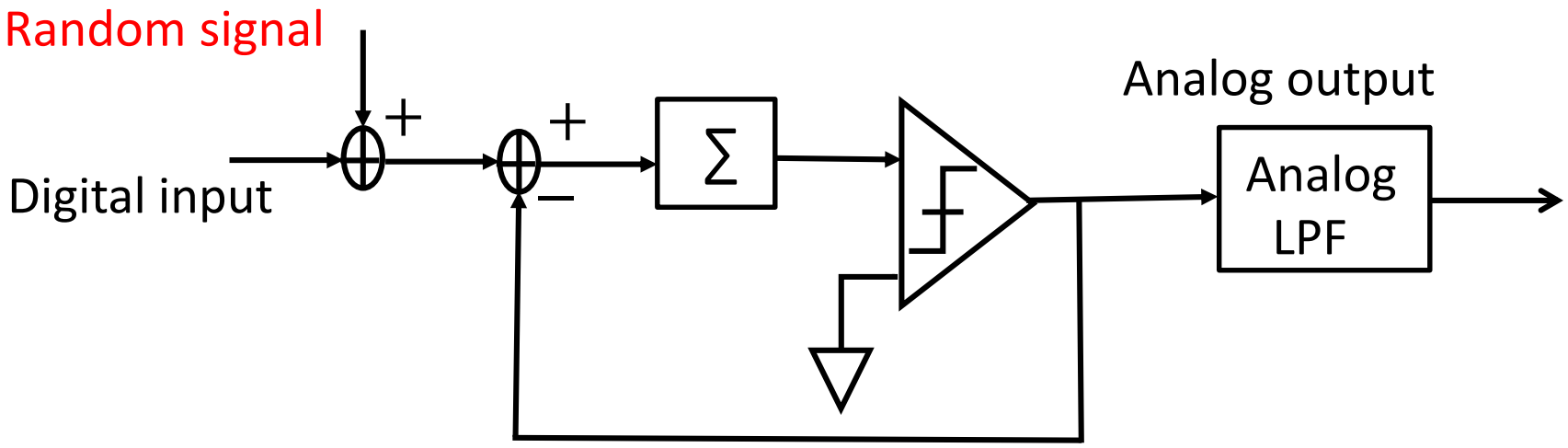
Limit cycle



※ Due to modulator nonlinearity by quantizer

Adding Dither at Input

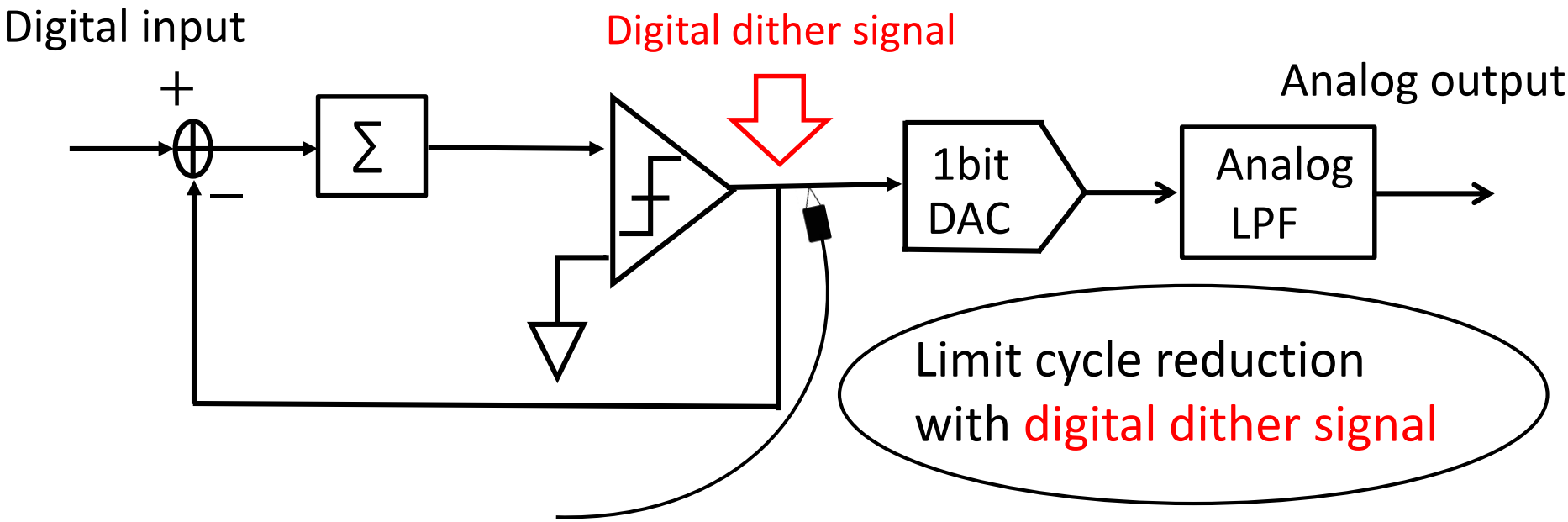
Adding random signal to digital input

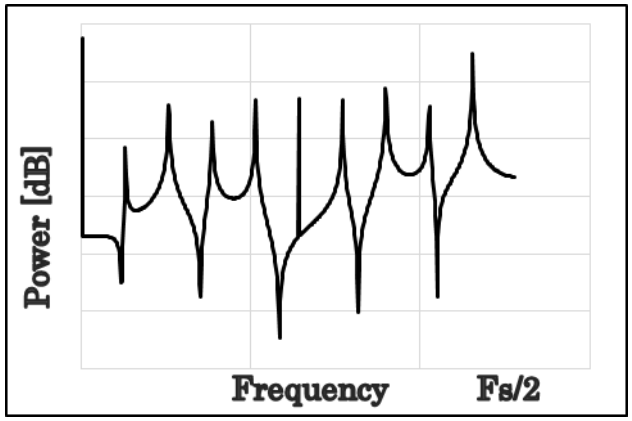


Drawbacks

- Input range sacrifice
- Random signal has to be out of signal band
  ⇒ difficult to generate

Our Approach



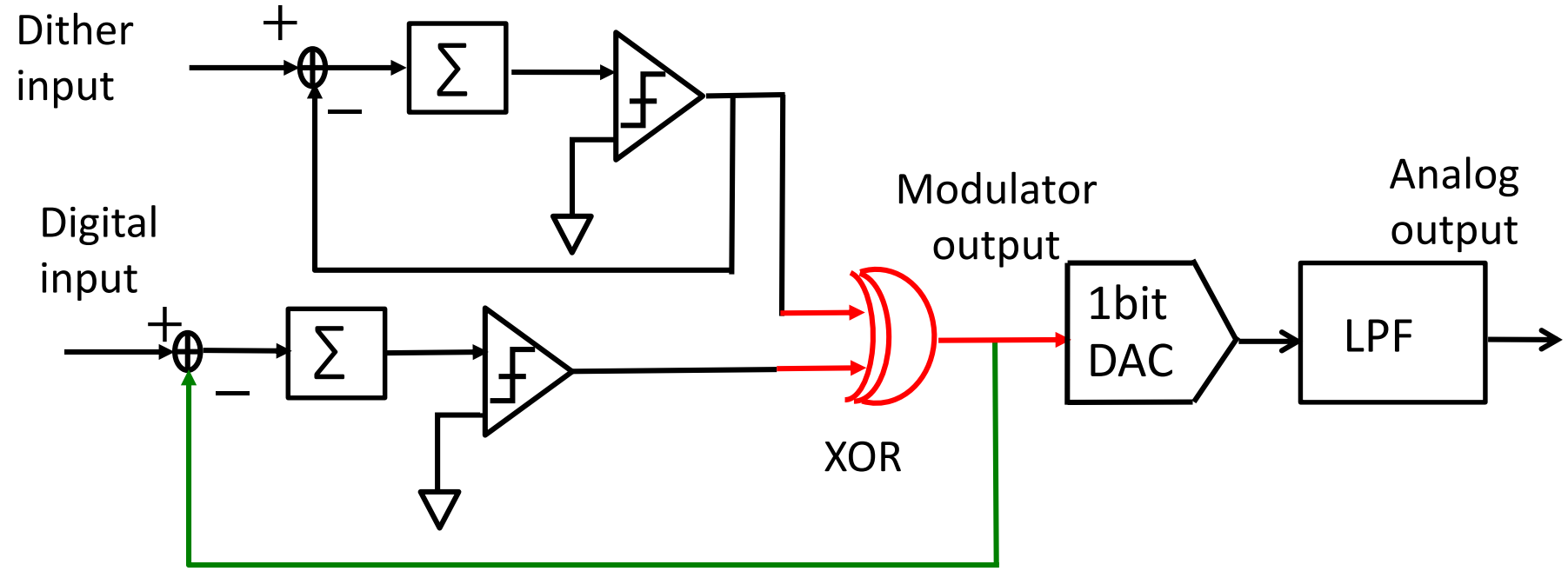


Limit cycle

Stair

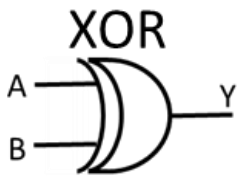
Smooth !

Proposed Circuit



< Features >

① 1-bit output



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

② Digital dither

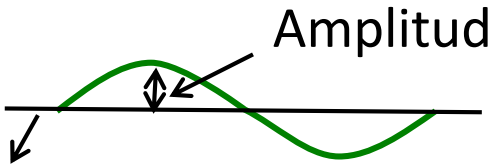
➡ NOT affect output signal, thanks to feedback

Digital signal “1” reverses comparator output with XOR

10-bit case

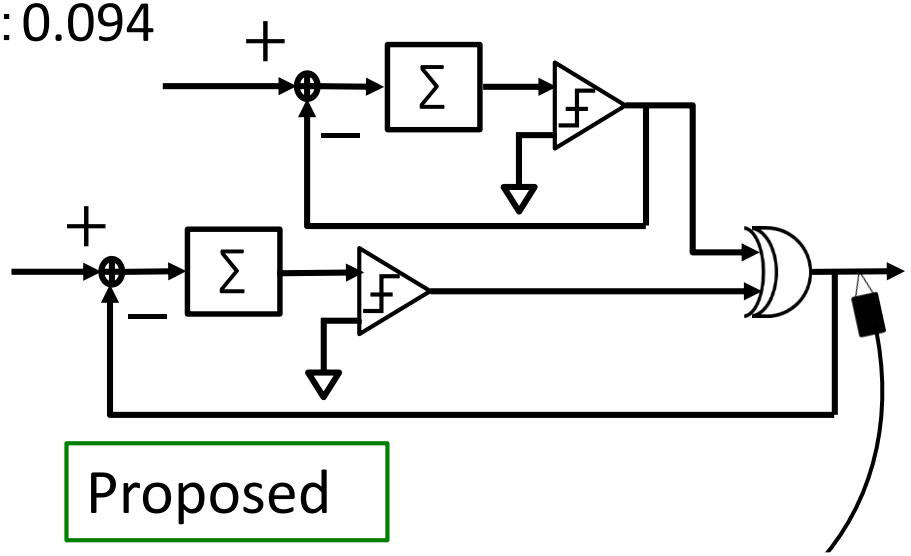
Simulation Results

Sine wave

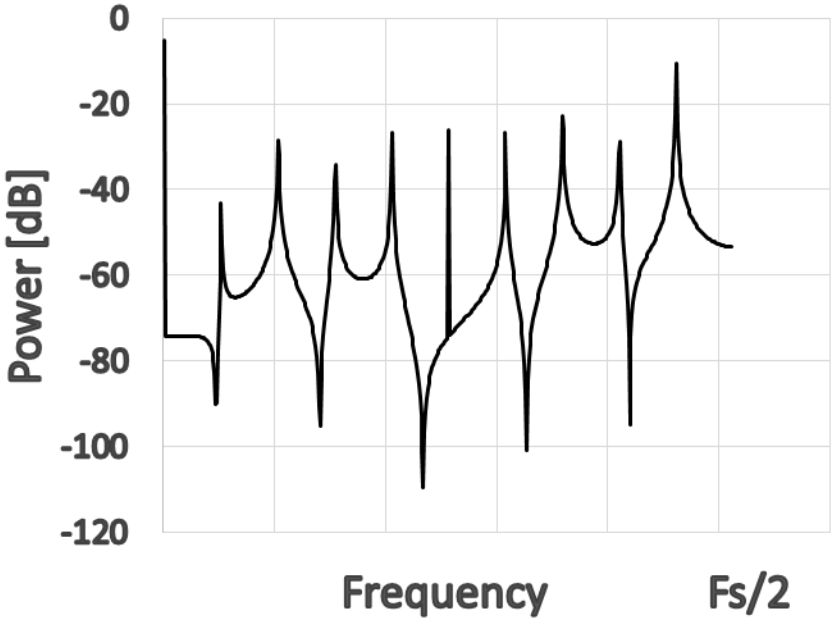


Center value : -0.520

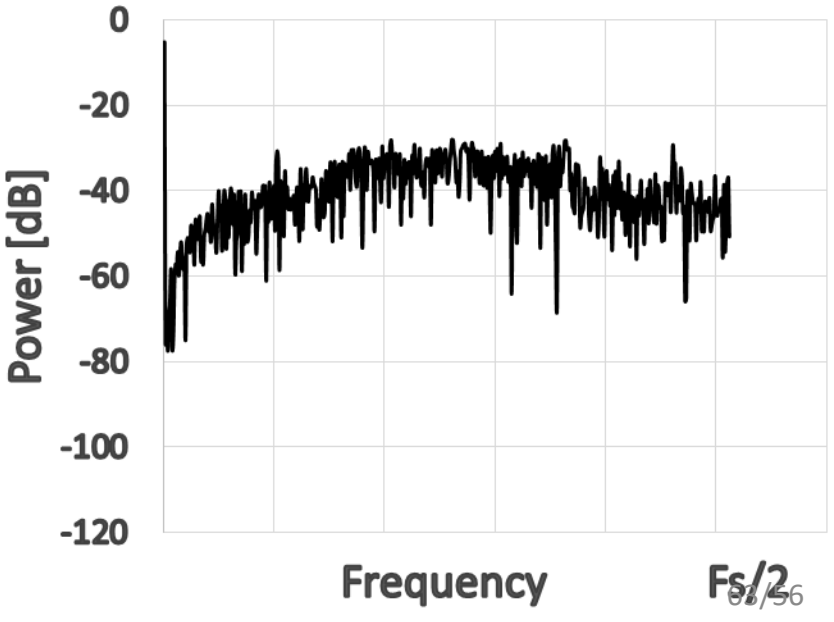
DC = 0.1



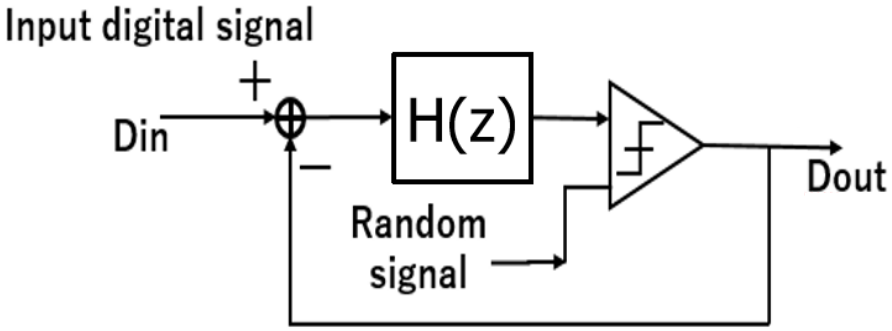
Conventional



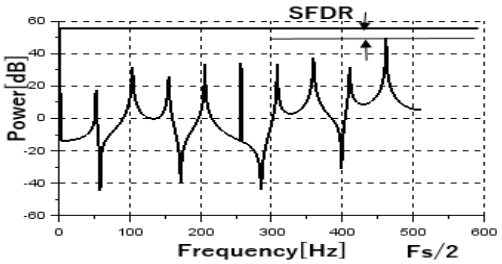
Proposed



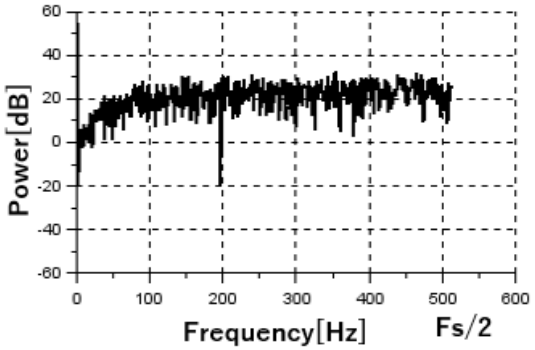
Another Configuration



LP modulator

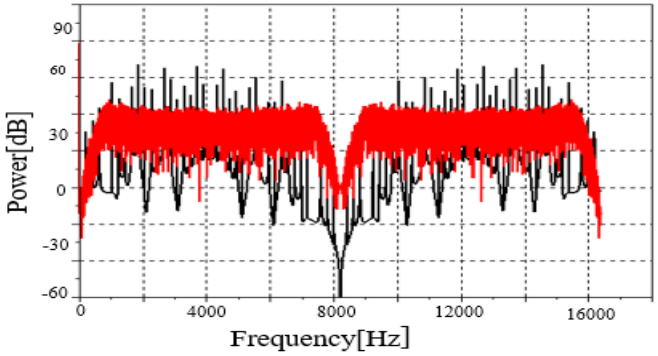


w/o dither



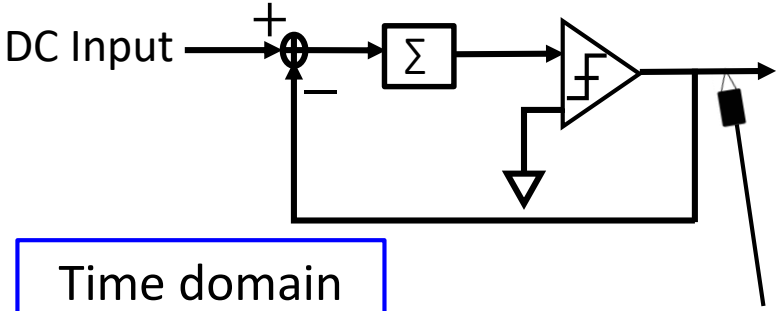
w/ dither

BP modulator



Modulator Operation

- Without dither

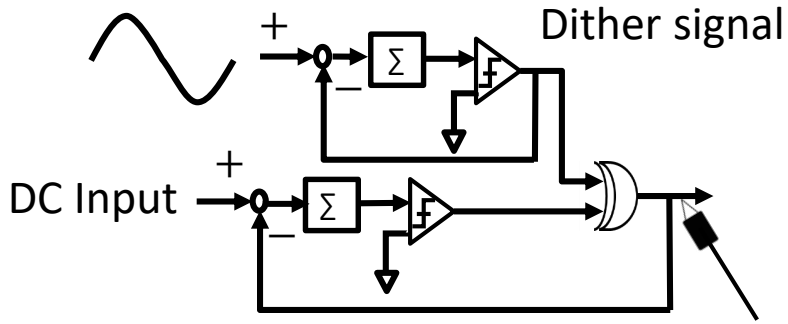


Time domain

1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0

Period

- With dither



1 0 0 0 0 1 0 1 0 0 0 0 0 1 0 0

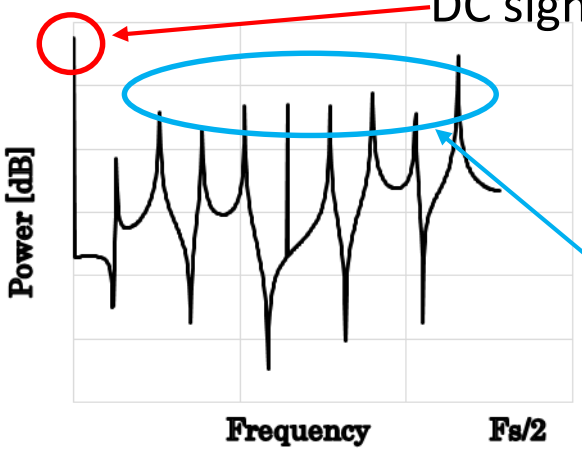
Not Periodic

✓ Orders of '0' and '1' -> different

✓ Total numbers of 1's -> the same

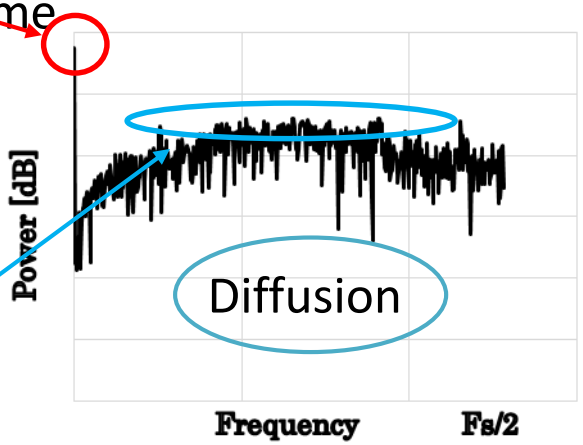
Frequency domain

DC signal power -> the same



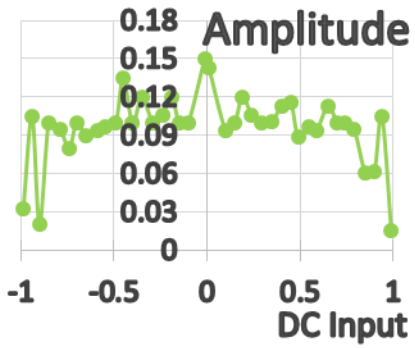
Linear

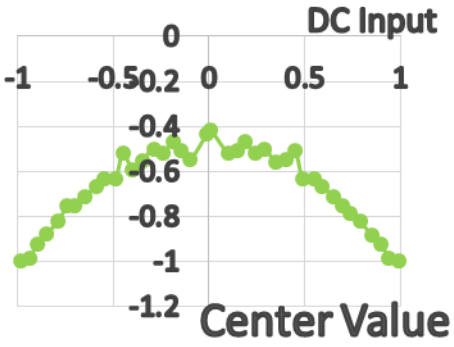
Noise

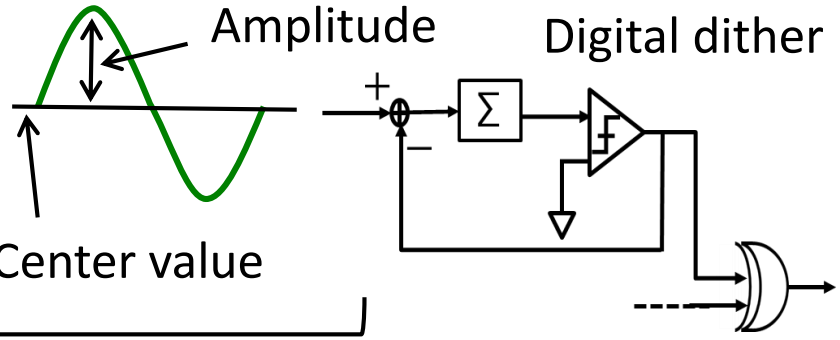


10-bit case

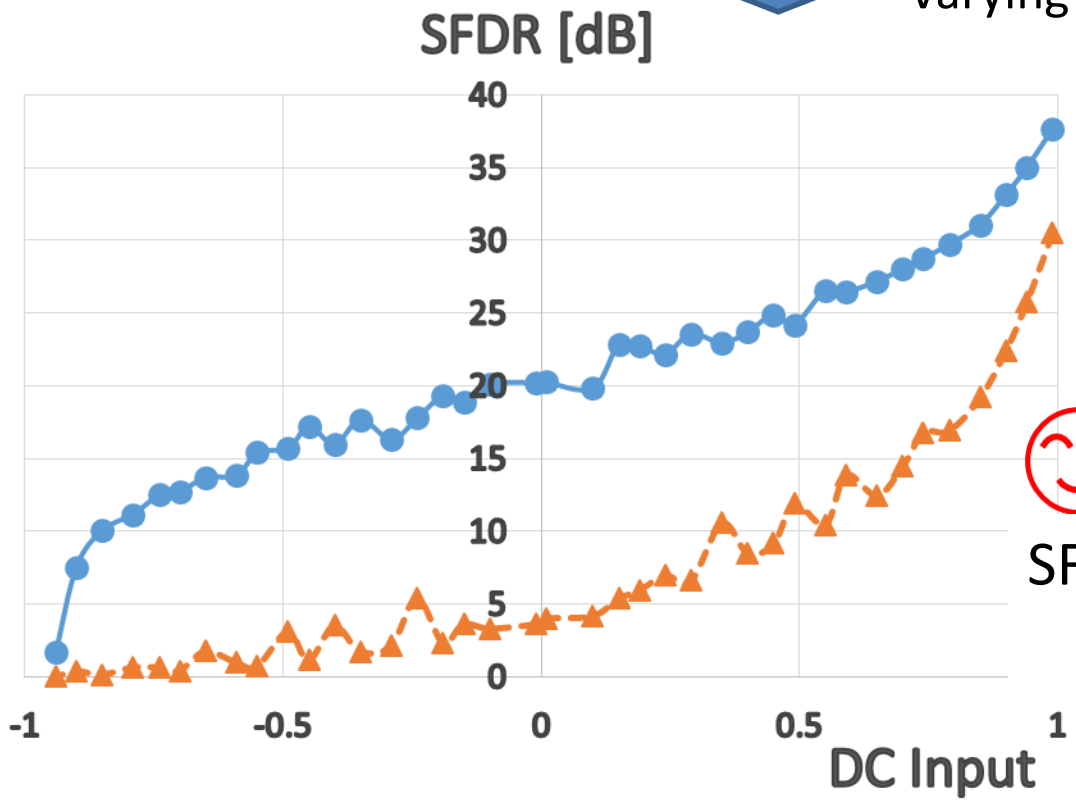
SFDR Comparison







Varying DC input



With dither
Without dither

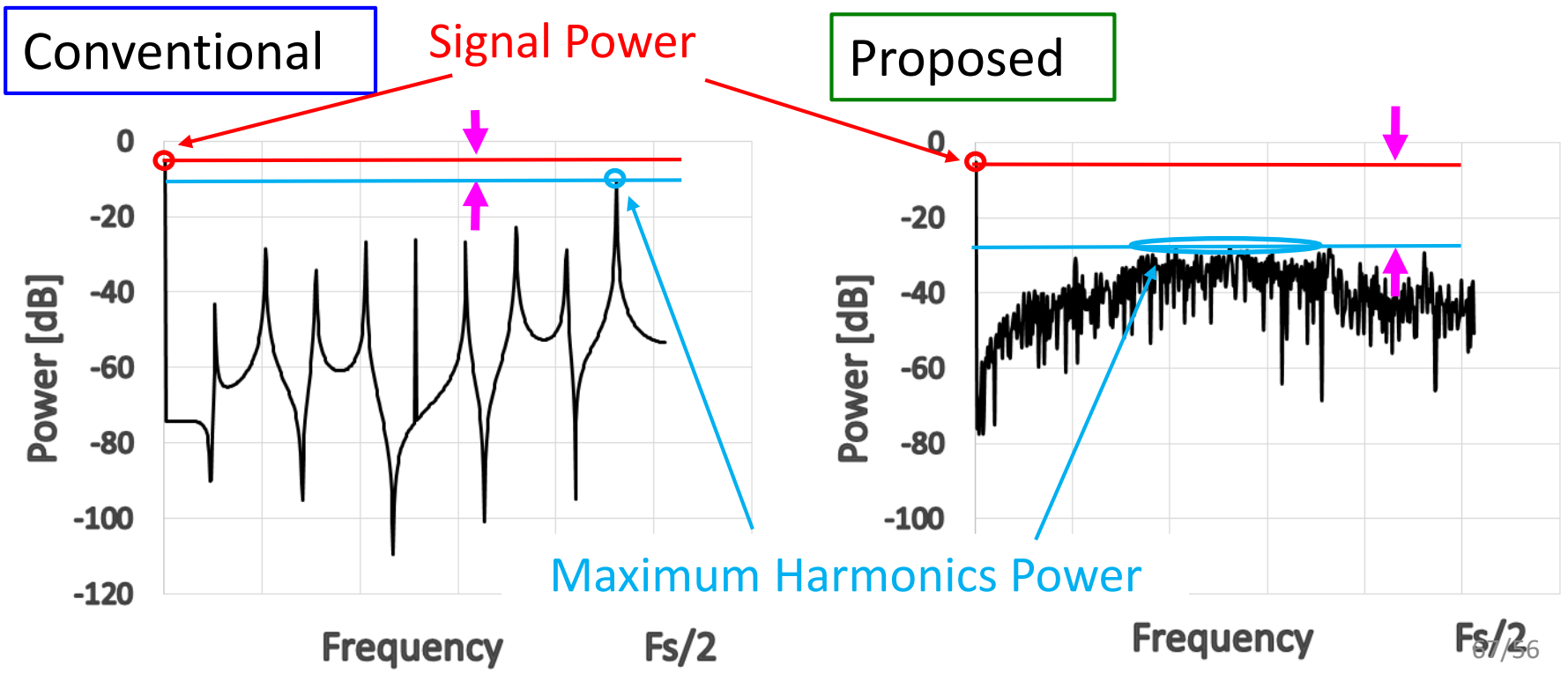
SFDR improvement
by more than 10dB

10-bit case
DC = 0.1

SFDR (Spurious Free Dynamic Range)

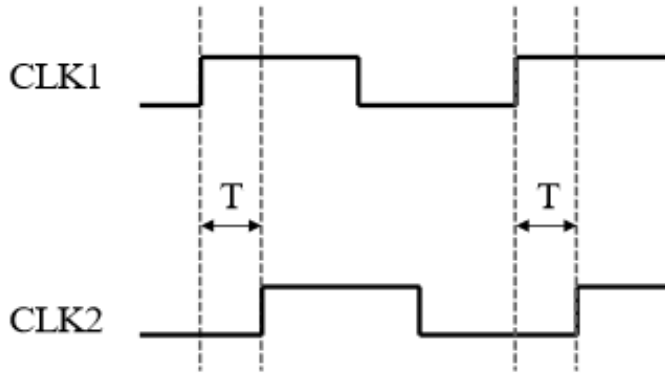
$$\text{SFDR} = \frac{\text{Signal Power}}{\text{Maximum Harmonics Power}}$$

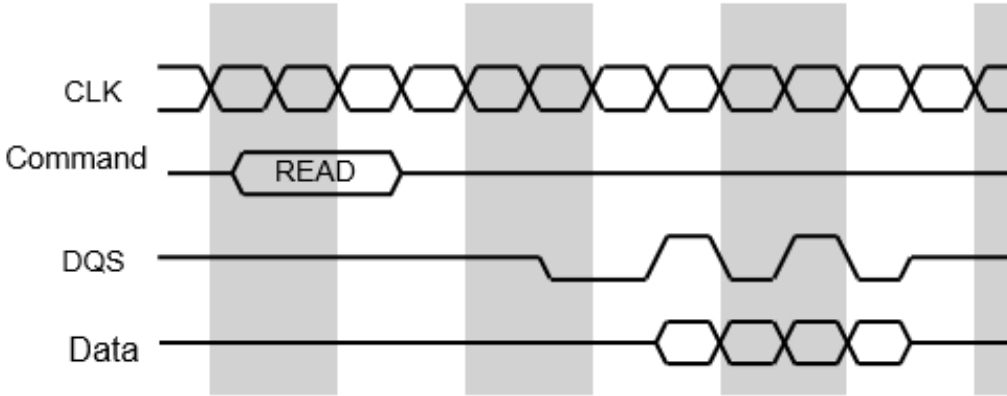
SFDR = 5.4 dB ＜ 22.9 dB



Research Objective

- Testing the timing between two repetitive digital signals
  - Ex. Data and clock in Double Data Rate memory



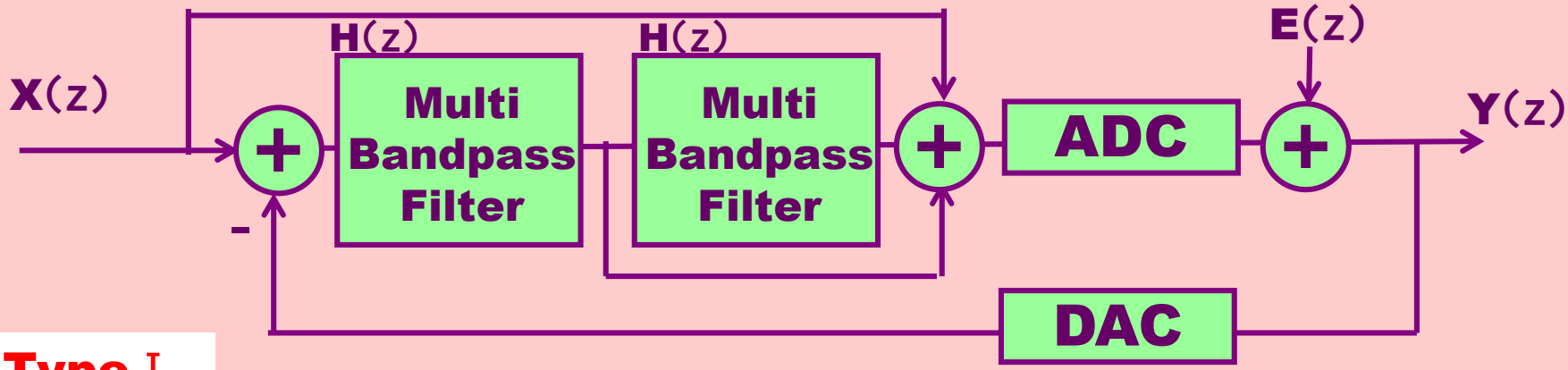


- Short testing time
- Good accuracy

Implement BOST with small circuitry

BOST: Built-Out Self-Test

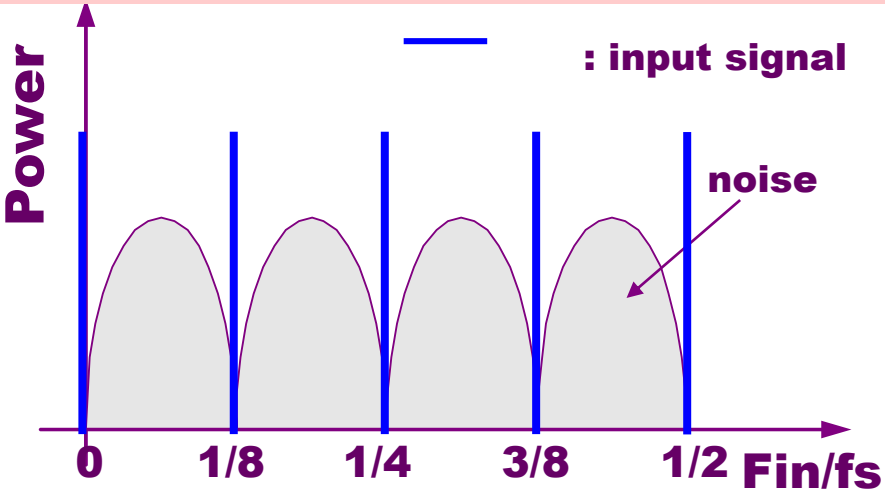
Type Ⅰ N=8
Multi-BP ΔΣ AD Modulator



Type Ⅰ

H(z)

$$\frac{Z^{-8}}{1-Z^{-8}}$$



$$STF = Z^{-8}$$

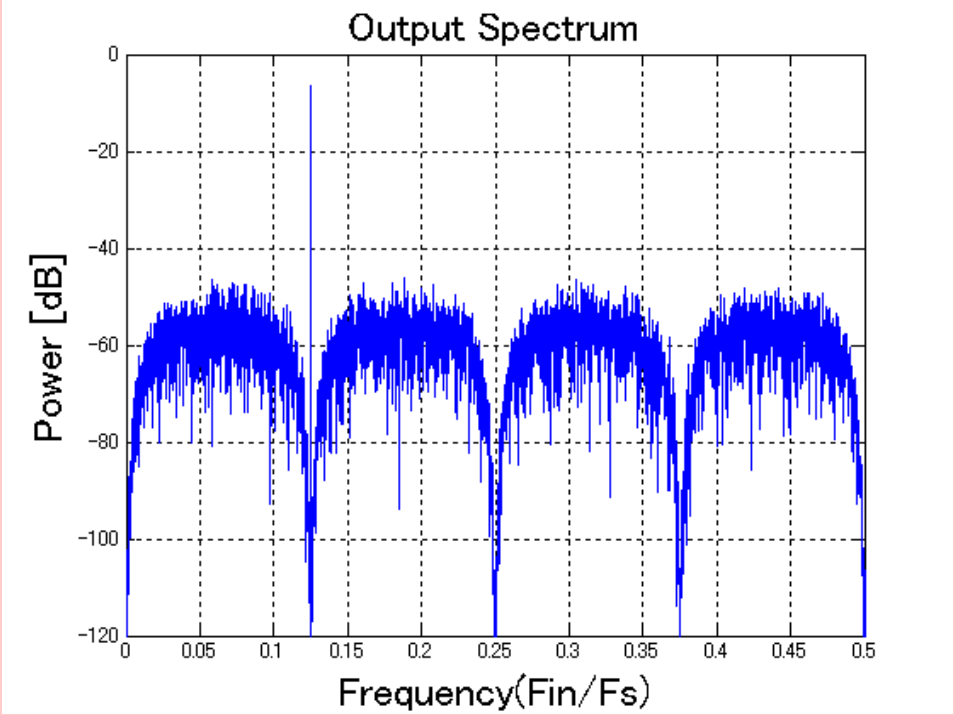
$$NTF = (1-Z^{-8})^2$$

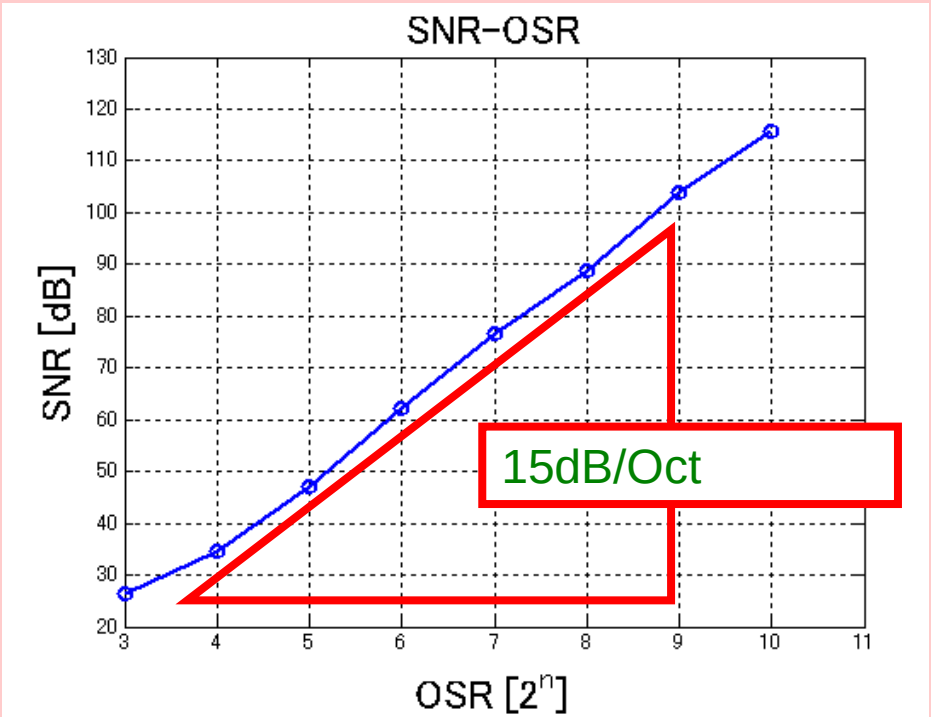
Signal Bands :

0, 1/8, 1/4, 3/8,1/2

x Fs

Type Ⅰ N=8
Multi-BP ⊿∑ AD Modulator
Simulation Results





Modulator operation is confirmed.

Our Work

Focus on Multi-bit ΔΣ Time-to-Digital Converter (TDC)

- Repetitive digital signals
  - ⇒ ΣΔ TDC can be used
- Simple circuit
- Fine time resolution
- Testing time
  - Single-bit ΣΔ TDC Long
  - Multi-bit ΣΔ TDC Short
- Linearity
  - Single-bit ΣΔ TDC Good
  - Multi-bit ΣΔ TDC Bad due to delay elements mismatches

⇓

For their compensation

DWA algorithm, BOST (FPGA) verification

Conclusion

- Spectrum shaping of errors is possible with DWA algorithms.
  Their hardware implementation is simple.
- The algorithm derivation is based on mathematical intuition of the researcher as well as simulation.

  There are no systematic or theoretical methods.
- There are till possibilities of new algorithm.
- Dither adding at the comparator is effective.