Performance Improvement of Delta-Sigma ADC/DAC/TDC Using Digital Technique

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Contents

- Objective of This Paper
- What is DWA?
- LP, HP DWA
- Multi-Bandpass DWA
- Multi-Bandpass Complex DWA
- Second-Order DWA
- Application to Multi-bit ΔΣ TDC
- Conclusion
## Contents

- **Objective of This Paper**
  - What is DWA?
  - LP, HP DWA
  - Multi-Bandpass DWA
  - Multi-Bandpass Complex DWA
  - Second-Order DWA
  - Application to Multi-bit ΔΣ TDC
  - Conclusion
Objective of This Paper

- Review the research results of authors’ group in the area of DWA: Data Weighted Averaging.

ADC/ DAC performance improvement with simple digital techniques

- Consider their application to TDC

- Consider to unify the DWA algorithms and establish their design methodology.
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Calibration Techniques Classification

ADC/DAC/TDC digital calibration techniques prevail in nano-CMOS era.

● Error Correction
  - No measurement of errors
  - Redundancy usage

● Self-Calibration
  - Error measurement
  - Compensation
  - Reference
    Voltage
    Current
    Time (frequency)
    Linearity
DWA Techniques

- Error Correction
  - No measurement of errors
  - Redundancy usage
    Time averaging of errors
    Spectrum shaping of errors

DWA: Data Weighted Averaging
DEM: Dynamic Element Matching

Diagram:
- W/O DWA
- LP DWA
- BP DWA
- HP DWA
Segment DAC with Redundancy

Digital input = 4

Multiple realization configurations
Unit Cell Mismatches

Current mismatches $e_{15}, e_{14}, \ldots, e_1$
spectrum shaping by cell selection order

DWA algorithm

No measurement of $e_{15}, e_{14}, \ldots, e_1$

\[ I_{out1} = 4I + [e_4 + e_3 + e_2 + e_1] \]

\[ I_{out2} = 4I + [e_8 + e_7 + e_6 + e_5] \]

\[ I_{out3} = 4I + [e_{14} + e_{13} + e_{12} + e_{11}] \]
$V_{out}(z) = V_{in}(z) + (1 - z^{-1}) \cdot \delta(z)$

DAC nonlinearity $\delta(z)$ is first-order noise-shaped.
This configuration can NOT be implemented!
Equivalent Operation Using DWA to $\Delta\Sigma$ Modulation

“Infinite” is equivalently realized with wrap-around
DWA Operation is a fun!

Passing a baton in relay race!
Contents

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● **LP, HP DWA**
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● Conclusion

**LP:** Low Pass
**HP:** High Pass
LP ΔΣAD Modulator

\[ Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}E(z) \]

Analog input \( X(z) \)

Filter

Quantization noise \( E(z) \)

ADC

Digital output \( Y(z) \)

DAC

Output power spectrum

Signal band

\( \Delta \Sigma \) ADC noise
Varieties of ΔΣAD Modulators

[Diagram of three different types of ΔΣAD modulators: LP, HP, BP, each with a power spectrum diagram showing power vs. frequency (Fs/2)].
Multi-bit DAC Nonlinearity

\[ Y(z) = \frac{H(z)}{1 + H(z)} \{X(z) - \delta(z)\} + \frac{1}{1 + H(z)} E(z) \]

\( \delta(z) \) is NOT noise-shaped
Why Multi-bit ADC/DAC inside ΔΣ AD Modulator?

- High slew-rate of opamp
  - Large power

- Low slew-rate of opamp
  - Small power
  - Problem:
    - Multi-bit DAC nonlinearity
Unit Cell Mismatches

Segment DAC

Current Cell Mismatch
\((e_0, e_2, e_3, \cdots, e_7)\)

\(\rightarrow\) DAC nonlinearity

Errors of specific current cells are accumulated
Equivalent LP DWA Algorithm

- Signal $\rightarrow$ Integration x Differentiation $\rightarrow$ Flat
- DAC Nonlinearity $\rightarrow$ Differentiation (High Pass)

DAC nonlinearity effects at DAC output
LP DWA Algorithm Realization

DAC nonlinearity $\delta(z)$

Digital integration

Analog differentiation

$H(z)=1/(1-Z^{-1})$

Current Cell

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</table>
Let’s Consider HP DWA Algorithm

- Signal $\rightarrow$ Differentiation $\times$ Integration $\Rightarrow$ Flat
- DAC Nonlinearity $\rightarrow$ Integration (Low Pass)

![Diagram showing digital differentiation and analog integration with DAC nonlinearity effects at DAC output graph]
HP DWA Algorithm Realization

\[ H(z) = \frac{1}{1 + Z^{-1}} \]

DAC nonlinearity \( \delta(z) \)

Digital differentiation

Analog integration

Current Cell

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Input Data

Back and forth
Contents

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Multi-Bandpass DWA

**Type I DWA**
- N pointers
- N-channel interleave of LP DWA algorithm

**Type II DWA**
- N pointers
- N-channel interleave of HP DWA algorithm

DAC nonlinearity shaping
Type I

LP ⇒ Multi-BP

LP Algorithm

Multi-BP Algorithm (LPF)

N=4

LP Pointer

LP Pointer

LP Pointer

LP Pointer

H(z) = \frac{1}{1-Z^{-1}}

Current Cell

Time

Digital Input

0 1 2 3 4 5 6 7

4

2

6

5

5

3

7

H(z) = \frac{1}{1-Z^{-4}}

Current Cell

Time

Digital Input

0 1 2 3 4 5 6 7

4

2

6

5

5

3

7

26/56
Type II

HP ⇒ BP ⇒ Multi-BP

HP Algorithm

BP Algorithm

Multi-BP Algorithm

N=4

N=2

H(z)=1/(1+Z^{-1})

H(z)=1/(1+Z^{-2})

H(z)=1/(1+Z^{-4})

HP Pointer

BP Pointer

Multi-BP Pointer

Input data

Current cell

Time

Back and forth

0 1 2 3 4 5 6 7

4 2 6 5 5 3 6 7

0 1 2 3 4 5 6 7

4 2 6 5 5 3 6 7

0 1 2 3 4 5 6 7

4 2 6 5 5 3 6 7

0 1 2 3 4 5 6 7

4 2 6 5 5 3 6 7
Multi-BP Type Ⅱ \( N=4 \)

\[
\begin{align*}
\text{STF} &= -Z^{-4} \\
\text{NTF} &= (1+Z^{-4})^2 \\
\text{Signal Bands} &= 1/8, 3/8 \\
& \quad \times Fs
\end{align*}
\]
Multi-BP Type II N=4
Simulation Results

Multi-BP DWA algorithm is effective
Contents

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Necessity of I,Q signal
RF analog front-end of Receiver IC

Need testing!
Necessity of Multi-Tone Signal

Linearity testing of

- Mixer
- Up/Down converter
- Radio communication system, etc.

Need!

Noise Power Ratio (NPR)

Distortion by DUT
2nd-order Complex Multi-BP ΔΣ DAC

Output spectrum

Output spectrum

Single-band

Multi-band

$N = 1$

$N = 4$
Principle of Complex BP Noise Shape

Signal Transfer Function = 1

\[ I_{out} + jQ_{out} = 1 \left( I_{in} + jQ_{in} \right) \]

Noise Transfer Function = 0

\[ 0 \left( E_I + jE_Q \right) \]
Complex Resonator

Output spectrum

\[ \frac{\omega_{in}}{\omega_s} \]

\[ N = 1 \]

Single-band

\[ N = 4 \]

Multi-band
Complex Resonator

Asymmetric

Output spectrum

$N = 1$

Single-band

$N = 4$

Multi-band
Equivalent Circuit of Complex DWA

Complex resonator

\[ I_{\text{in}} \]

\[ Q_{\text{in}} \]

DAC input can be \( \infty \) \( \rightarrow \) Can’t be realized directly

DAC output is \( \infty \)

Complex notch filter

\[ I_{\text{out}} \]

\[ Q_{\text{out}} \]

\( \delta_I \), \( \delta_Q \) affected by only complex notch

Can’t be realized directly
Attach pointers
Exchange upper-path and lower-path every N clock

Complex DWA is realized.
Complex Multi-Bandpass DWA Algorithm

\(N = 4\) (four zero points)

<table>
<thead>
<tr>
<th>I_{in}</th>
<th>Q_{in}</th>
<th>I_0</th>
<th>I_1</th>
<th>I_2</th>
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DAC_1 (LP operation)

DAC_2 (HP operation)
Simulation Result  ~Ideal Linear DAC~
Simulation Result ~Actual Non-Linear DAC~

Notches filled with noise
Simulation Result

~Actual Non-Linear DAC + DWA~

- Notches filled with noise
Simulation Result

~Actual Non-Linear DAC + DWA~

Digital input

\[ \delta_I \]

\[ \delta_Q \]

Complex Bandpass ΔΣ Modulator

DAC

DWA

DAC

Complex Bandpass Filter

Analog output

\[ \text{SNDR [dB]} \]

\[ \text{OSR} (2^n) \]

Notches filled with noise

\[ \text{Steep Notches} \]

DWA

\[ \text{Complex DWA} \]
<table>
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<th></th>
<th>Research Objective</th>
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2\textsuperscript{nd}-order DWA

\[ Y(z) = X(z) + (1 - z^{-1})^2 \delta(z) \]

- 2\textsuperscript{nd}-order DWA is more effective
- But its circuit/operation become complicated
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**ΔΣ TDC Features**

Timing $T$ measurement between CLK1 and CLK2

ΔΣ Time-to-Digital Converter (TDC)

- Simple circuit
- High linearity
- Measurement time $\rightarrow$ longer $\Rightarrow$ time resolution $\rightarrow$ finer

$T \propto \# \text{ of 1's at Dout}$
Principle of $\Delta\Sigma$TDC

CLK1 $\rightarrow$ $\Delta\Sigma$TDC delay: $\tau$ $\rightarrow$ Dout 0 or 1
CLK2 $\rightarrow$

$\Delta T$ $\rightarrow$ CLK1 CLK2

Dout # of 1’s is proportional to $\Delta T$

short $\uparrow$ few $\uparrow$
long $\downarrow$ many

Dout

$\begin{array}{cccccccccccc}
0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\
\end{array}$

$\begin{array}{cccccccccccc}
0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \\
\end{array}$

$\begin{array}{cccccccccccc}
0 & 1 & 1 & 1 & 1 & 1 & 0 & 1 & 1 & 1 & 1 & 1 \\
\end{array}$
ΔΣTDC Configuration

Multi-Bit ΔΣ TDC

- 3-bit: 7 comparators and delays
- Fine time resolution with a given measurement time

Shorter measurement time with a given time resolution

- TDC non-linearity due to mismatches among delay cells.
Multi-bit ΔΣ TDC with DWA

For short measurement time:

DWA: Data Weighted Averaging

DSP algorithm of compensation for mismatches among delays.
Measured Result

Analog FPGA Implementation

Integral Non-linearity

10,000 TDC output data are measured.

TDC output

# of 1’s

T [ns]

TDC output

# of 1’s

T [ns]
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Conclusion

- Spectrum shaping of errors is possible with DWA algorithms. Their hardware implementation is simple.

- So far, DWA algorithm derivation is based on mathematical intuition of the researcher as well as simulation. There are no systematic or theoretical methods.

- There are still possibilities of new DWA algorithms.
Mathematics is the alphabet with which God has written the Universe.

Galileo Galilei

Mathematics is the alphabet with which the circuit designer writes his/her new idea.
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- Digital Dither for ΔΣ DAC
- Conclusion


ΔΣ DA Converter

Digital input → Integrator → Quantizer → 1bit DAC → LPF → Analogo output

Feedback

ΔΣ Modulator

Digital

<Usage>
- Measurement
- Audio

High linear, High resolution
Merits & Demerits of $\Delta\Sigma$ DAC

**Merit**
- Mostly digital circuit
- High linear & high resolution for low frequency signal generation

**Demerit**
- Limit cycle problem for small input

※ Due to modulator nonlinearity by quantizer
Adding Dither at Input

Adding random signal to digital input

Drawbacks

- Input range sacrifice
- Random signal has to be out of signal band difficult to generate
Our Approach

Limit cycle reduction with digital dither signal

Digital input

Digital dither signal

Analog output

1bit DAC

Analog LPF

Limit cycle

Stair

Smooth!
Proposed Circuit

Features:

1. 1-bit output

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<th>B</th>
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2. Digital dither
   - NOT affect output signal, thanks to feedback
   - Digital signal “1” reverses comparator output with XOR
10-bit case

Simulation Results

Sine wave

Center value: -0.520

DC = 0.1

Amplitude: 0.094

Conventional

Proposed

Power [dB]

Frequency

Fs/2

Power [dB]

Frequency

Fs/2
Another Configuration

LP modulator

BP modulator

w/o dither

w/ dither
Modulator Operation

- **Without dither**

DC Input → + → Σ → + → Time domain

Period

1 0 0 0 1 0 0 0 1 0 0 0

- **With dither**

DC Input → + → Σ → Dither signal → Time domain

Not Periodic

Period

1 0 0 0 0 1 0 1 0 0 0 0 0 1 0 0

- **Frequency domain**

DC signal power → the same

- **Orders of ‘0’ and ‘1’** -> different

- **Total numbers of 1’s** -> the same

- **Linear**

- **Noise**

- **Diffusion**
10-bit case

SFDR Comparison

With dither
Without dither

SFDR improvement by more than 10dB
10-bit case
DC = 0.1

** SFDR (Spurious Free Dynamic Range) **

\[
SFDR = \frac{\text{Signal Power}}{\text{Maximum Harmonics Power}}
\]

\[
SFDR = 5.4 \text{ dB} < 22.9 \text{ dB}
\]
Research Objective

- Testing the timing between two repetitive digital signals
  - Ex. Data and clock in Double Data Rate memory

- Short testing time
- Good accuracy

Implement BOST with small circuitry

BOST: Built-Out Self-Test
Type I  N=8
Multi-BP $\Delta\Sigma$ AD Modulator

$$H(z) = \frac{Z^{-8}}{1-Z^{-8}}$$

**STF** = $Z^{-8}$

**NTF** = $(1-Z^{-8})^2$

Signal Bands:

0, 1/8, 1/4, 3/8, 1/2

$x\ F$s
Type I \( N = 8 \)
Multi-BP \( \triangle \Sigma \) AD Modulator
Simulation Results

Modulator operation is confirmed.
Our Work

Focus on Multi-bit $\Delta\Sigma$ Time-to-Digital Converter (TDC)

- Repetitive digital signals
  - $\Delta\Sigma$ TDC can be used
- Simple circuit
- Fine time resolution
- Testing time
  - Single-bit $\Delta\Sigma$ TDC: Long
  - Multi-bit $\Delta\Sigma$ TDC: Short
- Linearity
  - Single-bit $\Delta\Sigma$ TDC: Good
  - Multi-bit $\Delta\Sigma$ TDC: Bad due to delay elements mismatches

For their compensation

DWA algorithm, BOST (FPGA) verification
Conclusion

- Spectrum shaping of errors is possible with DWA algorithms. Their hardware implementation is simple.

- The algorithm derivation is based on mathematical intuition of the researcher as well as simulation. There are no systematic or theoretical methods.

- There are till possibilities of new algorithm.

- Dither adding at the comparator is effective.