*Proceedings of International Conference*
*Technology and Social Science 2018 (ICTSS 2018)*

# A Second-order DWA Algorithm for Multi-bit ΔΣADC/DAC

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**Keywords** multi-bit, ΔΣ modulator, 2nd-order data-weighted-averaging algorithm, dynamic element matching, noise-shaping

**Abstract -** This paper proposes a 2nd-order data-weighted averaging (DWA) algorithm for multi-bit low-pass ΔΣADC/DAC, which is one of dynamic element matching (DEM) algorithms. Oversampling and noise-shaping are used to achieve high linearity of ΔΣADC/DAC, and they are attractive as sensor interface circuits for Internet-of-Things (IoT) applications. However, when a multi-bit DAC is used inside their circuits, its nonlinearities are not noise-shaped and the overall linearity of the ΔΣADC/DAC degrades. To overcome this problem, several algorithms to noise-shape the DAC nonlinearities have been proposed; many of them perform the first-order noise-shaping. In this paper we investigate a second-order noise-shaping algorithm, which is more effective than the first-order one and easy to implement compared to conventional second-order ones, though it needs two-cycle operation which makes the circuit to be slow. Our MATLAB simulation shows the effectiveness of the algorithm, and also we show its switched capacitor circuit implementation.

## 1. Introduction

This paper presents a second-order data-weighted-averaging (DWA) algorithm for multi-bit ΔΣ analog-to-digital converters (ADCs) / digital-to-analog converters (DACs), for their linearity improvement with digital techniques. The ΔΣ ADCs/DACs are used for Internet-of-Things (Piot) applications such as sensor interface. However, their multi-bit configuration causes overall DAC non-linearity due to characteristics mismatches among multiple unit cells, even though they can be implemented with small hardware and power. [1-9] Therefore, we investigate a second-order DWA algorithm, which is more effective than the first-order one and easier to implement than the conventional second-order ones [7, 8], though its operation may be slower due to 2-clock cycle operation. We show here its algorithm, circuit design and simulation results.

## 2. Multi-bit ΔΣADC/DAC

Fig. 1 shows an equivalent block diagram of a ΔΣADC, where, H(z) is a loop filter and E(z) is a quantization noise. When an internal DAC is multi-bit, then its nonlinearity is modelled by δ(t).

$$Y(z) = \frac{H(z)}{1+H(z)}[X(z) - \delta(z)] + \frac{1}{1+H(z)}E(z) \qquad (1)$$

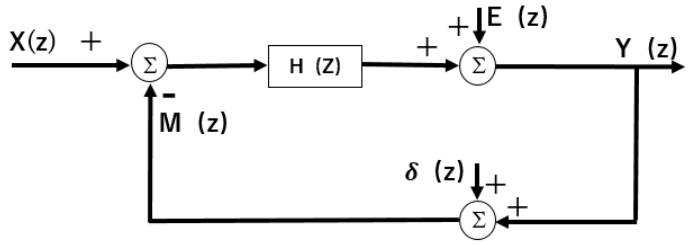


Fig.1: ΔΣAD modulator equivalent block diagram. H(z) is a loop filter, X(z) is an analog input, Y (z) is a digital output and E(z) denotes quantization noise of an internal ADC, while δ(z) indicates nonlinearity of a multi-bit internal DAC.

Let us consider a multi-bit (9-level) DAC with the switched capacitor circuit in Fig.2. There each unit capacitor value should be identical, however in reality there are manufacturing variations. Here each unit capacitor is denoted by $C_k = C + e_k$ (k = 0, 1, 2, ..., 7). Its average value is defined as

$$C := (C_0 + C_1 + C_2 + \ldots + C_7)/8.$$

Then we have

$$e_0 + e_1 + e_2 + \ldots + e_7 = 0 .$$

$e_k$ expresses error of $C_k$ from the average capacitor value C. When a digital input is *m* and the DWA algorithm is not used, then the output voltage is given by

$$V_{out} = -m\frac{C}{C_{out}}V_{ref} + \delta \qquad (2)$$

Nonlinearity δ of the DAC is expressed by

$$\delta = -\frac{e_0 + e_1 + e_2 + \ldots + e_{m-1}}{C_{out}}V_{ref} \qquad (3)$$

The DWA algorithm takes care of this problem.

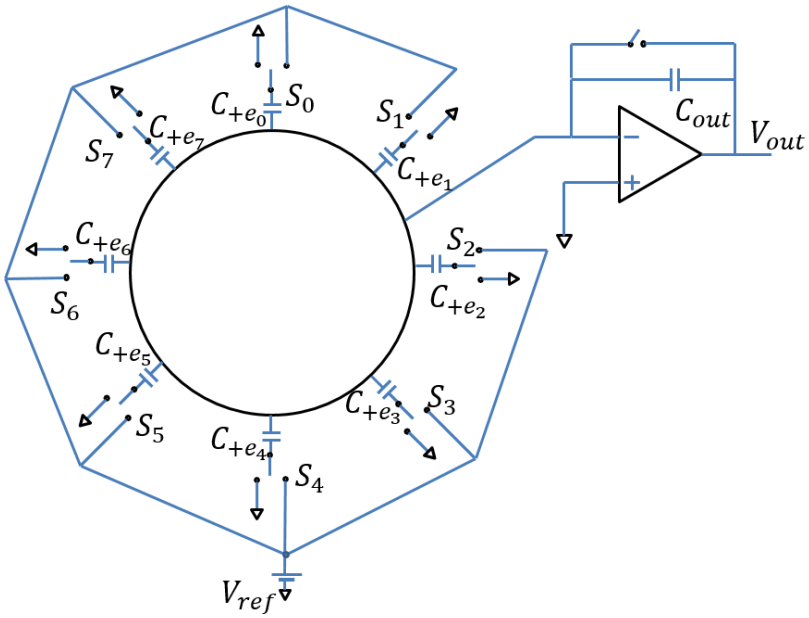


Fig 2: A segmented switched capacitor DAC with 9-level resolution in a ring form, where e0, e1, ...,e6, e7 indicate capacitor mismatches.

## 3. Proposed Second-order DWA Algorithm

### 3.1 Second-order Noise-Shaping of DAC Nonlinearity

Fig. 3 shows the basic idea of the second-order noise-shaping structure of multi-bit DAC nonlinearities. In front of a DAC, two digital integrators are added, while two analog differentiators follow the DAC.

$$Y(z) = X(z) + (1 - z^{-1})^2 \delta(z) \qquad (4)$$

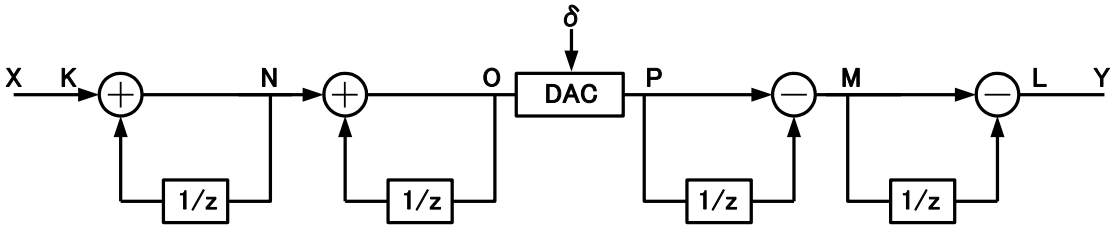


Fig 3: A second-order DWA architecture.

We see that the DAC nonlinearity δ (z) is second-order noise-shaped. However, this configuration in Fig. 3 does not work well; suppose that the digital input X is a constant value, then the DAC input O becomes large due to 2 integrators, which is out of the DAC input range. Then we consider a segmented DAC in a ring form in Fig.2.

Note that the first-order DWA algorithm has equivalently one digital integrator and one analog differentiator. [1-4]

### 3.2 Second-order DWA Algorithm

Now we explain the proposed second-order DWA algorithm equivalent to the configuration in Fig. 3. We consider that each unit cell can produce analog values of -1, 0, 1, 2 with some operations.

**A. Two pointers Po+, Po-**

Let us define as follows:

D(n): DAC input at time *n.*

$P_{0+}(n)$: plus-side pointer, $P_{0-}(n)$: minus-side pointer

$S_{+}(n)$: plus signal start, $S_{-}(n)$: minus signal start

$A_{+}(n)$: plus-side number, $A_{-}(n)$: minus-side number.

Then we have the following relationships:

**Plus side:**

$$P_{0+}(n) = mod_8\left[D(n-1) + \sum_{k=0}^{n-2} P_{0+}(k)\right] \qquad (5)$$

$$S_{0+}(n) = mod_8[P_{0+}(n) + 1] \qquad (6)$$

$$A_{0+}(n) = D(n) + mod_8[A_{+}(n-1)] \qquad (7)$$

**Minus side:**

$$P_{0-}(n) = P_{0+}(n-1) \qquad (8)$$

$$S_{-}(n) = mod_8[P_{0+}(n-1) + 1] \qquad (9)$$

$$A_{0-}(n) = mod_8[A_{+}(n-1)] \qquad (10)$$

**B. Assignment of "Positive" and "Negative" to Cell**

(i) Assign "positive : +" to the unit cells of

$$S_{0+}(n),\ mod_8(S_{0+}(n)+1), mod_8(S_{0+}(n)+2),\ \ldots\ mod_8(S_{0+}(n)+A_{0+}-1).$$

(ii) Assign " negative : -" to the unit cells of

$$S_{0-}(n), mod_8(S_{0-}(n)+1), mod_8(S_{0-}(n)+2),\ \ldots . mod_8(S_{0-}(n)+A_{0-}-1)$$

**C. Decision of Unit Cell Value: -1, 0, 1 or 2**

(i)Condition for unit cell value of -1:
"+ is k+2 times assigned" and "– is k+3 times assigned."
(ii) Condition for unit cell value of 0:
"+ is k+2 times assigned" and "– is k+2 times assigned."
(iii)Condition for unit cell value of +1:
"+ is k+2 times assigned" and "– is k+1 times assigned."
(ii) Condition for unit cell value of +2:
"+ is k+2 times assigned" and "– is k times assigned."

**D. DAC Output Without/With DWA Algorithm**

Let us consider the DAC output for D(n) = 3 in Fig.2.
Without DWA algorithm: It is always

$$V_{out} = -\frac{C_0+C_1+C_2}{C_{out}}V_{ref} = -\frac{3C}{C_{out}}V_{ref} - \frac{e_0+e_1+e_2}{C_{out}}V_{ref} \quad (11)$$

With the second-order DWA algorithm:
Case 1) "-1" is assigned to 1st unit cell. "+1" is assigned to 2nd, 3rd, 4th and 5th unit cells, and "0" is assigned to the other cells. Then the DAC output is given by

$$V_{out} = -\frac{-C_1+C_2+C_3+C_4+C_5}{C_{out}}V_{ref}$$

$$= -\frac{3C}{C_{out}}V_{ref} - \frac{-e_1+e_2+e_3+e_4+e_5}{C_{out}}V_{ref} \quad (12)$$

Case 1) "+2" is assigned to 3rd unit cell. "+1" is assigned to 4th unit cell+1. "0" is assigned to the other cells. Then the DAC output is given by

$$V_{out} = -\frac{2C_3+C_4}{C_{ref}}V_{ref} = -\frac{3C}{C_{ref}}V_{ref} - \frac{2e_3+e_4}{C_{ref}}V_{ref} \quad (13)$$

**E. Second-order DWA Algorithm Operation Example**

Let us consider the case that the DAC input changes 3, 4, 2, 5, 6, 1, … sequentially as shown in Fig.4. Then each value assigned to each unit cell changes as follows:
(i)Time 0 (D(0)=3): "+1" is assigned to $C_0,\ C_1,\ C_2$, and "0" is assigned to the other cells.
(ii)Time 1 (D(1)=4): By considering D(0)+D(1)=7, "+1" is assigned to $C_3,\ C_4,\ C_5,\ C_6,\ C_7,\ C_0,\ C_1$.
Also due to D(0)=3, "-1" is assigned to $C_0,\ C_1,\ C_2$.
Finally, since "+1", "-1" are assigned once to $C_0,\ C_1$, then "0" is assigned to $C_0,\ C_1$.
"-1" is assigned to $C_2$.
"+1" is assigned to $C_3,\ C_4,\ C_5,\ C_6,\ C_7$.
(iii)Time 2 (D(2)=2): By considering D(0)+D(1)+D(2)=9, "+1" is assigned to $C_2,\ C_3,\ C_4, C_5,\ C_6,\ C_7,\ C_0,\ C_1,\ C_2$. Also due to D(0)+D(1)=7, "-1" is assigned to $C_3,\ C_4,\ C_5,\ C_6,\ C_7,\ C_0,\ C_1$.

Finally "+2" is assigned to $C_2$, because "+1" is assigned twice to it.
Also "0" is assigned to the other cells because "+1" and "-1" are assigned to them.

input ↓

| | C0 | C1 | C2 | C3 | C4 | C5 | C6 | C7 |
|---|---|---|---|---|---|---|---|---|
| 3 | + | + | + | | | | | |
| 4 | | | - | + | + | + | + | + |
| 2 | | | ++ | | | | | |
| 5 | + | | - | + | + | + | + | + |
| 6 | | ++ | ++ | + | + | | | |
| 1 | + | | - | - | - | + | + | + |
| 2 | | - | + | + | + | | | |
| 3 | | ++ | + | | | | | |
| 3 | | - | - | + | + | + | + | + |

Fig 4: Explanation of the second-order DWA algorithm when the input data are sequentially given by 3, 4, 2, 5, 6, 1, 2, 3, 3,... "+" cells correspond +1 operation, and "++" cells correspond +2 (2-clock) operation while "-" cells correspond -1 (negative) operation.

## 4. Circuit Realization of Second-order DWA Algorithm

The proposed DWA algorithm described in previous section needs twice unit cell output and minus unit cell output. The twice unit cell output can be realized with 2-clock operation in a switched capacitor DAC in Fig.5. Also the minus unit cell output can be easily realized in a differential switched capacitor circuit by swapping the interconnections of the plus and minus parts.

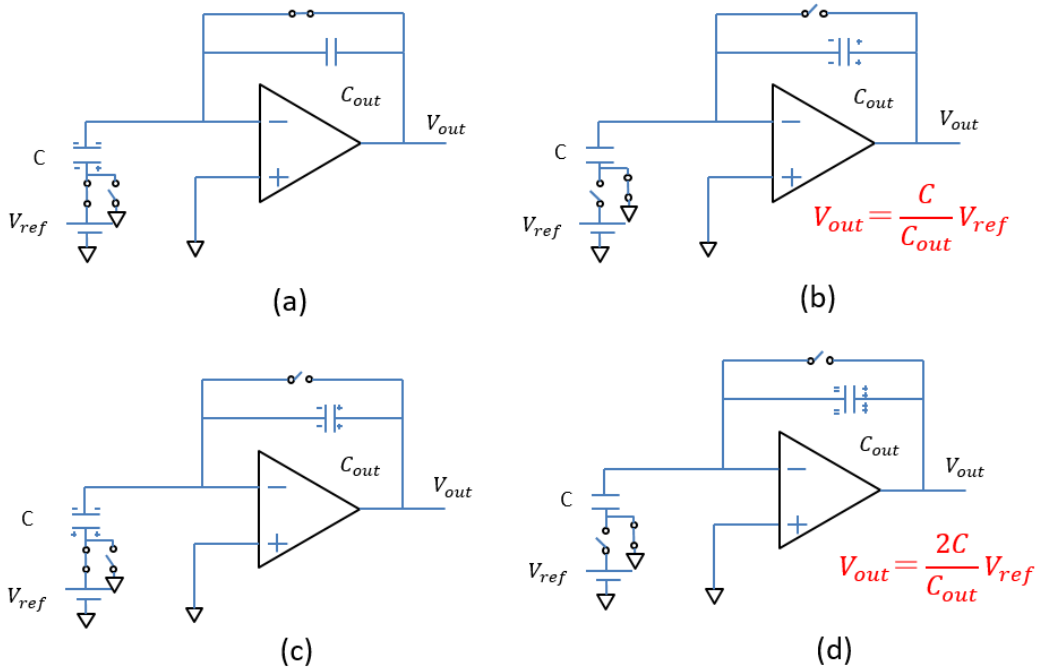


Fig 5: Explanation of +2 (2-clock) operation. (a) First charge into a capacitor C.
(b) Its first transfer to Cout. (c) Second charge into a capacitor C.
(d) Second transfer to Cout. Vout is two times of (C/Cout) Vref.

## 5. Simulation Verification

MATLAB simulations have been conducted with a 3-bit second-order low pass ΔΣADC. We have compared 4 cases: (i) ideal DAC (without mismatches), (ii) with mismatches without DWA, (iii) mismatches with the first-order DWA, (iv) with mismatches with the proposed second-order DWA. Fig. 6 shows the ADC output spectrum comparison, where *F*s is the sampling frequency and *F*in is the input signal frequency. Fig. 7 shows the relationship between SNR and OSR obtained by simulation. We see that our second-order DWA algorithm is effective.

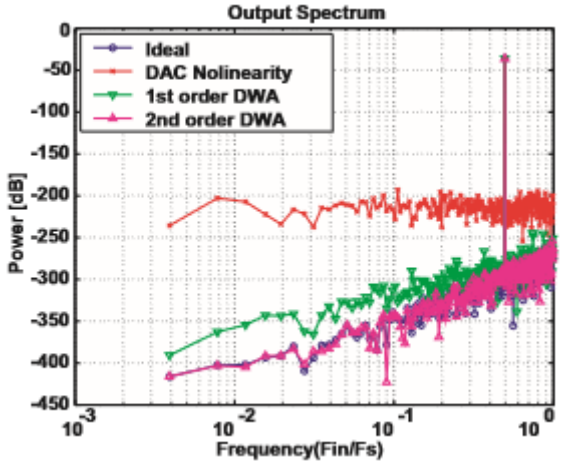


Fig.6: Simulated modulator output spectrum to show the effectiveness of the second-order DWA algorithm.

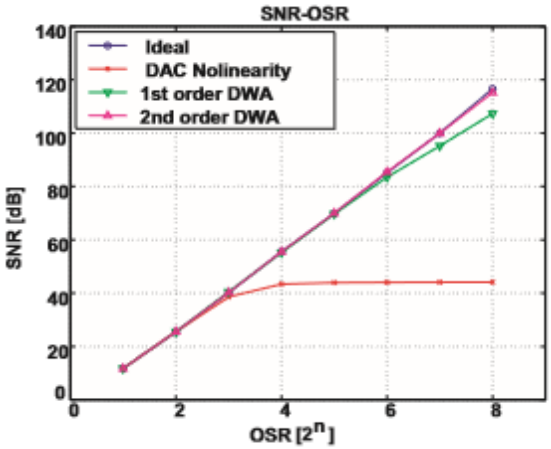


Fig.7: Modulator SNR obtained by MATLAB simulation. SNR stands for signal-to-noise ratio while OSR stands for oversampling ratio. [1]

## 6. Summary

This paper has proposed a second-order DWA algorithm to reduce mismatches among DAC unit elements with second-order noise-shaping. It requires a two clock operation with switched capacitor circuit, which might make the circuit operation slow, but easy to implement. Our MATLAB simulations have confirmed its effectiveness. As the future work, we will revise this algorithm, so that two-clock operation is not required.

**References**

[1] R. Schreier, G.C Temes, Understanding Delta-Sigma Data Converters, ***Wiley-IEEE press***, 2017.

[2] H. San, H. Kobayashi, S. Kawakami, N. Kuroiwa, "A Noise-Shaping Algorithm of Multi-bit DAC Nonlinearities in Complex Bandpass ΔΣ AD Modulators", ***IEICE Trans. Fundamentals,*** vol. E87-A, no. 4, pp.792-800, April 2004.

[3] A. Motozawa, H. Hagiwara, Y. Yamada, H. Kobayashi, T. Komuro, H. San, "Multi-Band-Pass ΔΣ Modulator Techniques and Their Applications", ***IEICE Trans.*** vol. J90-C, no.2, pp.143-158 Feb. 2007.

[4] M. Murakami, H. Kobayashi, S. N. B. Mohyar, O. Kobayashi, T. Miki, J. Kojima,"I-Q Signal Generation Techniques for Communication IC Testing and ATE Systems", ***IEEE International Test Conference***, Fort Worth, TX, Nov. 2016.

[5] I. Jang, M. Seo, M. Kim, J. Lee, S. Baek, S. Kwon, M. Choi, H. Ko, S. Ryu, "A 4.2mW 10MHz BW 74.4dB SNDR Fourth-order CT DSM with Second-order Digital Noise Coupling Utilizing an 8b SAR ADC", ***VLSI Circuits Symposium***, Kyoto, June 2017.

[6] S. Uemori, M. Ishii, H. Kobayashi, D. Hirabayashi, Y. Arakawa, Y. Doi, O. Kobayashi, T. Matsuura, K. Niitsu, Y. Yano, T. Gake, T. J. Yamaguchi, N. Takai,"Multi-bit Sigma-Delta TDC Architecture with Improved Linearity," ***Journal of Electronic Testing: Theory and Applications, Springer***, vol. 29, issue 6, pp. 879-892, Dec. 2013.

[7] Y. Geerts, M. Steyaert, W. Sansen, Design of Multi-Bit Delta-Sigma A/D Converters, ***Kluwer Academic Publisher,*** 2002.

[8] A. Yasuda, H. Tanimoto, T. Iida, "A Third-order ΔΣ Modulator Using Second-order Noise-shaping Dynamic Element Matching,", ***IEEE Journal of Solid-State Circuits,*** vol. 33, no. 12, pp.1879-1886, Dec. 1998.

[9] H. Kobayashi, J. Wei, M. Murakami, J. Kojima, N. Kushita, Y. Du, J. Wang, "Performance Improvement of Delta-Sigma ADC/DAC/TDC Using Digital Technique", ***IEEE 14th International Conference on Solid-State and Integrated Circuit Technology,*** Qingdao, China, Nov. 2018.