Proceedings of International Conference
on Mechanical, Electrical and Medical Intelligent System 2018

MOS Reference Current Source Insensitive to Temperature Variation

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Keywords: MOS reference current source, CMOS analog circuit, temperature characteristics, ZTC

Abstract. This paper proposes two simple MOS reference current sources that are insensitive to temperature variation, utilizing the temperature invariant bias point of the MOSFET I-V characteristics. The NMOSFET has a drain-current-invariant bias-voltage point where the drain current does not depend on temperature, and utilizing this characteristics, the proposed reference current sources consists of NMOSFETs connected in parallel. Then different gate voltages are applied to them so that cancellation of the temperature characteristic dependence on a wide voltage-current operating range is realized. The advantages of these circuits are small chip area and simple configurations. The proposed circuit configurations and their SPICE simulation results are shown.

1. Introduction

Currently, Internet of Things (IoT) is prevailing rapidly, and there, demand for electronic equipment is increasing. Especially the demand for high reliability products are needed. Reliability problems in electronic circuits are mainly caused by process / power supply voltage / temperature (PVT) variation. In this paper, we focus on the temperature in PVT variation and report on two MOS reference current sources that are insensitive to temperature variation. The reference current source provides a constant current to the circuit regardless of the PVT variation. In many cases, at least one reference current or voltage is required in an analog integrated circuit [1-6], and the proposed ones can be used for this purpose. Although a bandgap reference circuit is widely used as a general reference current or voltage source, its circuit configuration is complicated and its chip area is large.

2. Temperature Characteristics of MOSFET

Before describing the proposed reference current source circuit configuration, we show the temperature characteristics of MOSFET. The following equation holds for its drain current ($\boldsymbol{I_d}$).
In the triode region

$$I_d = \frac{W}{L}\mu C_{OX}\left[(V_{GS} - V_{th})V_{DS} - \frac{1}{2}{V_{DS}}^2\right]. \quad (1)$$

In the saturation region

$$I_d = \frac{W}{2L}\mu C_{OX}(V_{GS} - V_{th})^2(1 + \lambda V_{ds}). \quad (2)$$

(W / L: channel width / length, C_{OX}: gate oxide film capacitance per unit area, V_{th}: threshold voltage, μ: mobility, λ: channel modulation effect coefficient). Mobility (μ) is given as follows:

$$\mu = \mu_0(T/T_0)^{-1.5}. \quad (3)$$

μ_0 is the mobility at $T_0(=273.1K)$, whereas μ is the one at T.
In the threshold voltage can be expressed as follows:

$$V_{th} = \frac{\sqrt{2eN_A\varepsilon_{Si}(2\varphi_B)}}{C_{OX}} + 2\varphi_B + V_{FB} \tag{4}$$

$$\frac{dV_{th}}{dT} = \frac{d\varphi_B}{dT}\left(\frac{1}{C_{OX}}\sqrt{\frac{eN_A\varepsilon_{Si}}{\varphi_B}} + 2\right) \tag{5}$$

φ_B is the built-in potential, and n_i is the intrinsic carrier density of the NMOSFET. φ_B and n_i are expressed as follows:

$$\varphi_B = \frac{k_BT}{e}\ln\left(\frac{N_A}{n_i}\right)$$
$$n_i = Nexp\left(-\frac{\varepsilon_g}{2k_BT}\right) \tag{6}$$

Substitute (6) for (5). Then (7) is obtained.

$$\frac{dV_{th}}{dT} = -1 \sim -3 \ [mV/℃\ ] \tag{7}$$

NMOSFET temperature characteristics are derived from the above equations. [4, 5].

Fig. 1 shows SPICE simulation circuit, while Fig. 2 shows its SPICE simulation results of the temperature characteristic of the NMOSFET; we see that its drain current has a temperature invariant characteristic point as shown at the gate voltage V_p. This point is called drain current zero-temperature-coefficient (ZTC) point. In case that the gate voltage is less than V_p, the drain current increases as the temperature becomes high, whereas in case the gate voltage is bigger than V_p, the drain current decreases. Also see [6].

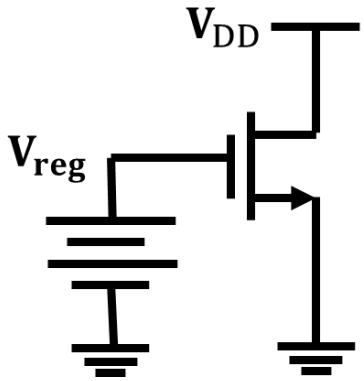

Fig.1 Circuit for MOSFET temperature characteristics check

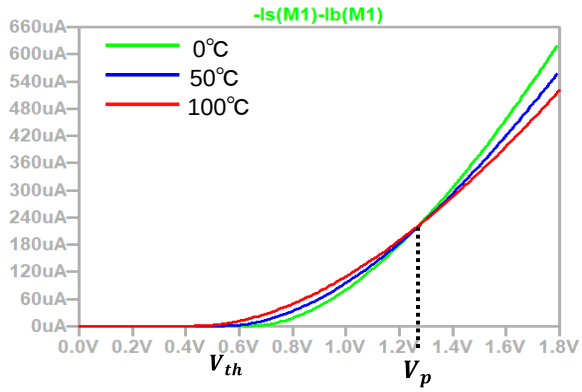

Fig.2 Temperature characteristics of MOSFET

3. Proposed MOS Reference Current Source Insensitive to Temperature

Fig. 3 shows the proposed MOS constant current source, and there, different bias voltages are applied to the gates of the NMOSFETs. Then their currents characteristics as well as their temperature characteristics are different, so that their temperature characteristics as the sum of the currents, or the total output current are cancelled. For the circuit in Fig. 3, when $V_1 > V_2$, the output current ($I_D - V_{GS}$ characteristic) of I_1 is shown in Fig. 4 whereas I_2 is shown in Fig. 5. As a result, the total output current ($I_{out} = I_1 + I_2$) is as shown in Fig.6. As we mentioned in the previous section, the MOS

current temperature dependency characteristic can be cancelled by utilizing the fact that the dominance of the drain current reverses on the low voltage side and the high voltage side of V_P.

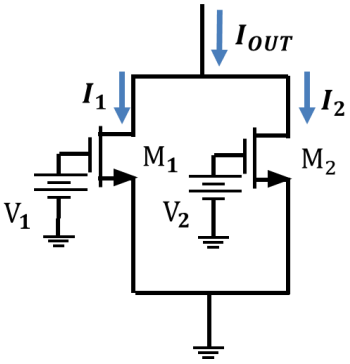

Fig.3 Concept of proposed circuit

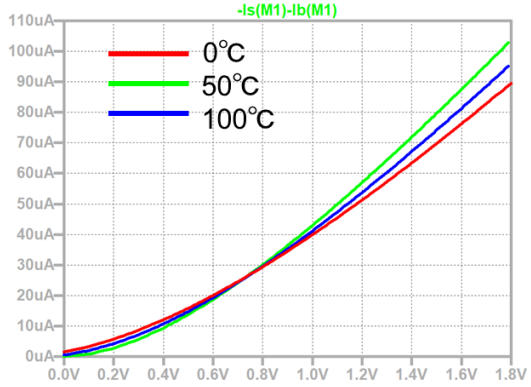

Fig.4 $I_D - V_{GS}$ characteristic of M_1

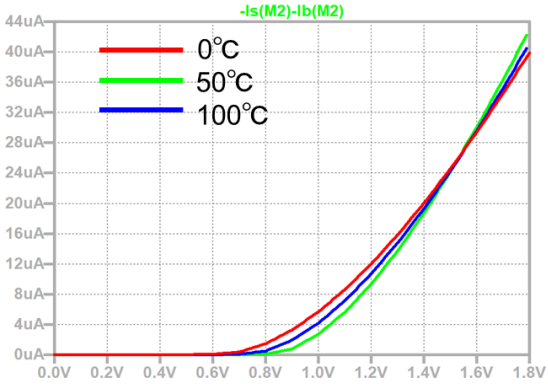

Fig.5 $I_D - V_{GS}$ characteristic of M_2

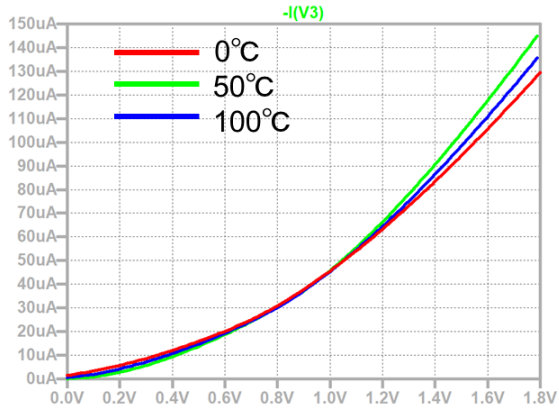

Fig.6 Output current : I_{OUT}

4. Design Method of Proposed Reference Current Source

This section shows the design method of the proposed circuit in Fig. 3. As shown in Fig. 2, V_p is a bias voltage point where there is no temperature dependency of the drain current. In Fig. 3, M_1 is defined as a reference current source MOSFET, while M_2 is defined as a temperature characteristic cancellation MOSFET. The bias voltage (:V_1) is applied to M_1 so that $V_{th} = V_p$ as the reference current source MOSFET. Then we have the following:

$$I_1 = K(V_1 - V_{th})^2(1 + \lambda V_{ds}) \tag{8}$$

$$I_2 = K(V_2 - V_{th})^2(1 + \lambda V_{ds}) \tag{9}$$

Since $V_1 = V_2 + V_P$, it becomes the following expression.

$$I_1 = K(V_{GS} + V_2 + V_P)^2(1 + \lambda V_{ds}) \tag{10}$$

$$I_{OUT} = K\{(V_2 + V_P - V_{th})^2 + (V_2 - V_{th})^2\}(1 + \lambda V_{ds}) \tag{11}$$

$$K \equiv \frac{W}{2L}\mu C_{OX} \tag{12}$$

In addition, by using multiple MOSFETs for temperature characteristics calibration, it is possible to further cancel the temperature characteristic. The output current equation in that case is given by

$$I_{OUT} = K\{(V_2 + V_P - V_{th})^2 + \mathrm{n}(V_2 - V_{th})^2\}(1 + \lambda V_{ds}) \quad (\mathrm{n} = 1,2,3,\ldots\ldots) \tag{13}$$

5.1. Bias Voltage Generator for Proposed Circuit

In this section, we describe gate bias voltage application methods to the NMOSFETs for the proposed circuit as shown in Fig. 7. Here we show the circuit that applies bias by a PMOSFET. The bias voltage is given to the reference NMOS by the PMOS, and temperature characteristics are canceled by the other NMOSFETs.

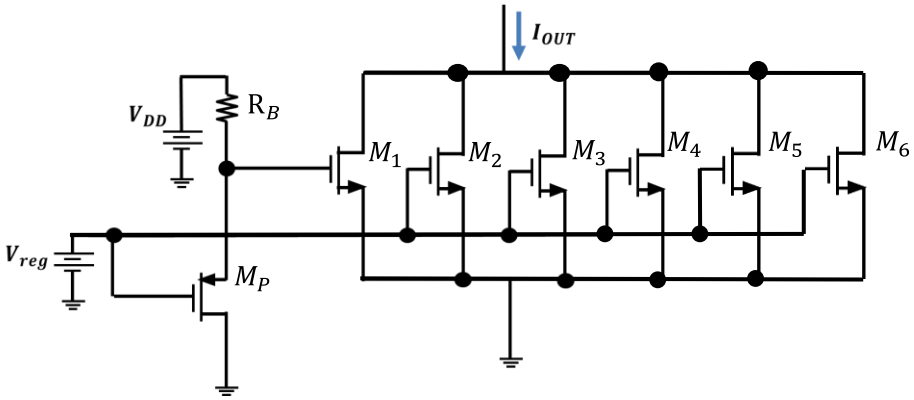

Fig.7 Proposed circuit using PMOSFET

5.2. SPICE Simulation Result

This section shows the SPICE simulation results of the circuit configuration in Fig. 7. V_{DD} is a fixed voltage and V_{reg} is a variable voltage. In this paper, we show the configuration using five temperature cancellation NMOSFETs. Also, by adjusting the resistance in the circuit, the gate voltage of the reference MOS can be changed. In the simulation, the temperature is set at 0℃, 50℃, and 80℃, and the reference temperature is 27℃.

Fig. 8 shows SPICE simulation results. We see that compared with the MOS current-voltage curve ($I_D - V_{GS}$ characteristics) shown in Section 2, the temperature-independent portion is greatly extended. Next, we compare the current-voltage characteristics of the proposed circuit and MOS alone with quantitative comparison with 0℃, 50℃, and 80℃ with 27℃ as the reference temperature. Figs. 9 and 11 show the difference in the output current at other temperatures versus 27℃. It also shows ± 0.25 V centering on the point where the temperature characteristic disappears. The error described in this paper is the absolute difference of $I_D - V_{GS}$ characteristics between 27℃ and each temperature. Then, the evaluation formula is defined as (14).

$$\left|\frac{I_{OUT(27℃)} - I_{OUT(\text{Comparison temperature})}}{I_{OUT(27℃)}}\right| * 100[\%] \qquad (14)$$

According to the simulation result, in the case of a single MOSFET, when the change is ± 0.25 V from V_p, the current value varies by 15% or more at each temperature. On the other hand, the proposed circuit shows that the $I_D - V_{GS}$ characteristics do not change much at each temperature.

Table 1. Simulation conditions.

Parameter	Value
$M_1 \sim M_6$	W＝5[um],L=2[um]
M_P	W＝5[um],L=2[um]
R_B	100 [kΩ]
V_{DD}	3 [V]
V_{reg}	0～1.5 [V]

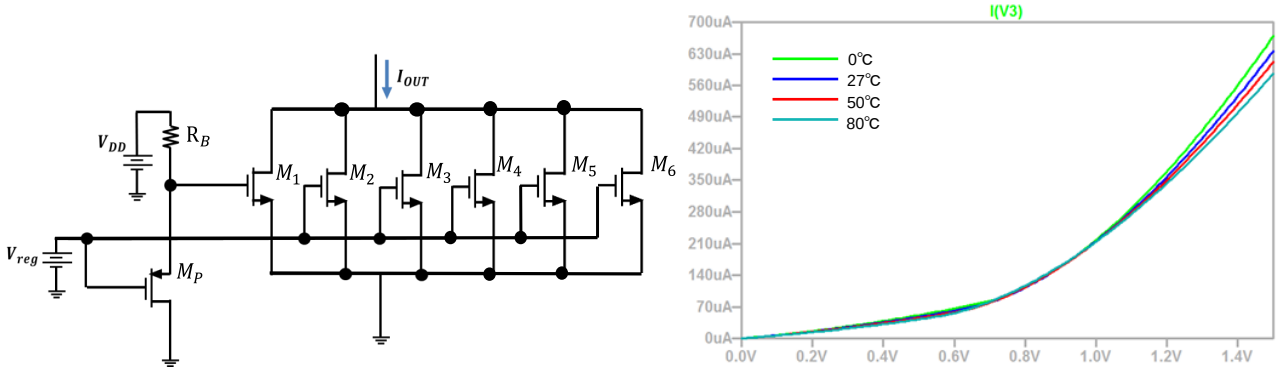

Fig.8 Output current of proposed circuit using PMOS.

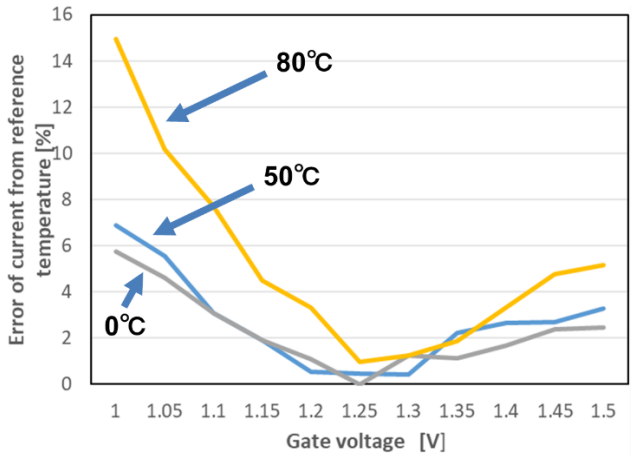

Fig.9 Difference in current-voltage characteristics between 27℃ and other temperatures (MOS alone)

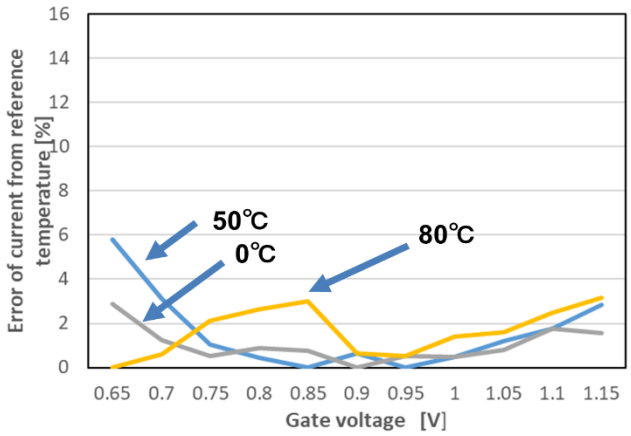

Fig.10 Difference in current-voltage characteristics between 27℃ and other temperatures (proposed circuit)

6. Proposed Circuit Configuration With Self-Bias Voltage Using Negative Feedback

In this section, we describe our proposed temperature characteristic cancellation circuit with self-bias, which is different from the circuit in the previous section. Fig. 11 shows its circuit configuration; M_{N2} and M_{N4} generate temperature-insensitive current, whereas M_{N1} and M_{N3} are added to make the circuit negative feedback and generate the gate voltages of M_{N2} and M_{N4}. The voltage applied to the gate of each MOS is controlled by using R_1 to R_3. M_{N2} and M_{N4} produce the main current. Also, M_{N1} and M_{N3}, M_{N2} and M_{N4} are designed to cancel each other temperature characteristics. M_{P1} to M_{P6} are cascode current mirrors. This circuit requires a start-up circuit.

Fig. 12 shows the simulation results with conditions in Table 2. Then the output current deviation is within 4% at maximum as shown in Table 3, from temperature 0℃ to 100℃, as a reference of temperature 27℃. We see that the circuit in Fig. 11 produces a current which is well insensitive to temperature with a simple configuration.

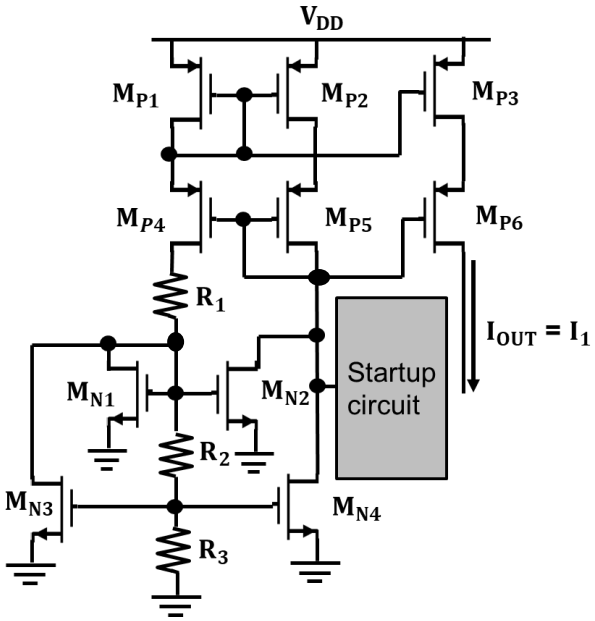

Fig.11 Proposed temperature-insensitive current source with self-bias voltage.

Table 2. Simulation conditions for the circuit in Fig. 11.

Parameter	Value
M_{P1}~M_{P6}	W=40[um],L=2[um]
M_{N1}	W=2[um],L=2[um]
M_{N2},M_{N3}	W=40[um],L=2[um]
M_{N3}	W=300[um],L=2[um]
R_1	4000[Ω]
R_2	2800[Ω]
R_3	2300[Ω]
V_{DD}	5 [V]

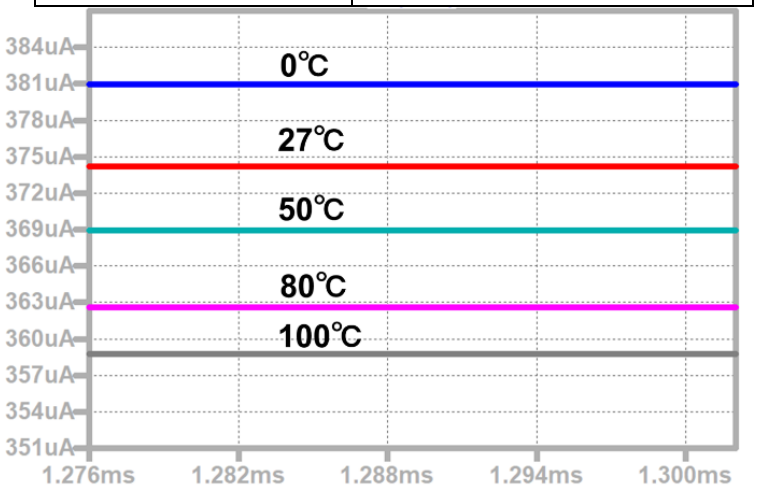

Fig.12 SPICE simulation results of the circuit in Fig.11.

Table 3. Output current for various temperatures

Temperature [℃]	Value[μA]	Difference from 27℃[%]
0	381	1.9
27	374	0
50	369	-1.3
80	363	- 2.9
100	359	- 4.0

7. Conclusion

In this paper, we have focused on the temperature characteristics of MOS current and proposed simple circuits for reference current sources independent of temperature using several MOSFETs in parallel. We show their circuit configurations and their effectiveness with SPICE simulations. As a next step, we will investigate their design methods in more details, as well as process and supply variation effects to them.

The authors would like to thank Jedat Inc. for their some interest in this research.

8. References

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