DWA Algorithm for Band-Pass $\Delta \Sigma$ DAC with Ternary Unit Cells

Jun-ya Kojima      Nene Kushita      Masahiro Murakami
Anna Kuwana        Haruo Kobayashi

Gunma University, Japan
Outline

◆ Research Background

◆ ΔΣDA Converter
  ➢ DWA*Algorithm (* Data-Weighted Averaging)

◆ Simulation Verification
  ➢ Binary, Ternary DWA Overview
  ➢ ΔΣ DA Converter : HP type
  ➢ ΔΣ DA Converter : BP type

◆ Conclusion
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Research Background

Delta Sigma Digital-to-Analog Converter (ΔΣDAC) → Required

- Mostly digital circuit
- High-resolution, high-linearity
- DC signal, low frequency signal generation

Analog signal

Digital signal

Continuous signal
Physical quantity existing in nature

Discrete signal
Binary number

ADC

DAC
ΔΣ Digital to Analog Converter (Low Pass)

Digital input

Integrator

Quantizer

Multi-bit DAC

Analog LPF

Analog output

Δ: Difference
Σ: Integral

Feedback

ΔΣ digital modulator

Digital

Analog

Power spectrum

Usage
- Electric measurement
- Audio system

Noise decrease at low frequency
**Introduction to Ternary**

Ternary \(\Rightarrow\) +, - and 0 value

Binary \(\Rightarrow\) + and 0 value

![Diagram showing the relationship between binary and ternary values](image-url)
Reasons for Ternary Usage

- **Comparison**

  8 current sources

- **Binary**
  - 9 Level
  - 0: $I + e_0$
  - +1: $I + e_1$
  - 1-bit

- **Ternary**
  - 17 Level
  - -1: $I + e_0$
  - 0: $I + e_1$
  - +1: $I + e_2$
  - 1.5-bit

- **Higher resolution for given current sources**
- **Smaller number of current sources for given resolution**
Multi-bit DAC Operation of Ternary (1/3)

DAC input = +3

\[ V_{out} = V_+ - V_- \]

\[ = +[3 \times I + e_0 + e_1 + e_2] R \]

Positive voltage

<table>
<thead>
<tr>
<th>Digital</th>
<th>( V_{out} )</th>
</tr>
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<tbody>
<tr>
<td>+3</td>
<td>( +[3I + e_0 + e_1 + e_2] R )</td>
</tr>
<tr>
<td>0</td>
<td>-</td>
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<tr>
<td>-2</td>
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\[ I_k = I + e_i \]

\( e_i \) : Variation in current cell
Multi-bit DAC Operation of Ternary (2/3)

DAC input = 0

\[ V_{out} = V_+ - V_- \]

= 0

0 voltage

\[ \text{current } I_k = I + e_i \]

\[ e_i : \text{Variation in current cell} \]

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<tr>
<th>Digital</th>
<th>( V_{out} )</th>
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<tbody>
<tr>
<td>+3</td>
<td>+[3I + e_0 + e_1 + e_2] R</td>
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<tr>
<td>0</td>
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<td>-2</td>
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Multi-bit DAC Operation of Ternary (3/3)

\[ V_{out} = V_+ - V_- = -[2 \times I + e_0 + e_1] R \]

Negative voltage

<table>
<thead>
<tr>
<th>Digital</th>
<th>( V_{out} )</th>
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<td>( +[3I + e_0 + e_1 + e_2] R )</td>
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<td>-2</td>
<td>( -[2 \times I + e_0 + e_1] R )</td>
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</table>

\[ I_k = I + e_i \]

\( e_i \): Variation in current cell
Nonlinearity Problem of Multi-bit ΔΣ DAC

- Quantization error ⇒ Decrease
- Performance of following analog filter ⇒ Ease

Nonlinearity Problem

- Characteristics mismatches among multiple unit cell ⇒ Nonlinearity problem

Ideal DAC

Real DAC

Merit
**Multi-bit DAC of Ternary (1/2)**

- **Segment type DAC of ternary**

\[
\text{DAC input} = +3 \quad V_{out} = V_+ - V_-
\]

\[
= +[3 \times I + e_0 + e_1 + e_2] R
\]

- **Switch on from left end**

- **Current source in DAC**
  - **Ideal** ⇒ All equal
  - **Real** ⇒ Process variation on manufacturing

  \[
  \text{current} \quad I_k = I + e_i
  \]
Multi-bit DAC of Ternary (2/2)

◆ Segment type DAC of ternary

DAC input = −2  \[ V_{\text{out}} = V_+ - V_- \]

\[ = -[2 \times I + e_0 + e_1] R \]

![Diagram of multi-bit DAC]

※ Switch on from left end

Current source in DAC

✔ Ideal ⇒ All equal

✔ Real ⇒ Process variation on manufacturing

\[ \text{current } I_k = I + e_i \]
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- ΔΣ DA Converter : BP type

Conclusion
Unit Cell Current Average $I$

Unit cell current average: \[ I = \frac{1}{8} (I_0 + I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7) \]

\[ I_0 = I + e_0 \]
\[ I_1 = I + e_1 \]
\[ I_2 = I + e_2 \]
\[ I_3 = I + e_3 \]
\[ I_4 = I + e_4 \]
\[ I_5 = I + e_5 \]
\[ I_6 = I + e_6 \]
\[ I_7 = I + e_7 \]

Mismatch: \( e_k \)

Total sum: \[ (I_0 + I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7) = 4I + (e_0 + e_1 + e_2 + e_3 + e_4 + e_5 + e_6 + e_7) \]

\[ I = \frac{1}{4} (I_0 + I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7) \]
\[ -\frac{1}{4} (e_0 + e_1 + e_2 + e_3 + e_4 + e_5 + e_6 + e_7) \]
DWA Techniques

w/o DWA

- Errors are flat in spectrum

w/ DWA LP type

- Spectrum of errors are low-pass shaped.
Multi-bit DAC of Ternary and DWA I (1/2)

- DWA* type DAC of ternary (*Data-Weighted Average)

DAC input = +3

\[ V_{out} = V_+ - V_- = +[3 \times I + e_0 + e_1 + e_2] R \]

[3I + e_0 + e_1 + e_2]R

※ In order Switch ON in turn

Positive Voltage

negative Voltage

Cell number

<table>
<thead>
<tr>
<th>Cell number</th>
<th>I_0</th>
<th>I_1</th>
<th>I_2</th>
<th>I_3</th>
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Distribute unit cell mismatch

⇒ Averaging

Improve linearity
◆ DWA* type DAC of ternary (*Data-Weighted Average)

DAC input = \(-2\)

\[ V_{out} = V_+ - V_- = -[2 \times I + e_3 + e_4] R \]

\(-[2I + e_3 + e_4] R\)

※ In order Switch ON in turn

\[ V_{out} = V_+ - V_- = -[2 \times I + e_3 + e_4] R \]

Distribute unit cell mismatch

⇒ Averaging

Improve linearity
Multi-bit DAC of **Ternary and DWA II** (1/3)

- **DWA* type DAC of ternary** (*Data-Weighted Average*)

DAC input = +3

\[
V_{out} = V_+ - V_-
= +[3 \times I + e_0 + e_1 + e_2] R
\]

\[
[3I + e_0 + e_1 + e_2]R
\]

※ In order Switch ON in turn

Distribute unit cell mismatch

⇒ Averaging

Improve linearity
Multi-bit DAC of Ternary and DWA II (2/3)

◆ DWA* type DAC of ternary (*Data-Weighted Average)

DAC input = \(-2\)

\[ V_{out} = V_+ - V_- = -[2 \times I + e_1 + e_2] R \]

\(-[2I + e_1 + e_2] R\)

※ In order Switch ON in turn

Positive Voltage

negative Voltage

Cell number

Back and forth

Distribute unit cell mismatch

⇒ Averaging

Improve linearity
DWA* type DAC of ternary (*Data-Weighted Average)

DAC input = +6

\[ V_{out} = V_+ - V_- \]
\[ = +[6 \times I + e_1 + \cdots + e_6] R \]

※ In order Switch ON in turn

Distribute unit cell mismatch

⇒ Averaging

Improve linearity
DWA type I (Pointer)

1 Pointer

2 Pointers

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DWA type II (Pointer)

1 Pointer

2 Pointers

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  ➢ ΔΣ DA Converter : HP type
  ➢ ΔΣ DA Converter : BP type

◆ Conclusion
## Binary, Ternary DWA Overview

<table>
<thead>
<tr>
<th>Signal Band</th>
<th>Value</th>
<th>Number (N) of Signal Bands</th>
<th>DWA type</th>
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New Findings
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High-Pass ΔΣDAC (Binary)

- High-pass (HP) ΔΣ DAC (N=1)

  Segmented DAC with binary unit cells

< DWA type I >

< DWA type II >
High-Pass ΔΣDAC (Binary)

High-pass (HP) ΔΣ DAC (N=1)

Segmented DAC with binary unit cells

\[ \sigma = 0.1\% \]

Graph showing SNDR (dB) vs. OSR (\(2^n\)) with different configurations of DACs:
- w/ DWA type I
- w/ DWA type II
- w/o DWA
- Ideal

Good Algorithm:
- noise-shaping
- Reduced noise

Diagram showing Power (dB) vs. Fin/Fs for DWA type II
High-Pass ΔΣDAC (Ternary)

- High-pass (HP) ΔΣ DAC (N=1)
- Segmented DAC with ternary unit cells

< DWA type I >

< DWA type II >
High-Pass ΔΣDAC (Ternary)

- High-pass (HP) ΔΣ DAC (N=1)

Segmented DAC with ternary unit cells

**Good Algorithm**

- noise-shaping
- Reduced noise

< DWA type I >

![SNDR vs OSR Graph]

\[ \sigma = 0.1\% \]
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Band-Pass $\Delta \Sigma$ DAC (Binary)

- Band-pass (BP) $\Delta \Sigma$ DAC ($N=2$)
- Segmented DAC with binary unit cells

- $<\text{DWA type I}>$
- $<\text{DWA type II}>$
**Band-Pass ΔΣDAC (Binary)**

- Band-pass (BP) ΔΣ DAC (N=2)

  Segmented DAC with **binary** unit cells

![Graph showing SNDR vs. OSR](image)

\[ \sigma = 0.1\% \]

Good Algorithm

- Noise-shaping

![Power spectrum](image)
Band-Pass ΔΣDAC (Binary)

- Band-pass (BP) ΔΣ DAC (N=4)
  - Segmented DAC with binary unit cells

< DWA type I >

< DWA type II >
Band-Pass $\Delta \Sigma$ DAC (Binary)

- Band-pass (BP) $\Delta \Sigma$ DAC ($N=4$)

Segmented DAC with binary unit cells

- Good Algorithm
  - noise-shaping

$\sigma = 0.1\%$

SNDR (dB) vs. OSR ($2^n$)

Power [dB] vs. Fin/Fs

< DWA type II >
Band-Pass $\Delta \Sigma$ DAC (Ternary)

- Band-pass (BP) $\Delta \Sigma$ DAC ($N=2$)
  - Segmented DAC with ternary unit cells

![Graphs showing performance comparison between DWA type I and DWA type II](image-url)
Band-Pass ΔΣDAC (Ternary)

- Band-pass (BP) ΔΣ DAC (N=2)

Segmented DAC with ternary unit cells

Good Algorithm
- noise-shaping

< DWA type I >

\[ \sigma = 0.1\% \]
Band-Pass ΔΣDAC (Ternary)

- Band-pass (BP) ΔΣ DAC (N=4)

Segmented DAC with ternary unit cells

< DWA type I >

< DWA type II >
Band-Pass $\Delta \Sigma$ DAC (Ternary)

- Band-pass (BP) $\Delta \Sigma$ DAC ($N=4$)

Segmented DAC with ternary unit cells

**Good Algorithm**

- noise-shaping

![Graph showing Power vs. Fin/Fs and SNDR vs. OSR](image)

$\sigma = 0.1\%$
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 Conclusion

- HP, BP multi-bit ΔΣ DACs

  • In case HP, BP ΔΣ DACs with **ternary** unit cells, DWA type I with pointers alternately used is effective.
Thank you for attention
Appendix
**LUT: Save data in advance**  

Data corresponding to input output

**Example**

<table>
<thead>
<tr>
<th>Cat's age</th>
<th>Equivalent human age</th>
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<td>7</td>
<td>44</td>
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<tr>
<td>8</td>
<td>48</td>
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</table>

1 → **LUT** → 17

Cats one year old  

Human being 17 years old
Self-Calibration Algorithm

Preparation
⇒ Feed back value measured with high precision ΔΣ ADC
Save to LUT

Implementation of self-calibration algorithm

<table>
<thead>
<tr>
<th>LUT</th>
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<th>Output</th>
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<tr>
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<td>3</td>
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