



## ICSICT-2018 Participation Report

### EMI Reduction and Output Ripple Improvement of Switching DC-DC Converters with Linear Swept Frequency Modulation



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## ACKNOWLEDGEMENT

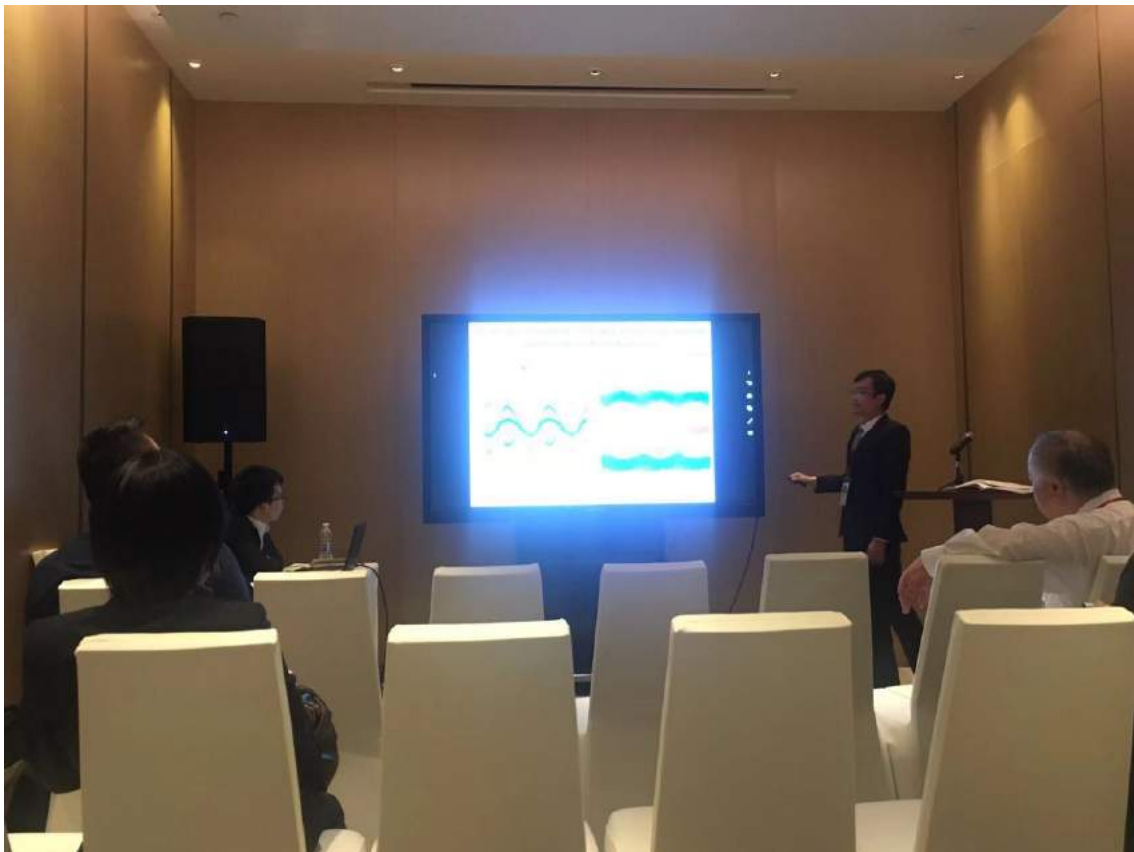
I would like to thank Prof. H. Kobayashi, Dr. Kobori and Kobayashi Lab members who gave me a good chance to travel many beautiful places at Qingdao in China.







I would like to thank my lovely Prof. Kobayashi!



It was the first time I attended a large conference, therefore I was very nervous.



I would like to thank my lovely Dr. Kobori!



I would like to thank my lovely Dr. Mastuda!





I could see many scholars from all over the world.





I would like to thank Prof. Thomas Skotnicki!

<https://www.semiwiki.com/forum/content/4830-thomas-skotnicki-fd-soi-26-years-making.html>

In one particular instance, Thomas had a long fight over a key paper at IEEE Transactions on Electron Devices, where the editors didn't want to publish. Then a serendipitous change of editor opened the door to publication; the paper was given the Rappaport Award, as "best publication of the year" by the IEEE Electron Devices Society. As Mahatma Gandhi said: First they ignore you, then they laugh at you, then they fight you, then you win.

With these successes building momentum, the semiconductor community finally started to believe in the idea. One important believer was Carlos Mazure from SOITEC where they make wafer blanks. SOITEC was excited by the potential of these thin-box, short-channel devices, but at the time they could only make a box 145nm thick, not the 10-20nm that was required. Under Carlos' leadership, SOITEC was instrumental in launching the R&D program that successfully delivered thin box SOI wafers.

At this point LETI got involved. Although most of their work was on thick-box devices, they decided to collaborate with Thomas to actually fabricate his ideas into real silicon. LETI helped with both silicon-on-nothing and then with thin-box FD-SOI. Up until then it had all been equations. The whole idea gained speed once the project was transferred from the whiteboard to silicon.

Then, in 2011, Intel announced FinFET. Everyone already knew about FinFET and it was known to be really difficult technology. The complexity of FinFETs and the concerns about efficiently producing it led to raucous debate within the industry and within companies. Thomas sold the deal at ST when he showed that by turning a FinFET on its side you pretty much had silicon-on-nothing, FD-SOI with a thin box. It was the biggest day of Thomas' professional life when ST's top management, including CEO Carlo Bozotti, COO Jean-Marc Chery, and EVP of Front-End Manufacturing Joël Hartmann made the decision to take its Ultra-Thin Body and Box FD-SOI to manufacture. Thomas recounted that from initial conception and equations to industrial fabrication it took 26 years.

Industrialization of the manufacturing process went fast since the technology worked even better than the equations and FD-SOI is a much simpler technology than FinFET—it leverages the learnings of planar (bulk) silicon with fewer masks and processing steps, albeit with a slightly more expensive wafer.

Still, selling FD-SOI beyond ST took a bit more time, as initially ST was alone and customers require partners, second sources, alliances and not just a single manufacturer. Today, however, the technology is being deployed worldwide not just at ST but also at Samsung and GlobalFoundries.

As a marketing guy, I can't but help noticing a missed opportunity. "Silicon on nothing" is a much better name than FD-SOI.







I would like to thank Prof. Adrian Ionescu!

<https://people.epfl.ch/cgi-bin/people?id=122431&lang=en&cvlang=en>

EPFL > People@EPFL > Mihai Adrian Ionescu

français / English

## MIHAI ADRIAN IONESCU

**Contact** **Biography & current work** **Main publications** **Teaching & PhD**

Share:    

### Biography and current work

#### Mission

The Nanoelectronic Devices group (NANOLAB) is working on various subjects in the field of silicon micro/nano-electronics with special emphasis on the technology, design and modelling of nanoscale solid-state devices (including Silicon-On-Insulator devices, few-electron devices, hybrid SET/CMOS, single electron memory, nanowires and nanotubes), Radio Frequency MEMS devices for in- and above-IC and integrated optoelectronic devices.

The group is interested in exploring new materials, novel fabrication techniques, and novel device concepts for future nanoelectronic systems.

#### Biography

Adrian M. Ionescu is Full Professor at the Swiss Federal Institute of Technology, Lausanne, Switzerland. He received the B.S./M.S. and Ph.D. degrees from the Polytechnic Institute of Bucharest, Romania and the National Polytechnic Institute of Grenoble, France, in 1989 and 1997, respectively. He has held staff and/or visiting positions at LETI-CEA, Grenoble, France and INP Grenoble, France and Stanford University, USA, in 1998 and 1999.

Dr. Ionescu has published more than 400 articles in international journals and conferences. He received many Best Paper Awards in international conferences, the Annual Award of the Technical Section of the Romanian Academy of Sciences in 1994 and the Blondel Medal in 2009 for remarkable contributions to the progress in engineering sciences in the domain of electronics. He is the 2013 recipient of the IBM Faculty Award in Engineering. He served the IEDM and VLSI conference technical committees and was the Technical Program Committee (Co)Chair of ESSDERC in 2006 and 2013.

He is director of the Laboratory of Micro/Nanoelectronic Devices (NANOLAB). He is appointed as national representative of Switzerland for the European Nanoelectronics Initiative Advisory Council (ENIAC) and member of the Scientific Committee of CATRENE. Dr. Ionescu is the European Chapter Chair of the ITRS Emerging Research Devices Working Group.



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### FIELDS OF EXPERTISE

Nanoelectronic devices  
Silicon nanotechnology  
Silicon On Insulator  
Radio Frequency MEMS and NEMS  
Small Swing Switches  
Emerging Memories  
Modeling and Simulation of Solid-State Electronic





I would like to thank Prof. Yeo Kiat Seng!

<https://epd.sutd.edu.sg/people/faculty/yeo-kiat-seng>

#### Yeo Kiat Seng

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#### Research Areas:

Electrical Engineering

Pillar / Cluster: Engineering Product Development



#### Biography



Associate Provost for International Relations and Graduate Studies, Professor Yeo Kiat-Seng joined Singapore University of Technology and Design (SUTD) on 2nd July 2014. He has over 25 years of experience in industry, academia and consultancy. Before his appointment at SUTD, he was Full Professor at Nanyang Technological University (NTU), Singapore, and spent 13 years in management positions as Associate Chair (Research), Head of Circuits and Systems and Sub-Dean (Student Affairs) in the School of Electrical and Electronic Engineering (EEE). As Associate Chair (Research), he developed EEE mega research centres into a top-notch hub to advance cutting-edge research innovations and unparalleled inventions. Prof. Yeo was also a Fellow of the Renaissance Engineering Programme (REP) and served as Senator and Advisory Board Member at NTU. Besides, he was the Founding Director of VIRTUS, a \$550 million IC Design Centre of Excellence jointly set up by NTU and Singapore Economic Development Board. Since 1996, he has been providing consultancy services to statutory boards, local SMEs and multinational corporations in the areas of electronics and IC design.

Currently, Prof. Yeo is a Visiting Professor in the School of EEE at NTU, a Member of Board of Advisors of the Singapore Semiconductor Industry Association, a Council Member of the Assembly & Test WSQ Framework Industry Skills and Training of the Singapore Workforce Development Agency, a Member of the Engineering Science (ES) Advisory Committee of Ngee Ann Polytechnic and a Member of Hwa Chong Institutional IP Advisory Board.



I would like to thank Prof. Yong Lian!


<http://eecs.lassonde.yorku.ca/faculty/peter-lian/>

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### RESEARCH INTERESTS

- Zero-power wearable wireless biomedical sensors;
- Miniaturized biomedical instrumentations;
- Ultra low power biomedical circuits and systems;
- Signal processing.



### BIO

Peter (Yong) Lian received the B.Sc degree from the College of Economics & Management of Shanghai JiaoTong University (SJTU) in 1984, and the Ph.D degree from the EE Department of National University of Singapore (NUS) in 1994. He worked in industry for 9 years and joined NUS in 1996 where he served as the Deputy Department Head for Research, Area Director for IC and Embedded Systems in the ECE Department, member of University Tenure and Promotion Committee, and member of Senate Delegacy. His last appointment in NUS is the Provost's Chair Professor. Currently he is the Professor in the Department of Computer Science and Engineering.

His research has attracted more than US\$20 million research funding from various sources in the past 6 years, the most recent one being a US\$8 million grant under the 8th Competitive Research Program from the National Research Foundation of Singapore. Dr. Lian's research has won more than 20 awards including 1996 Guillemin-Cauer Award for the Best Paper published in the IEEE Transactions on Circuits and Systems and 2008 Multimedia Communications Best Paper Award from the IEEE Communications Society, the latest being the Institute of Engineers Singapore Prestigious Engineering Achievement Award in 2011 and Faculty Research Award of NUS in 2012. Dr. Lian is the Founder of ClearBridge Vital Signs Pte Ltd, a start-up company for wireless wearable biomedical devices. Dr. Lian is Fellow of IEEE and Fellow of Academy of Engineering Singapore.

### Staff Information

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🔗 [Visit Website](#)

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### Stay in Touch





I would like to thank Prof. Cheng Yuhua!

<http://eecs.pku.edu.cn/EN/People/Faculty/Detail/?ID=5954>



Cheng, Yuhua

**Professor**

**Research Interests:** Advanced analog/mixed-signal/RF integrated circuits for system integration applications

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**Cheng, Yuhua** received the BSEE, MSEE, and Ph.D. EE degrees in Shandong Polytechnic University (Now Shandong University), Tianjin University, and Tsinghua University, China in 1982, 1985 and 1989, respectively. In 1990, he joined in the Institute of Microelectronics (IME), Peking University, China. From 1992 to 1996, he was an associate professor in IME. He is now with Peking University, as a full professor.

Dr. Cheng has served on many Technical Program Committees and chaired numerous Sub-committees at international conferences, including the IEEE Custom Integrated Circuits Conference (CICC) (from 2002 to 2005) and Radio Frequency Integrated Circuits Symposium (since 2002). He organized and participated in numerous workshops and panels related to RFCMOS technology and SoC design. He has authored and co-authored over 160 research papers, two book chapters, two books "MOSFET Modeling & BSIM3 User's Guide" by Kluwer Academic Publishers (1999), and "Device modeling for analog/RF circuit design" by John Wiley and Sons (2002). He was a Guest Editor for IEEE Journal of Solid-State Circuits. He is an IEEE Fellow and a member of both Electronic Device Society (EDS) and Solid-state Circuit Society (SSCS). His research interests include smart power discrete semiconductor devices and advanced analog/mixed-signal/RF integrated circuits for system integration applications.

Dr. Cheng was the principal developer to BSIM3v3 (Yuhua Cheng, et al., BSIM3v3 User's Manual, UC Berkeley, UCB/ERL M97/2, 1997). Due to Dr. Cheng's efforts, the discontinuity problems, considered as a major shortcoming in BSIM models, were resolved in BSIM3v3, while many new physical effects were implemented. BSIM3v3 has been used worldwide by foundries and design companies for IC simulation. It was selected as the first MOSFET model for compact model standardization effort for IC simulation by Electronics Industry Association/Compact Model Council and given an R&D 100 Award in 1996.

Since 2006, Dr. Cheng has been conducting research on ESD for more than 10 years, which has made significant achievements, which resulted in more than 30 research papers. He shared with the IC industry his research results in international conferences and journals including IEEE Journal of Solid-state Circuits, IEEE Trans. On Electron Devices, and IEEE Electron Devices Letters.



I would like to respect, thank and acknowledge the ICSICT 2018 which gave me a chance to represent my research paper.



I would like to thank my new friend!





I would like to thank my new friend!



I would like to thank my new friend!



I would like to thank my new friend!





I would like to thank my new friends!

<https://www.hisim.hiroshima-u.ac.jp/>

## HiSIM 研究センター

- ▶ ENGLISH 
- ▶ トップページ
- ▶ 理念
- ▶ HiSIM-モデル研究履歴
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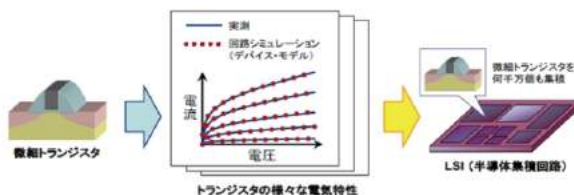
◆ HiSIM: Hiroshima-University STARC IGFET Model

### The 2<sup>nd</sup> International Symposium on Device Circuit and Systems (ISDCS 2019)

を2019年3月6日～8日に向け、広島大学 東広島キャンパスにて開催予定。  
(ISDCSのウェブサイトへのリンクは[こちら](#)です。)

#### コンパクトトランジスタモデルHiSIMの概要

集積回路は膨大な数のトランジスタを組み合わせて様々な機能を作り出している。  
この際に、トランジスタ特性を記述したトランジスタモデルを用いて、与えられた電圧に対するトランジスタ応答を計算して集積回路特性を予測しながら設計を進めていく。トランジスタ特性としては電圧に対する電流やトランジスタに与えられる電荷応答がある。(図1参照。)









谢谢

Don't be sad my friend!

I hope that you will be able to come back Qingdao on someday in future!

