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INVITED

Output Voltage Ripple Correction with Spread Spectrum Using Frequency Modulation for Switching Converters

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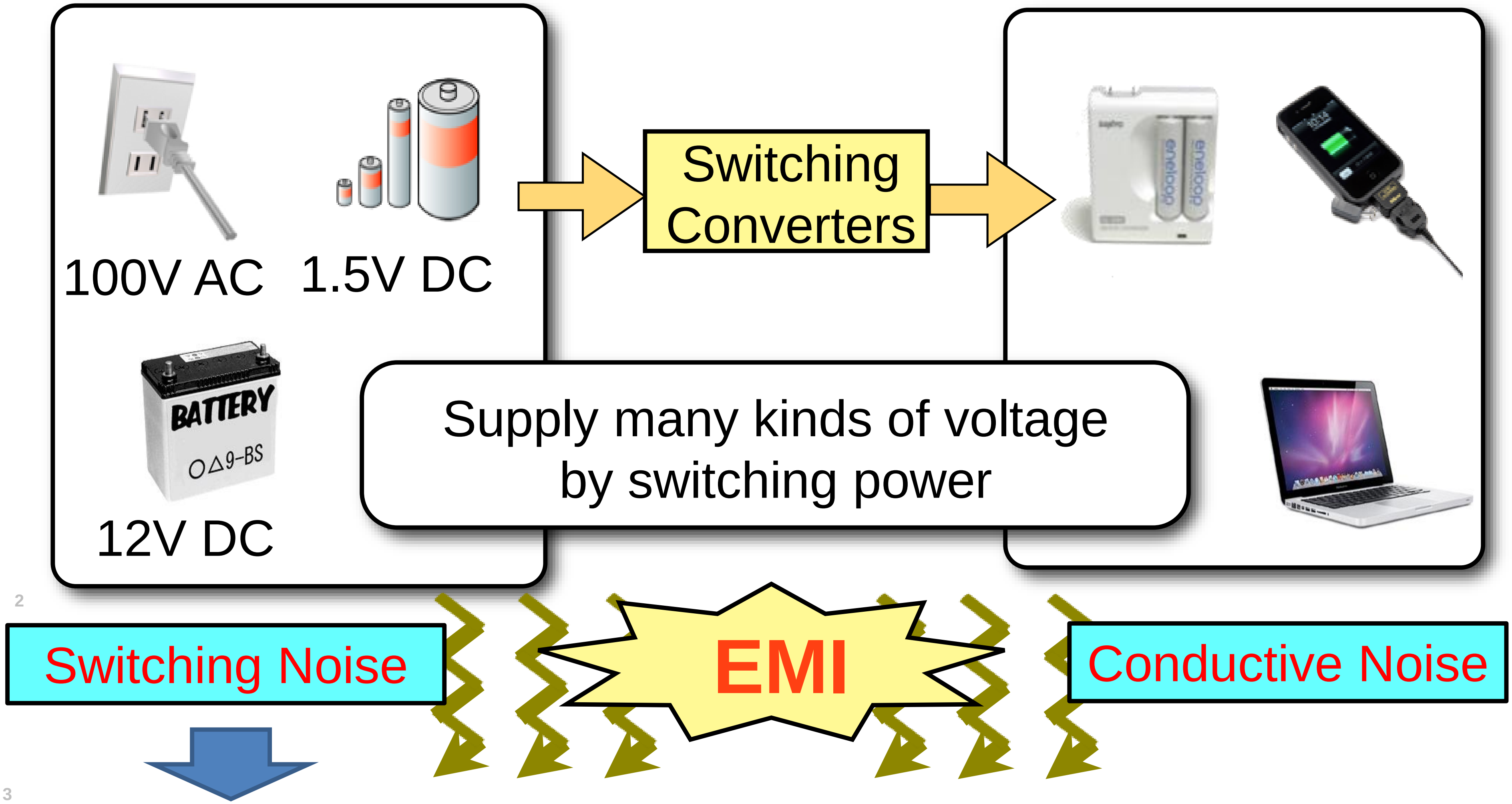
Outline

1. Background
   1-1 Switching Converter
   1-2 EMI Reduction Method
2. EMI Reduction with Clock Modulation
   2-1 Frequency modulation method
   2-2 Relationship with modulation level
3. Output Voltage Ripple Correction
   3-1 Analyze the correction method
   3-2 Simulation results
4. Conclusion

EMI: Electro-Magnetic Interference

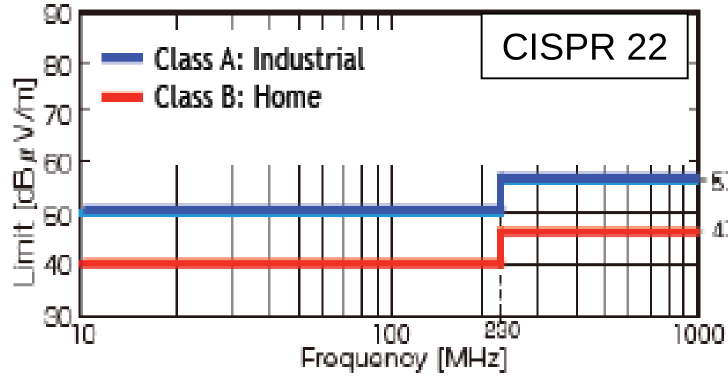
1. Background



- Important to reduce SW noise & conductive noise.
- Decrease the spectrum level of switching noise.

research process

● Need to reduce noise spectrum level
below the Standard Level



★ By modulating the clock frequency,
spread the clock noise around
the clock frequency or its harmonics.

◆ The more clock modulation increases,
the lower noise spectrum decreases.
⇒ Output ripple increases. ⇒ No Good!

※ Our Objective

● Decrease the peak level of spread spectrum without increase of the output ripple by compensating the clock modulation.

1-1 Buck-type Switching Converter

* Output Voltage Vo is compared with reference voltage Vref and amplified to get ⊿Vo.
* ⊿Vo is compared with SAW-tooth signal to generate Pulse Width Modulation (PWM) pulse.
* PWM controls power SW & I_L changes to control Vo stable.

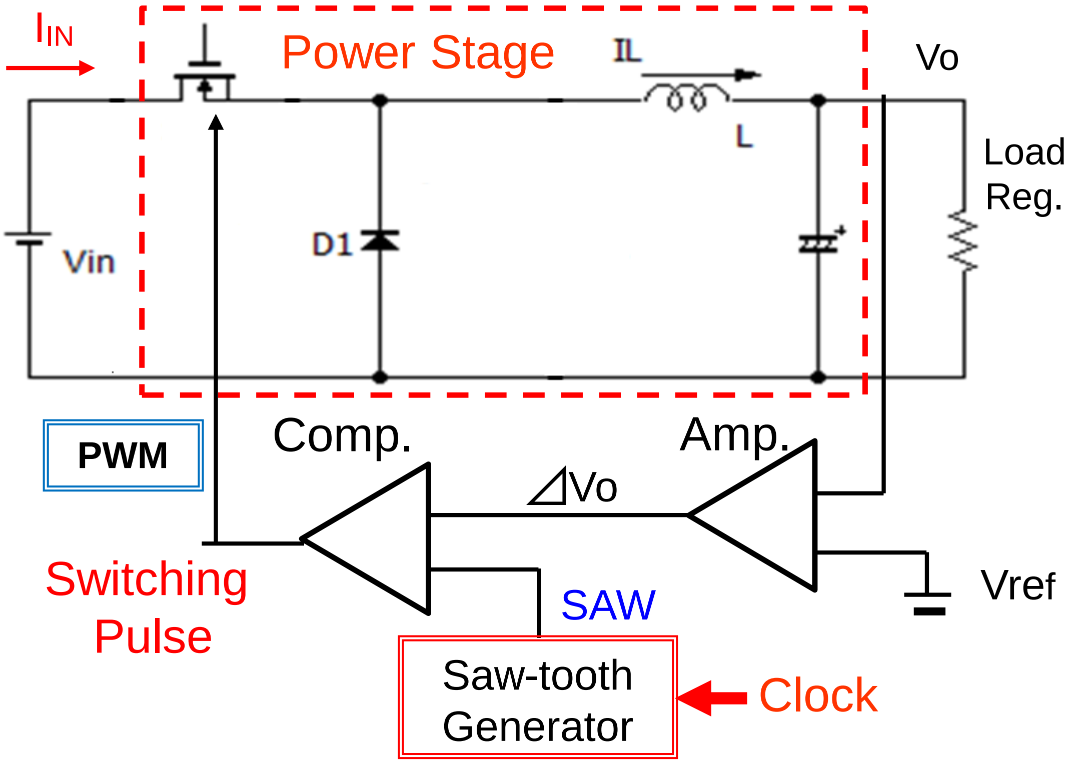


Fig.1-2 Circuit of the Buck converter

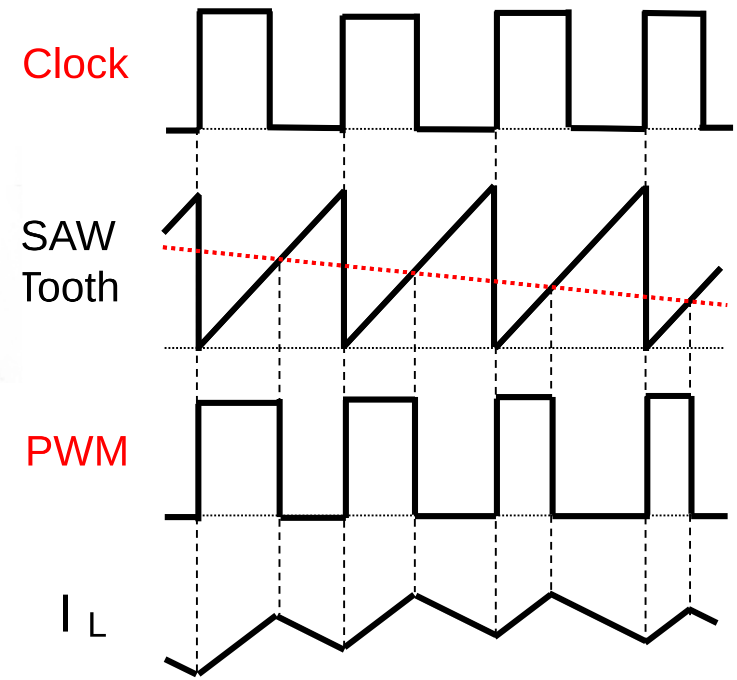


Fig.1-3 Waveforms

- Output ripple : 2.5mV
- Spectrum of PWM pulse:
  Peak level @ Fck: 3.1V

★Important to reduce
the spectrum level at Fck.

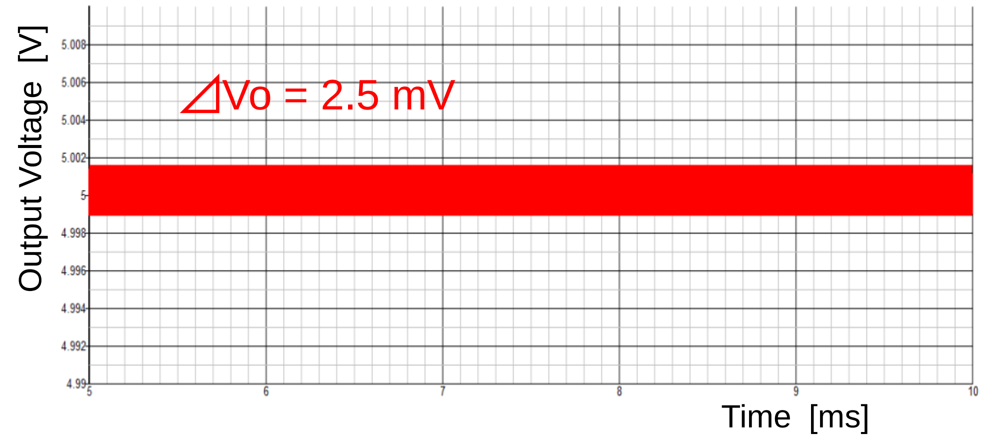


Fig.1-4 Stable output ripple

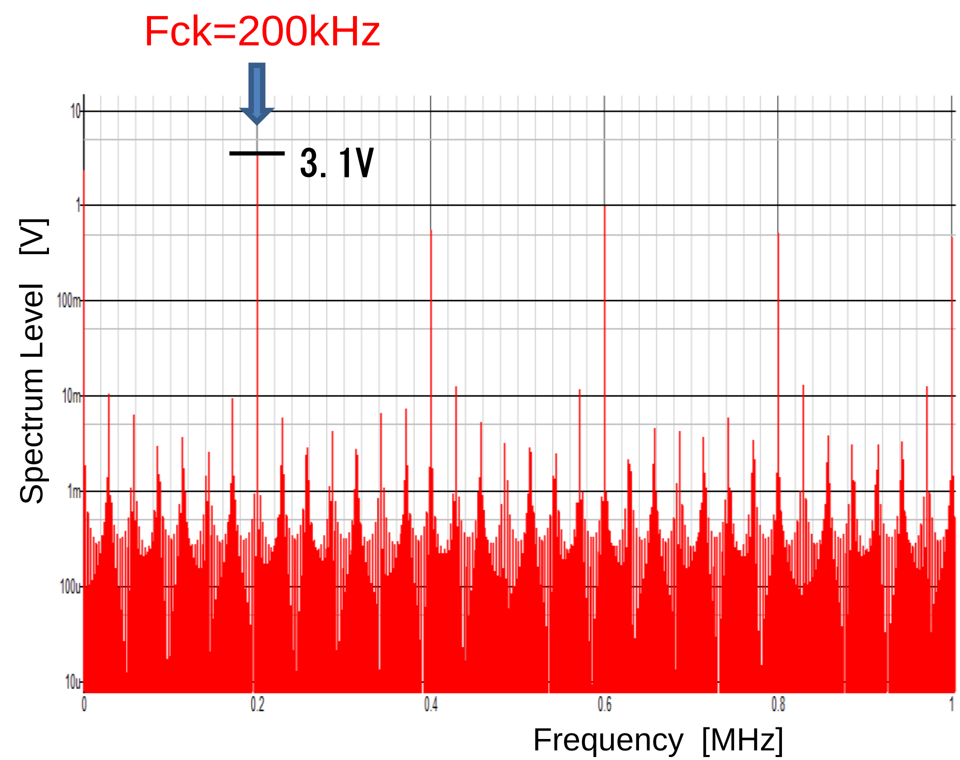


Fig.1-5 Noise Spectrum

Table 1 Parameter of converter

Input Voltage	12 [V]
Output Voltage	5.0 [V]
Clock Frequency	200 [kHz]
Inductance	200 [uH]
Capacitance	220 [uF]

1-2 Spectrum Reduction Method

＊ To reduce EMI noise, clock frequency is modulated.

⇒ Clock spectrum is spread and reduced.

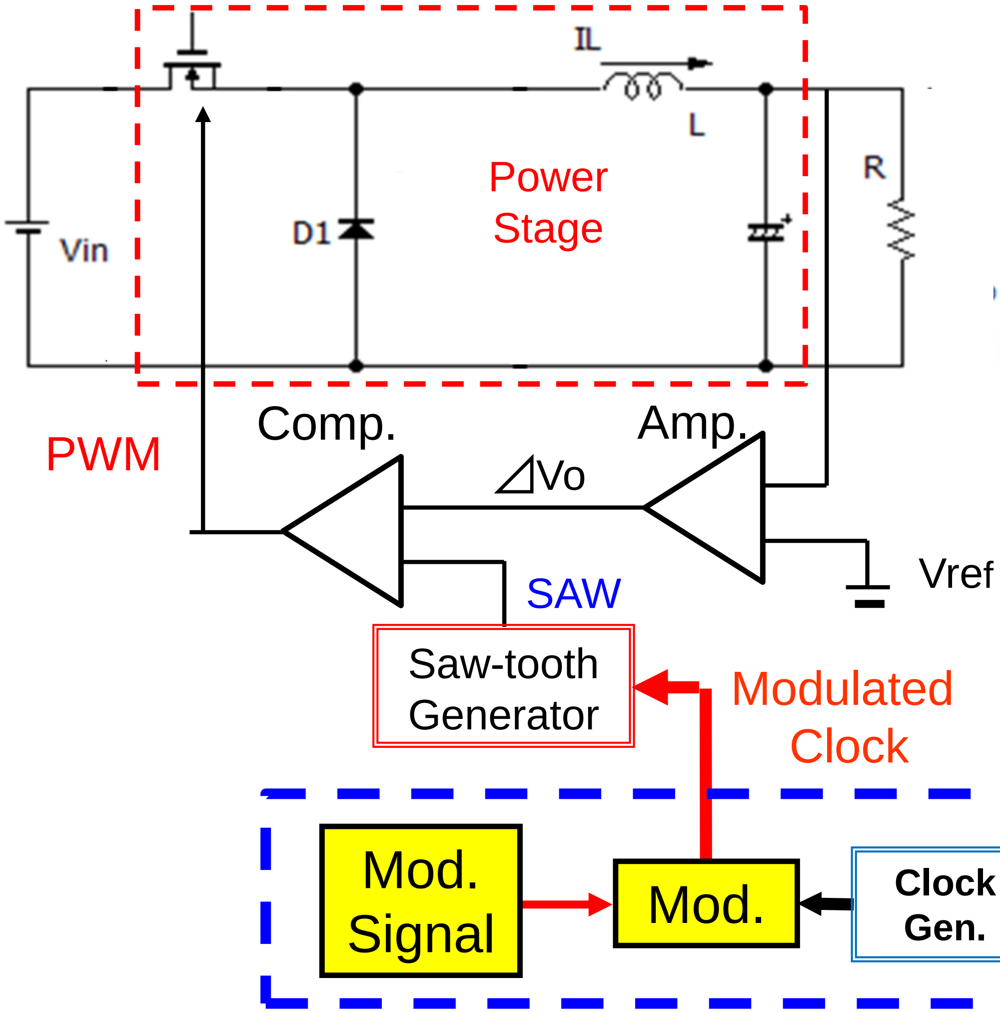


Fig. 1-5 Converter with EMI reduction

＊Clock to SAW generator is modulated by shaking phase or frequency.

＊PWM pulse is modulated and the clock frequency is spread.

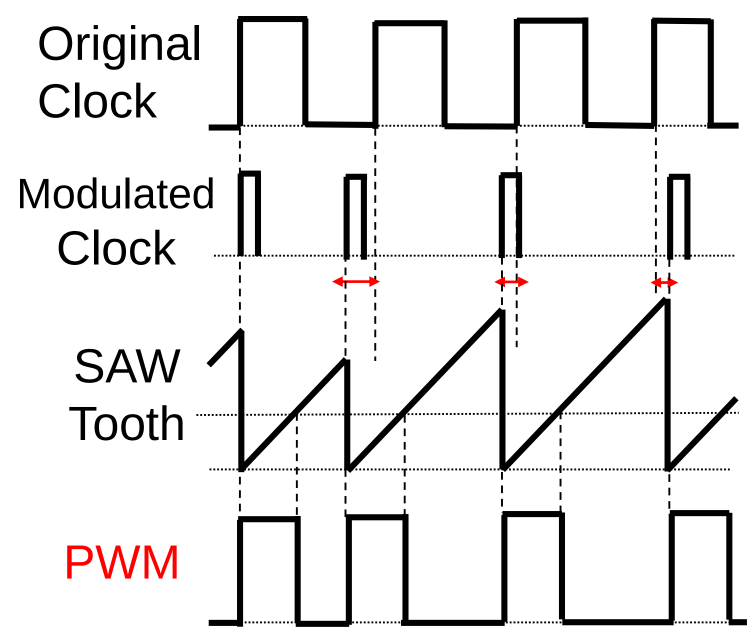


Fig.1-6 Waveforms

● Modulation signal: SIN

- Frequency： Fm =500 Hz
- Amplitude ： Vm=2 Vpp

＊Spectrum level is reduced from 3.1V to 0.5V (−15.8dB).

But output voltage ripple is ･･･

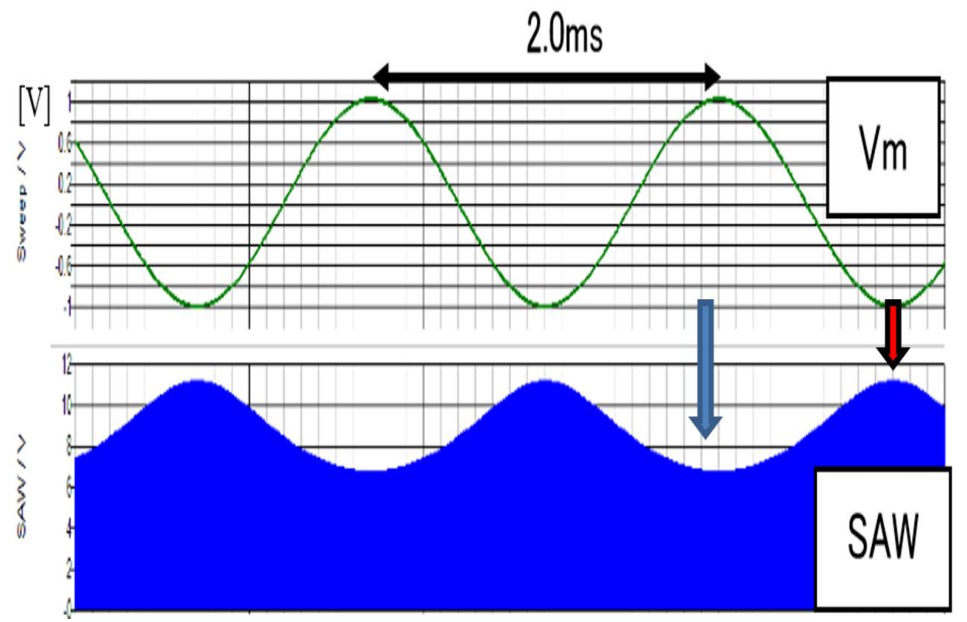


Fig.1-6 Modulation signal

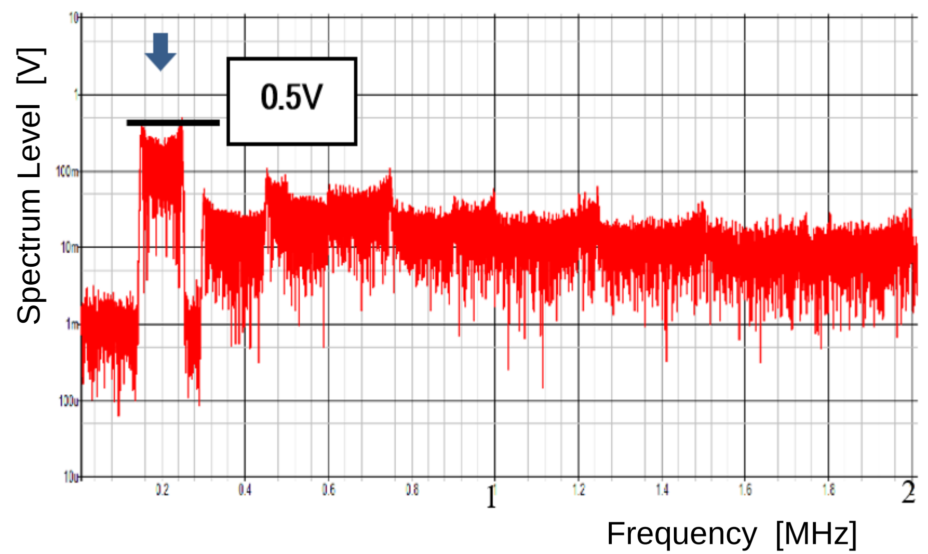


Fig.1-7 Spectrum with modulation

● Modulation signal: SIN

- Frequency： Fm =500 Hz
- Amplitude ： Vm=2 Vpp

＊Spectrum level is reduced from 3.1V to 0.5V (−15.8dB).

★Output ripple increased 20mV.

Need to suppress the ripple keeping spectrum level low.

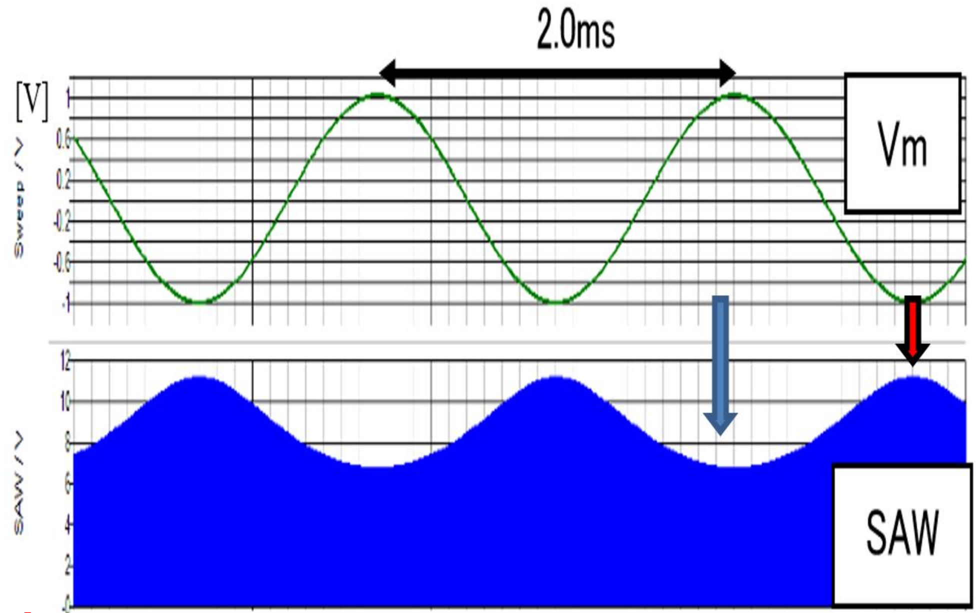


Fig.1-6 Modulation signals

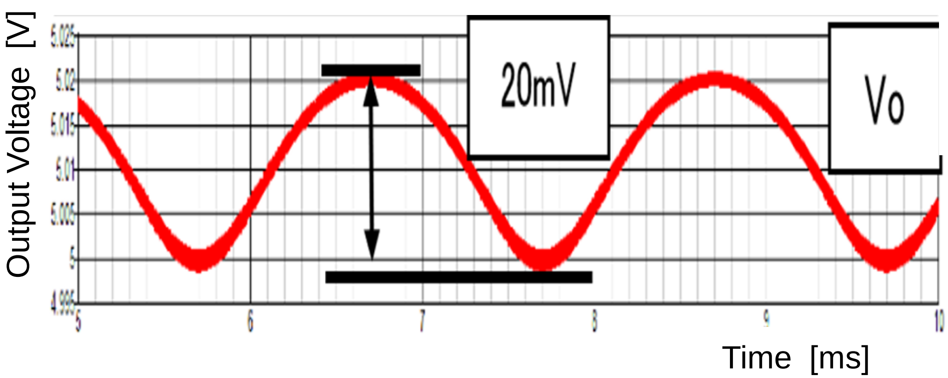


Fig.1-8 Spectrum with modulation

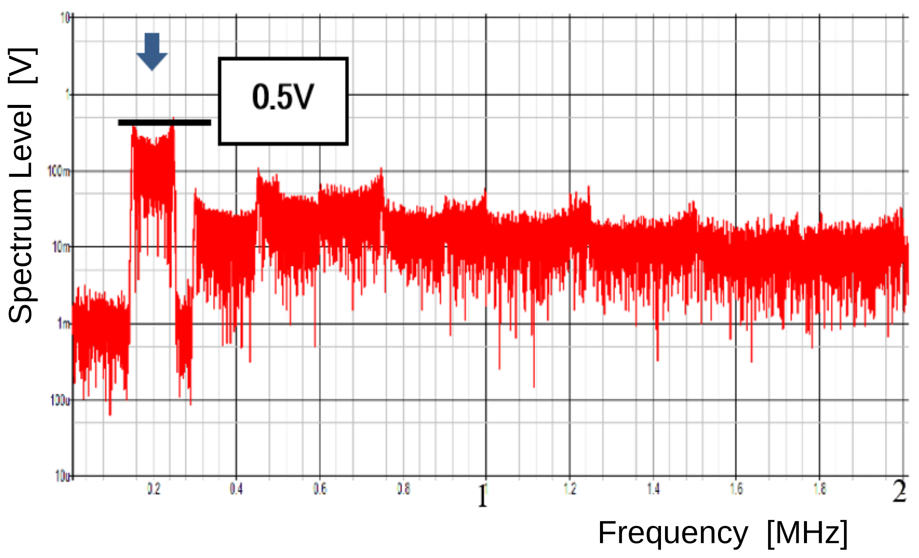


Fig.1-7 Spectrum with modulation

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   1-2 EMI Reduction Method

2. EMI Reduction with Clock Modulation
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EMI: Electro-Magnetic Interference

2. EMI Reduction with Frequency Modulation

2-1 Frequency modulation method

VCO: Voltage Controlled Oscillator

* Clock pulse is generated using VCO.
  - VCO is modulated by Triangular (or Sine) signal.
* Spectrum of PWM pulse has flat top shapes.
  - Peak level is reduced from 3.1V to 0.55V. (−15dB)

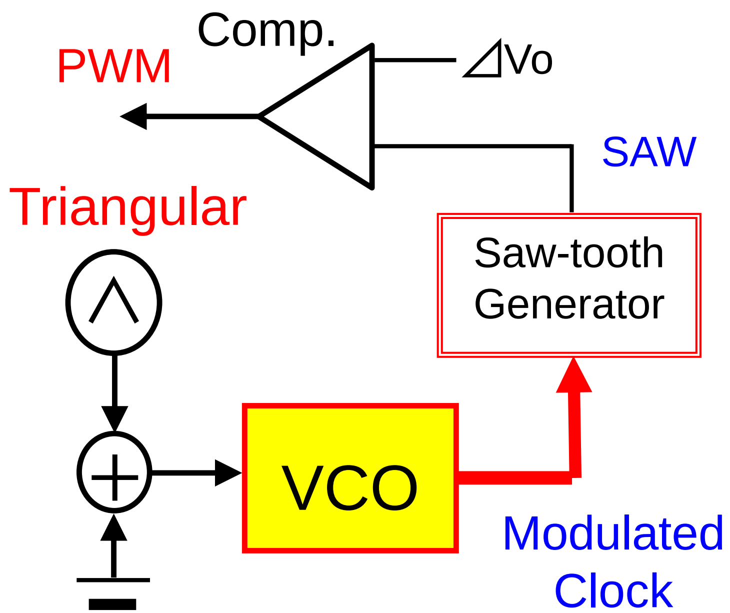

Fig. 2-1 Frequency modulation circuit

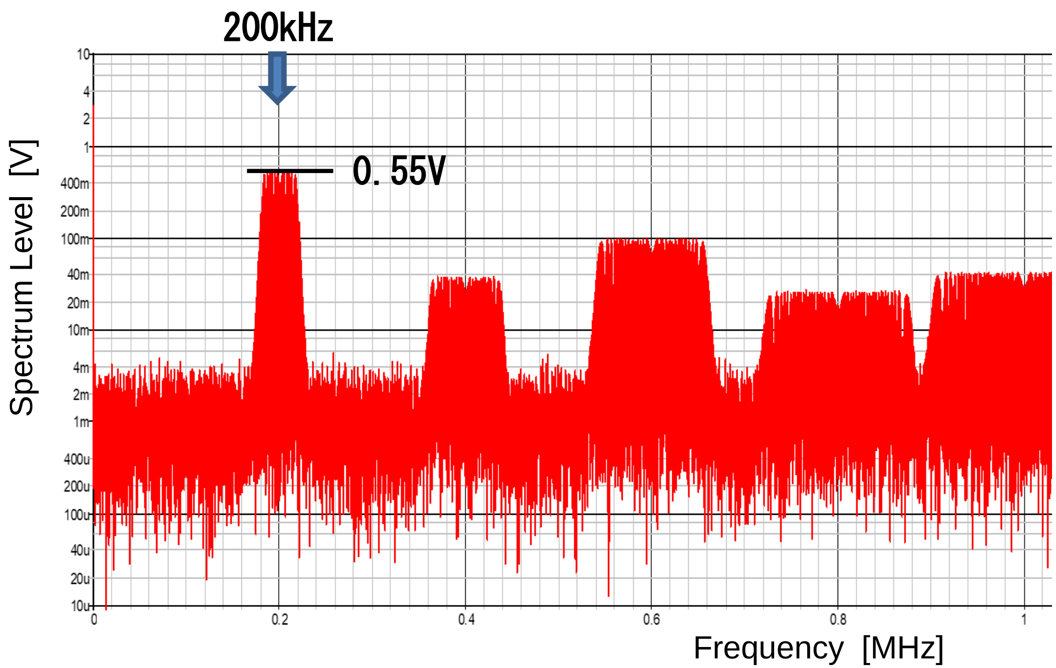

Fig. 2-2 Spectrum with Linear Sweep

● Comparison of spectrum

- (a) Without modulation (Vm=0 V)
- (b) with modulation 1 (Vm=0.5V)
- (c) with modulation 2 (Vm=2.0V)

● Spectrum level at Fck

- 3.1V ⇒ 0.9V ⇒ 0.5V
  [−10.4dB] [−5.1dB]

Check the relationship between Vm & spectrum level

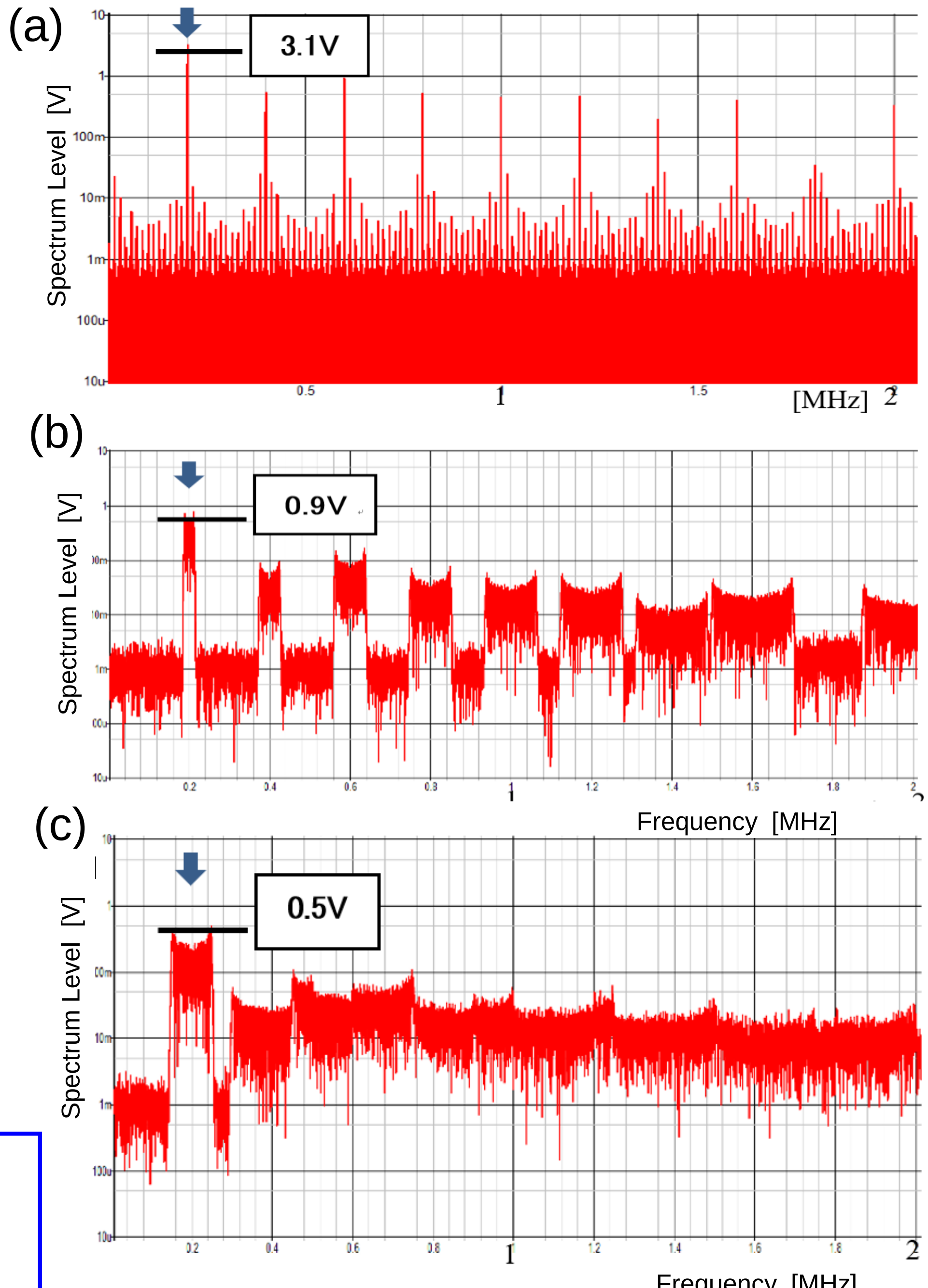

Fig.2-5 Spread Spectrum

2-2 Relationship with modulation level

(1) modulation level vs. Peak spectrum level

＊Spectrum level is in proportion to logarithm of Vm.

・$Vpeak = 0.55 - 0.65 \cdot LOG_{10}(Vm)$ [V]　　　　(2-1)

Here, Vpeak is the peak level of Fck spectrum,
Vm is the amplitude of modulation signal.

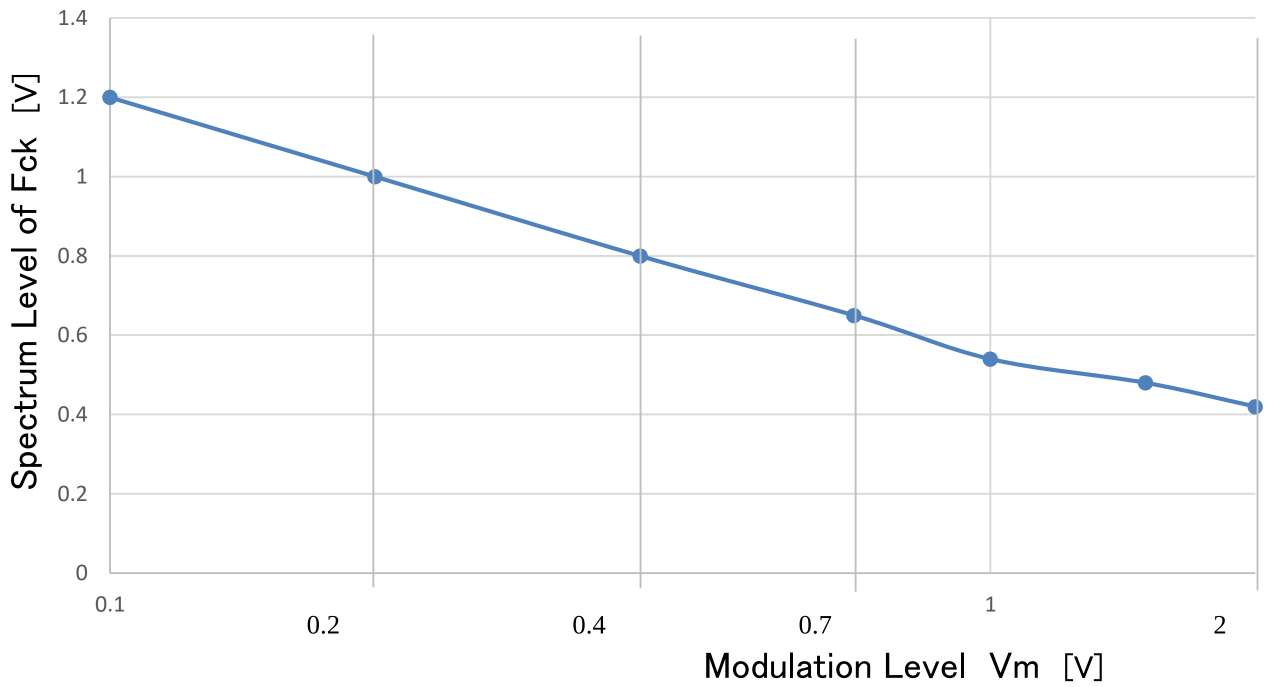

Fig.2-6 Modulation level vs. Spectrum level

(2) Relationship: modulation level vs. output ripple

∗ Output voltage ripple is changed by modulation signal level.
- Modulated ripple: caused by modulation signal
- Static ripple : caused by switching pulse

∗ Modulated output ripple is in proportion to modulation level.
- $\Delta Vo_m = 12.5 \cdot Vm$ [mV] (2-2)

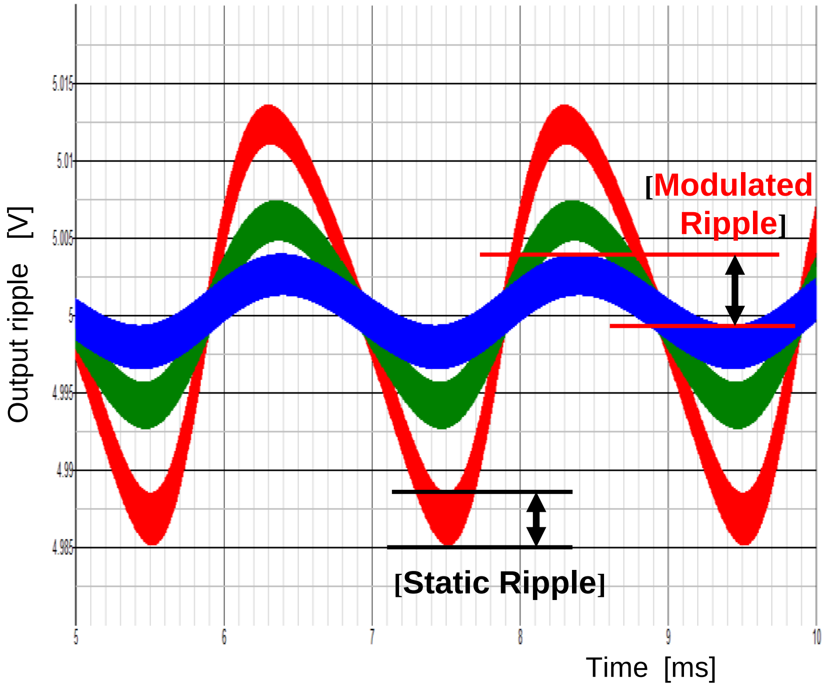

Fig.2-6 Modulated output ripple

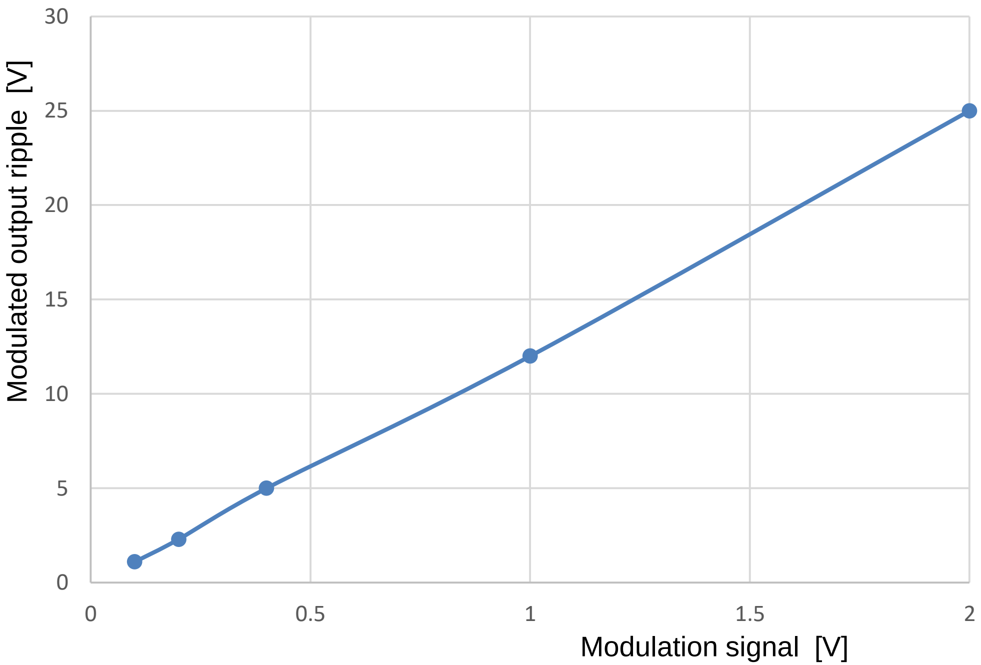

Fig.2-7 Modulation level vs. Output ripple

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3. Output Voltage Ripple Correction

3-1 Analysis of ripple correction method

- Consider the duty ratio of modulated SAW-tooth signal
  - ・Period of SAW signal is changed by modulation signal.
    But amplified output voltage keeps the level in a short time.
    ⇒ Pulse width W is not changed. ⇒ Duty ratio is changed.

$$D' = W/(T_o - \Delta T) = (W/T_o)/(1-\alpha) \fallingdotseq D_o(1+\alpha) \quad (3\text{-}1)$$

$\because \alpha = \Delta T/T_o < 0.01 \quad (=F_m/F_{ck})$

$$\Delta D = \alpha D_o = 2(V_m/V_b)/(F_{ck}/F_m) \quad (3\text{-}2)$$

Here, $F_{ck} = K \cdot (V_b + V_m)$

K [kHz/V] is the sensitivity of VCO

＊ ⊿D is the cause of the modulated ripple.

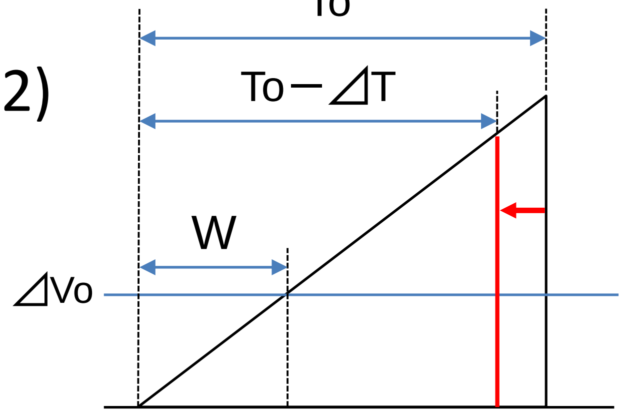

Fig. 3-1 Modulated SAW

＊Cancel ⊿D in the SAW-tooth generator
by compensating the slope of SAW-tooth signal

⇒ Pulse width W is changed into modulated width W'.

⇒ Compensated circuit: additional current source.

● Investigate conductance G which is controlled by Vm.

$$\Delta T=(T_{MAX}-T_{MIN})/\{Fo/(Fm/2)\}$$

$$\fallingdotseq 2(Vm/Vb)/(Fo/Fm)=2(Vm/Vb)To/Tm \qquad (3\text{-}3)$$

$$\therefore\ \alpha=\Delta T/To \fallingdotseq 2(Vm/Vb)/Tm \qquad (3\text{-}4)$$

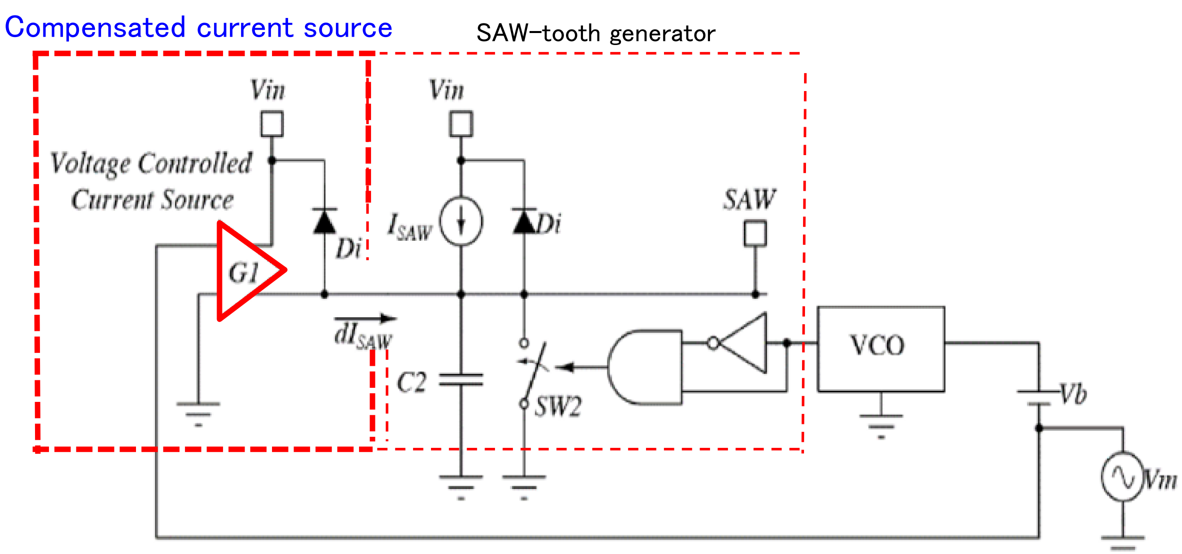

Fig.3-2 Compensated SAW generator

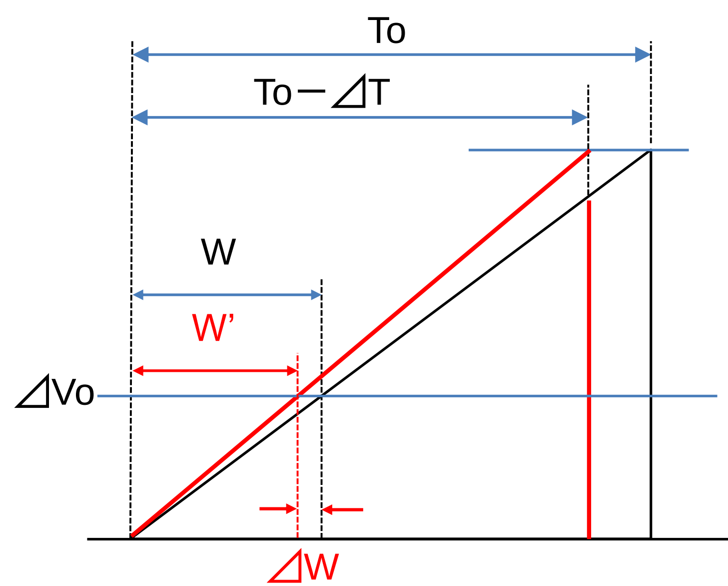

Fig.3-3 Compensation of duty

* To design conductance G, check the relationship Fm & Fck.

* The number of clock pulses in the half period of Fm is derived as Eq. (3-5).

* Set the additional current ΔI_{SAW}, derive the current ratio β.
⇒ Ratio β is equal to ratio α. ⇒ Set conductance G.

$$\alpha = \Delta T/To \fallingdotseq 2(Vm/Vb)/Tm \qquad (3\text{-}4)$$

$$N=(Tm/2)/Tck=0.5\cdot Fck/Fm \qquad (3\text{-}5)$$

$$\Delta I_{SAW} = G\cdot Vm \qquad (3\text{-}6)$$

$$\beta = (\Delta I_{SAW}/I_{SAW})/N = G\cdot Vm/(I_{SAW}N) \qquad (3\text{-}7)$$

* From Eq.(4)=Eq.(7),

$$2(Vm/Vb)/Tm = G\cdot Vm/(I_{SAW}N) \qquad (3\text{-}8)$$

・The conductance G is set bellow.

$$G = I_{SAW}/Vb\ [S] \qquad (3\text{-}9)$$

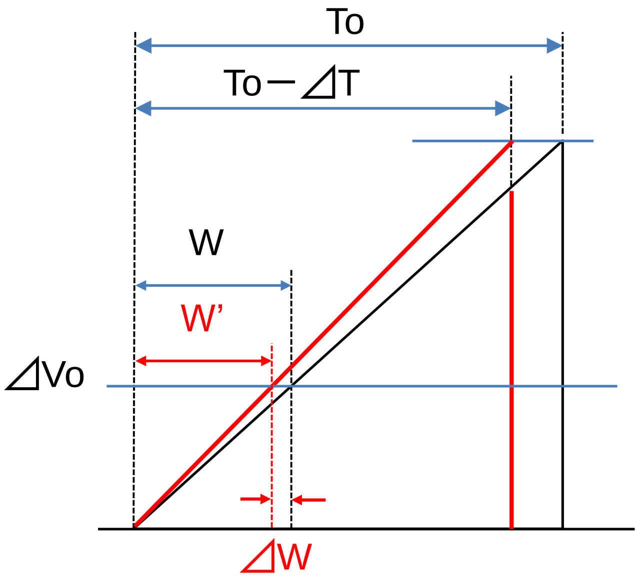

Fig.3-3 Compensation of duty

3-2 Simulation results

＊Theoretical conductance:

$G = I_{SAW} / Vb\ [S] = 500\ [uS]$

Additional current

Saw-tooth generator

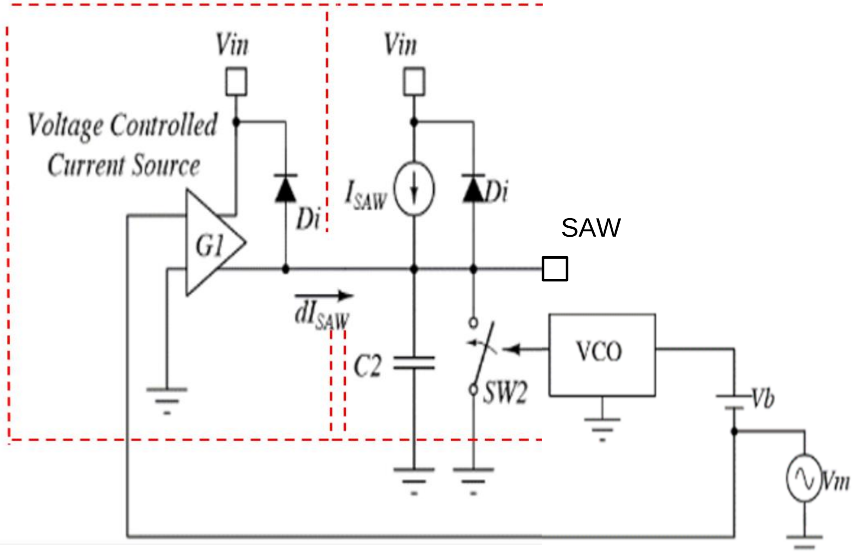

Fig.3-4 Circuit of new SAW generator

Table 2-1 Parameters of converter

1	**Input Voltage**	**Vin**	**12**	**[V]**
2	**Output Voltage**	**Vo**	**5.0**	**[V]**
3	**Output Current**	**Io**	**0.5**	**[A]**
4	**Inductance**	**Lo**	**200**	**[uH]**
5	**Capacitance**	**Co**	**220**	**[uF]**
6	**Clock Frequency**	**Fck**	**200**	**[kHz]**

Table 2-2 Parameters of VCO & SAW gen.

1	**Sensitivity**	**S**	**50**	**[kHz/V]**
2	**Base Voltage**	**Vb**	**4.0**	**[V]**
3	**Modulation V.**	**Vm**	**0.5～2.0**	**[V]**
4	**Modulation Freq.**	**Fm**	**0.5～2.1**	**[kHz]**
5	**SAW Current**	**I_{SAW}**	**2.0**	**[mA]**
6	**SAW Capacitance**	**C_{SAW}**	**1.2**	**[nF]**

● Relationship between G & Vo_m

＊Set modulation signal: Fm=2 kHz, Vm=2 V.

＊Modulated ripple with various G.

Modulated ripple is decreased when the conductance increase.

But G is larger than 500uS, phase of the ripple is reversed.

＊Show relationship in Fig. 6.

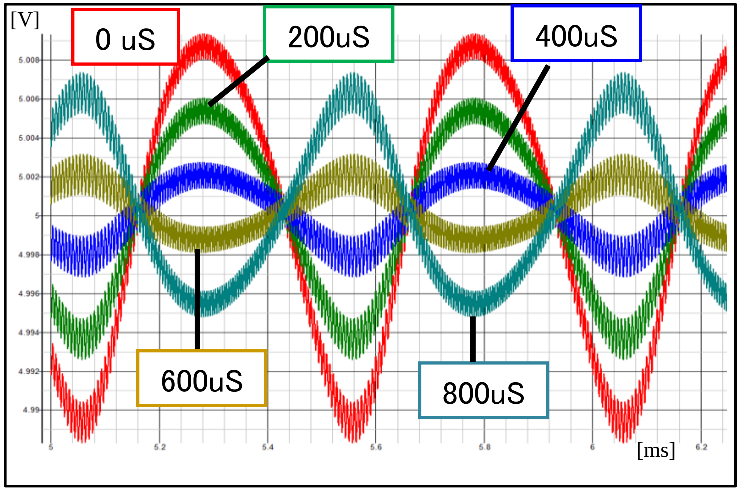

Fig.3-5 Ripples with various G

V_R=20－(31mV/800uS)･G [mV]

＊Best conductance is
G= 516 uS

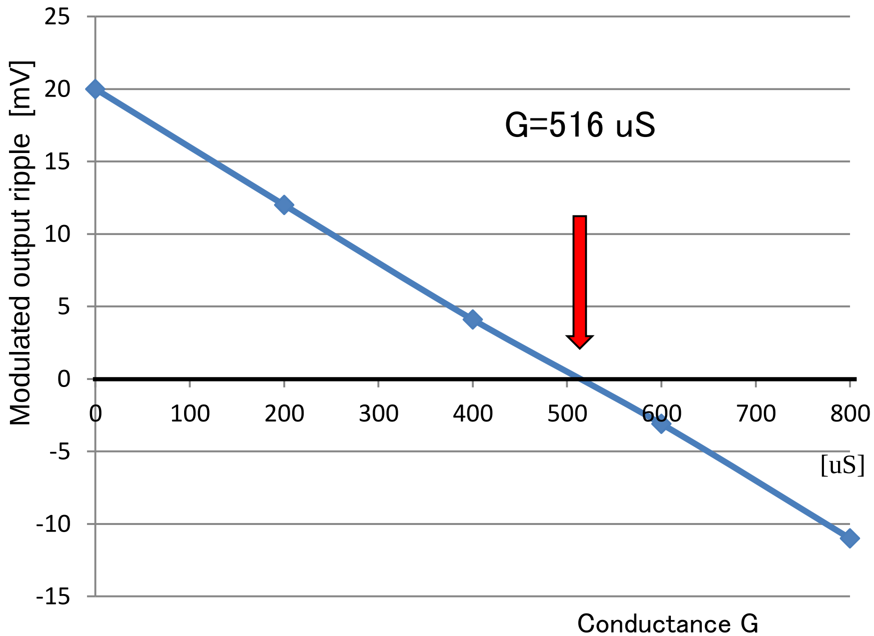

Fig. 3-6 Conductance vs. modulated ripple

● Simulation result (Fm=2.0kHz, Vm=2.0V, Sine Wave)

＊Best conductance is about

G=510 uS

・Modulated ripple is reduced from 20mV to 0.8mV (−28dB).

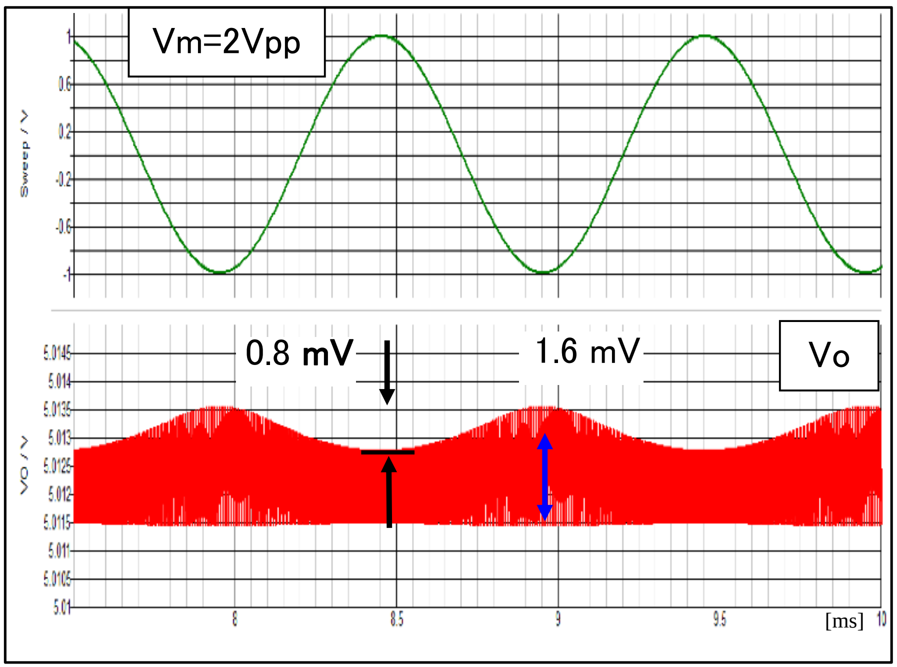

Fig. 3-7 Ripple with G=510 us

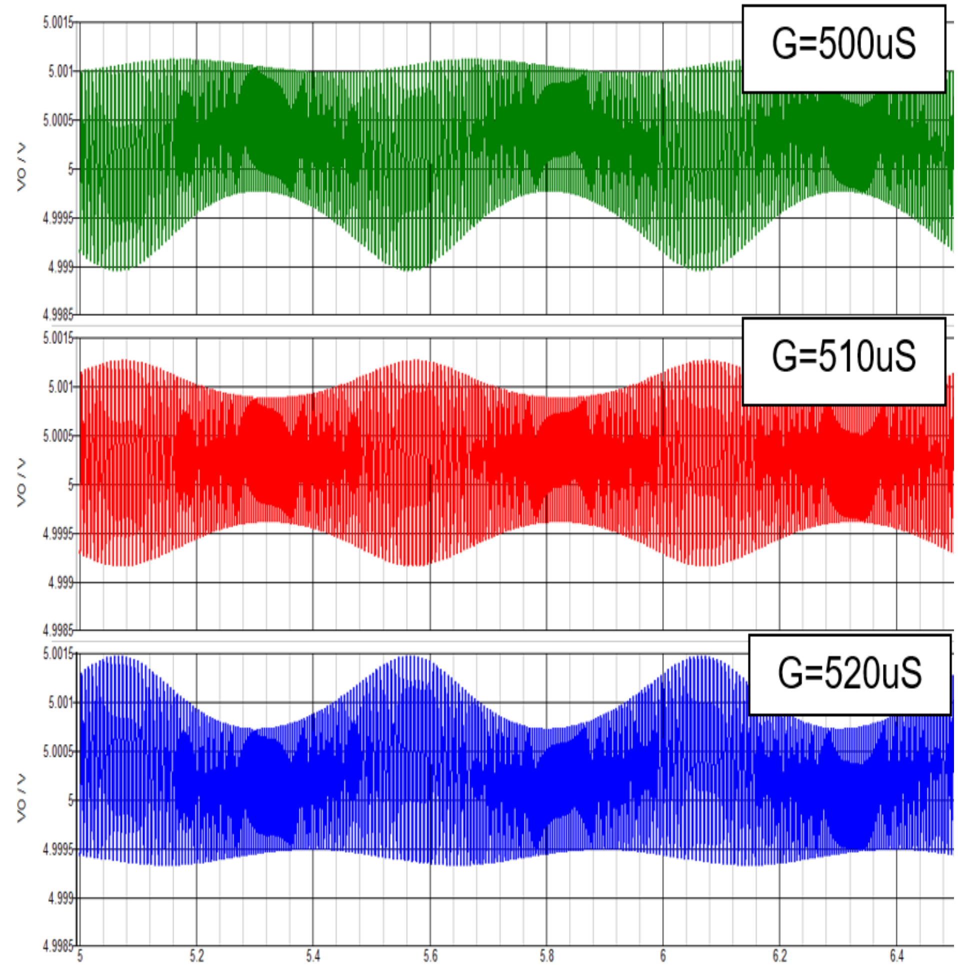

Fig.3-8 Ripples with various conductance

● Modulation signal : Triangular, Fm=2.0kHz, Vm=2.0V

＊Output ripple @ G=510 uS

Modulated ripple = 0.8mV, Static ripple = 2.7mV

＊Peak spectrum level: Vp = 0.65 V. (@ Fck = 200 kHz)

It is almost same as that of no ripple correction.

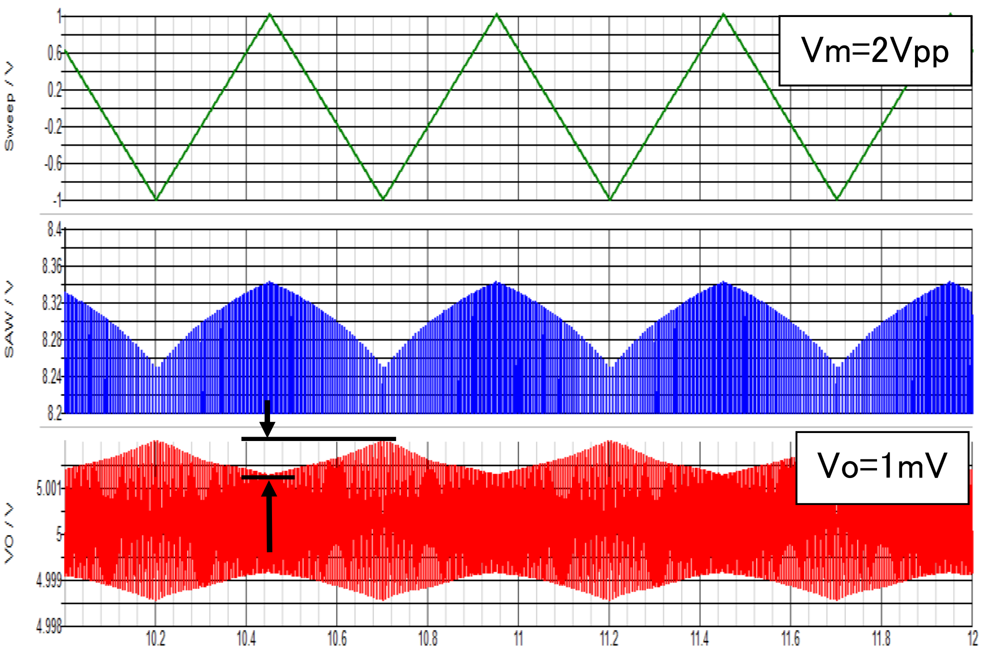

Fig. 3-9 Ripple with correction

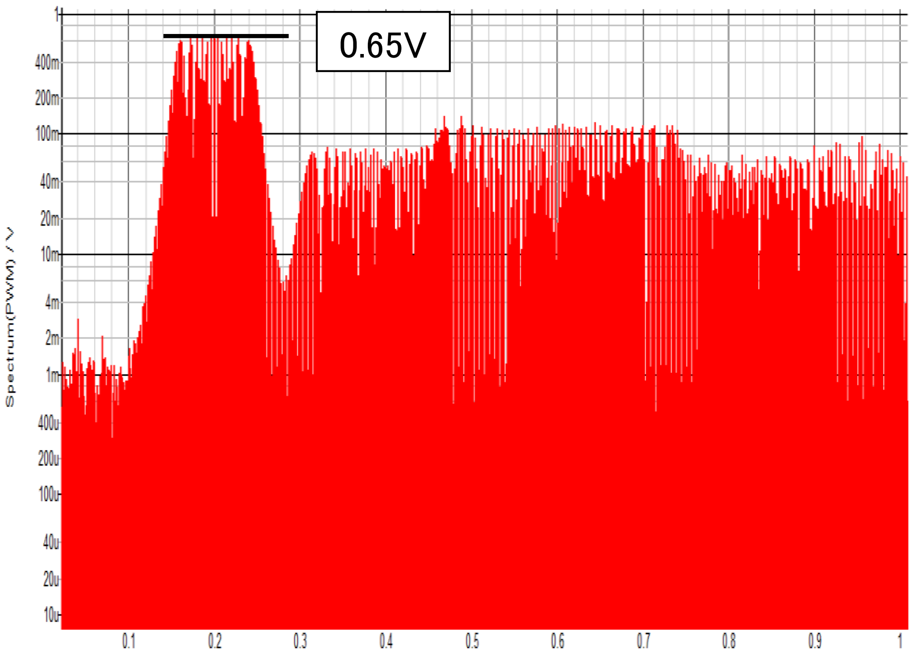

Fig. 3-10 Spectrum with correction

1) Transfer function: modulation signal to the output ripple
(Modulation signal : Triangular, Vm=2.0 V)

* Without correction: similar to closed-loop transfer function
* With correction : very low and constant

2) Spectrum level vs. Modulation Frequency Fm;

* Peak spectrum level is proportional to Modulation Frequency.
* Spectrum level is no concern with ripple correction.

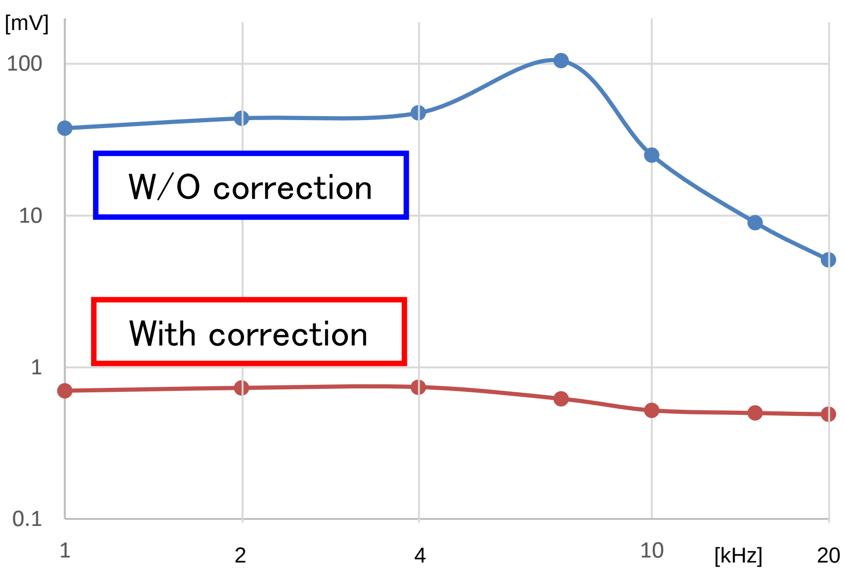

Fig. 3-11 Fm vs. Ripple

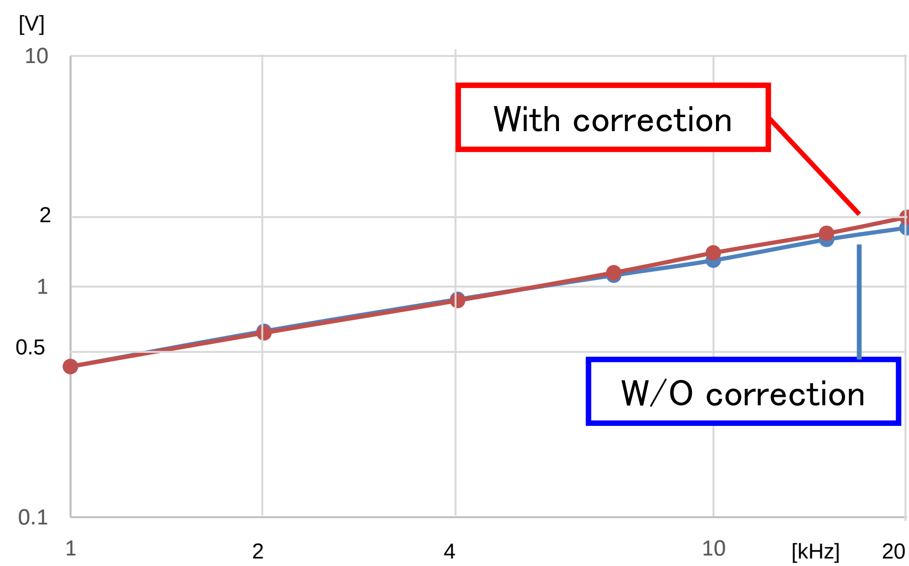

Fig. 3-12 Fm vs. Peak spectrum

Conclusion

1. Developed ripple correction method for SW converters in which spectrum level is reduced with frequency modulation.
2. Shown the relationship between modulation level and compensation level.
   - ・Conductance G for the additional current level is
     $G = I_{SAW}/Vb$ [S] : Here, I_{SAW} is current of SAW generator.
     Vb is the DC voltage of VCO.
3. Simulation results:
   Modulated ripple is corrected less than 1mV
   Peak spectrum level at clock Fck is reduced −28dB.

● Future work is to apply this correction method to another SW converters.
(ex. current mode switching converter)

Thank you for your kind attention!

Is there any question?