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Linearity Improvement Algorithms of Multi-bit ΔΣ DA Converter
- Combination of Unit Cell Re-ordering and DWA -

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Outline

- Research Background
- ΔΣDA converter
  - DWA*Algorithm (* Data-Weighted Averaging)
  - Unit Cell Re-ordering
- Simulation verification
  - 2nd - order ΔΣ DA converter : LP type
  - 2nd - order ΔΣ DA converter : HP type
- Conclusion

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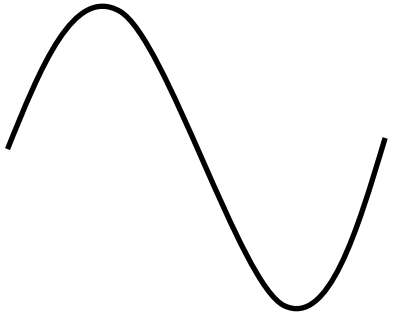
Research Background

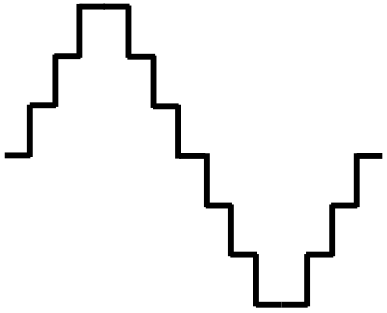
Analog signal



ADC

DAC

Digital signal

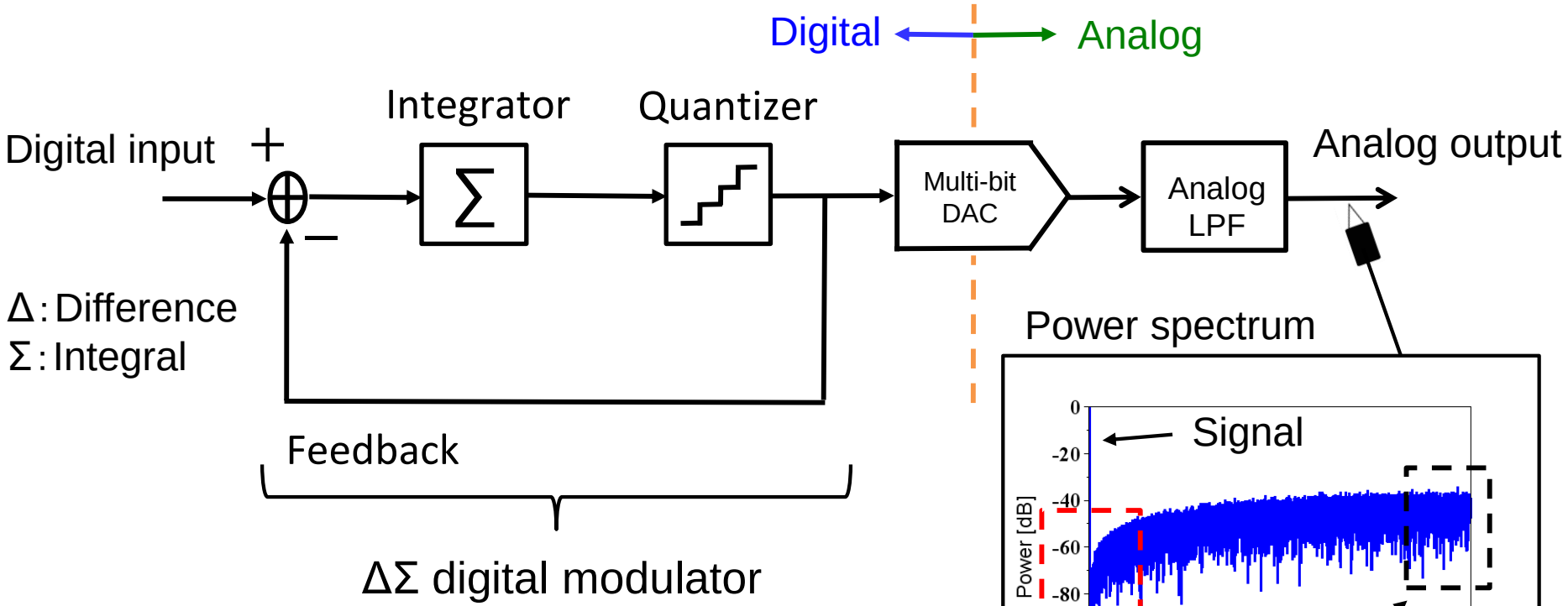


Continuous signal
Physical quantity existing in nature

Discrete signal
Binary number

- ΔΣ Digital-to-Analog Converter (ΔΣDAC) →Required
  - Mostly digital circuit
  - High-resolution ,High-linearity
  - DC signal , low frequency signal generation

ΔΣ DA Converter (LP model)

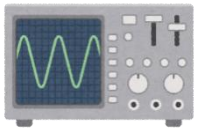


Power spectrum

Noise is decreased at low frequency
increased at high frequency

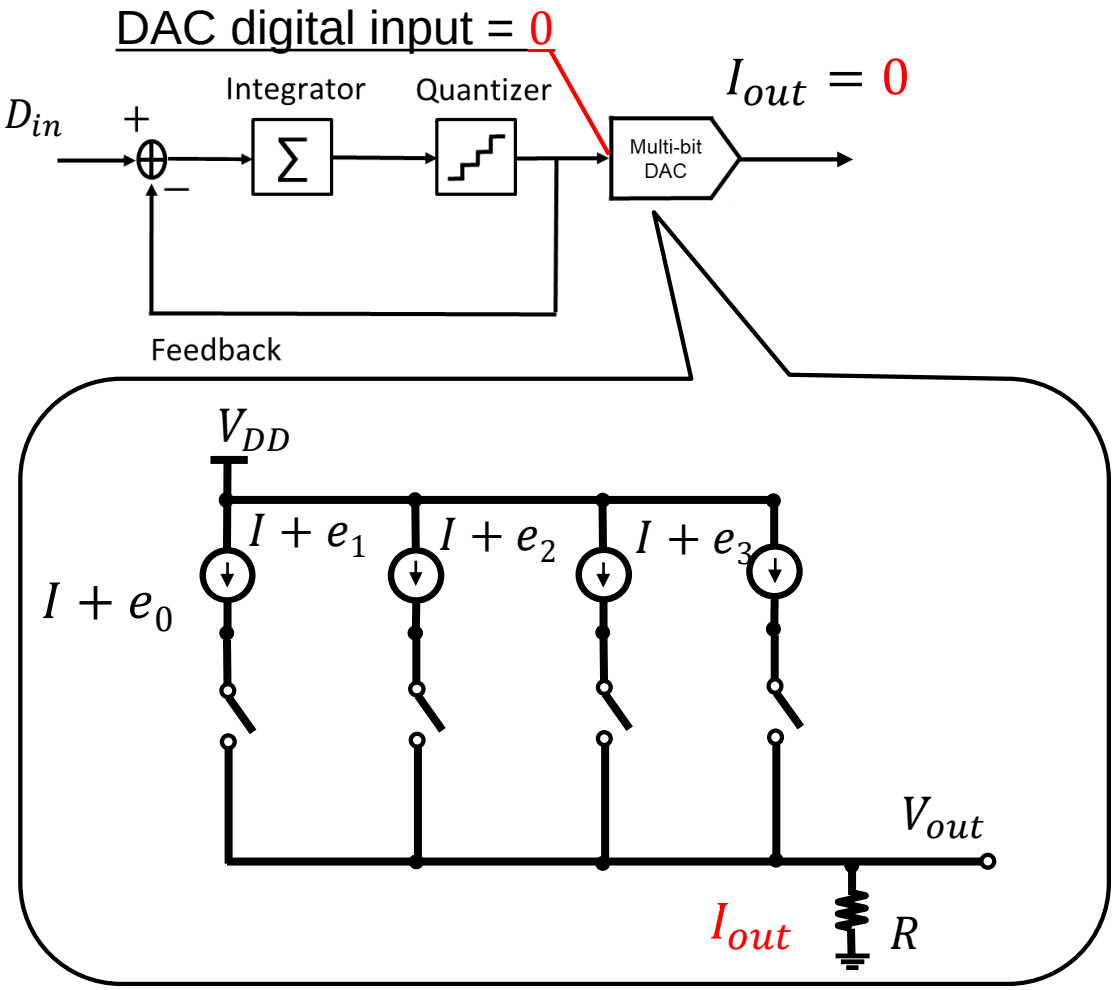
＜Usage＞

- Electric measurement



- Audio system

Multi-bit DAC Operation (1/3)



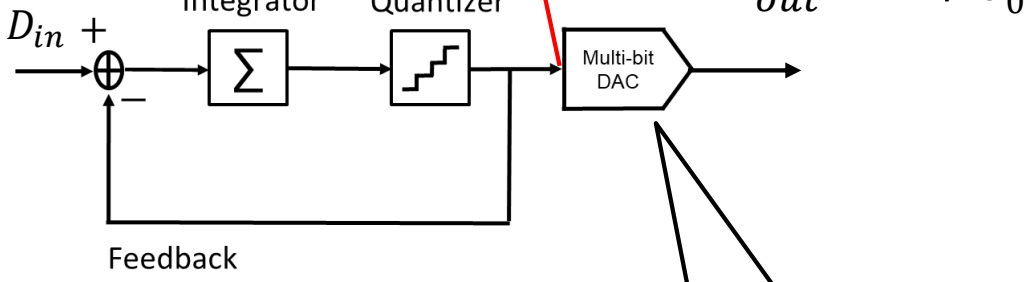
Current $I_k = I + e_k$

e_k : Current source mismatches

DAC Digital Input	I_{out}
0	0
1	
2	

Multi-bit DAC Operation (2/3)

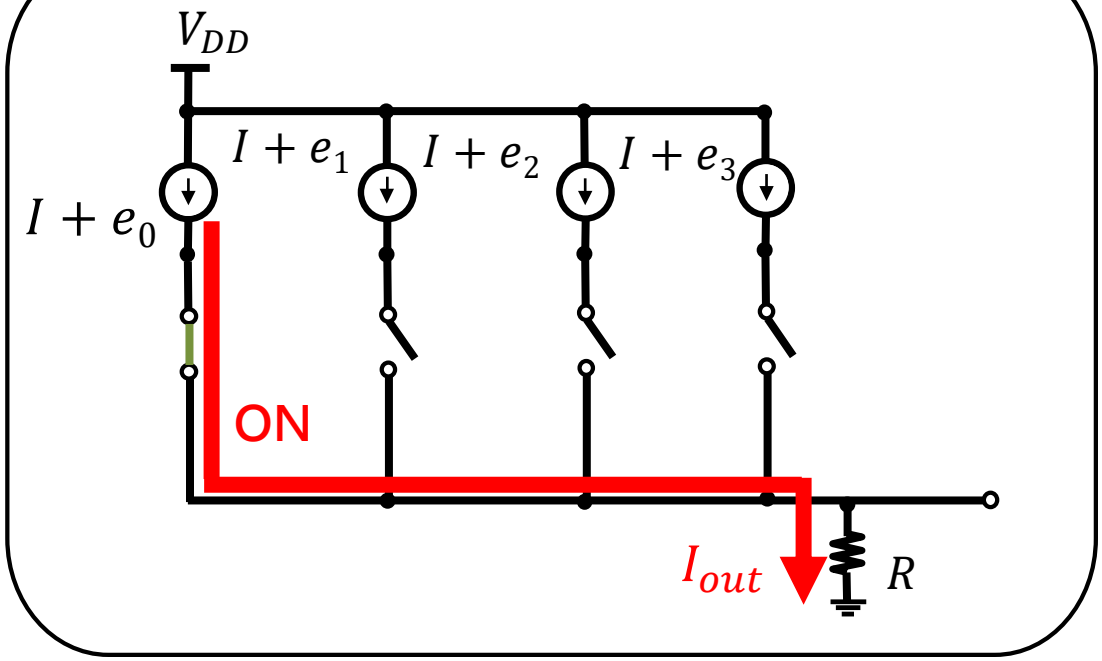
DAC digital input = 1



$I_{out} = I + e_0$

Current $I_k = I + e_k$

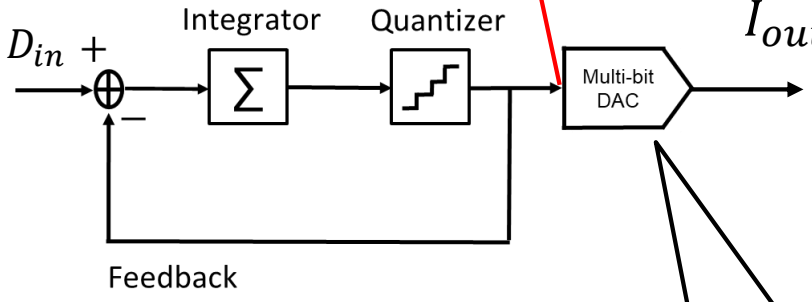
e_k : Current source mismatches



DAC Digital Input	I_{out}
0	0
1	$I + e_0$
2	

Multi-bit DAC Operation (2/3)

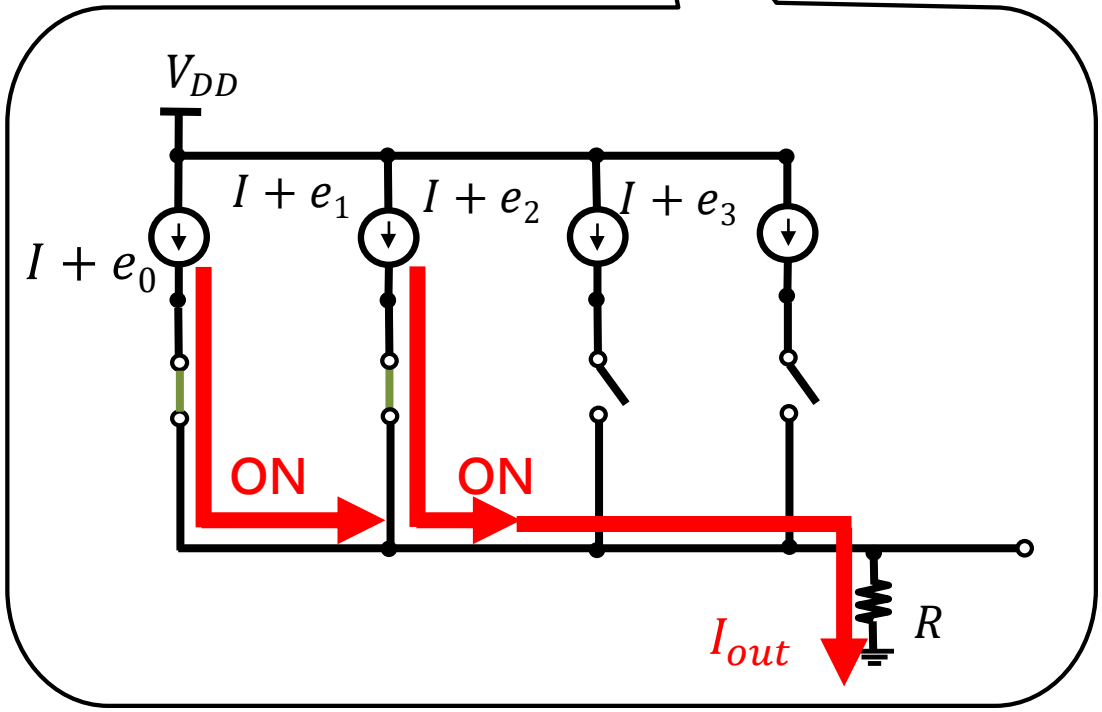
DAC digital input = 2



$$I_{out} = 2 \times I + (e_0 + e_1)$$

Current $I_k = I + e_k$

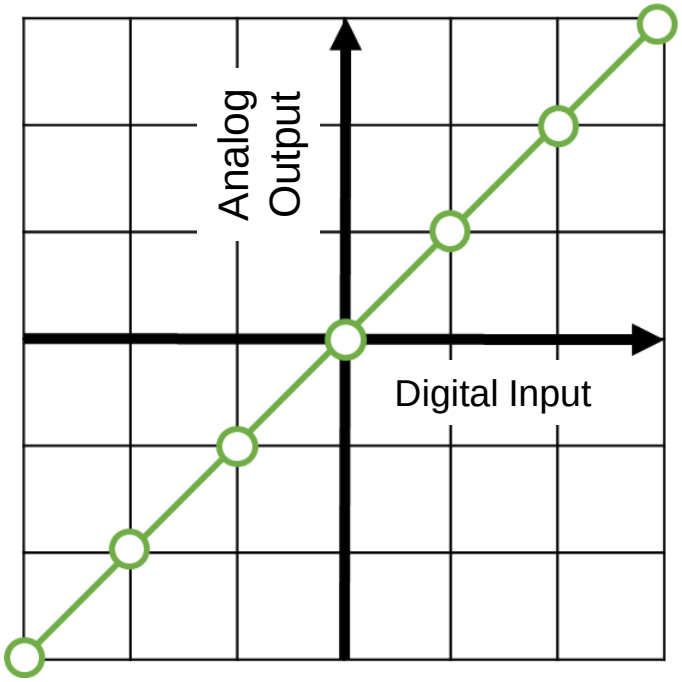
e_k : Current source mismatches



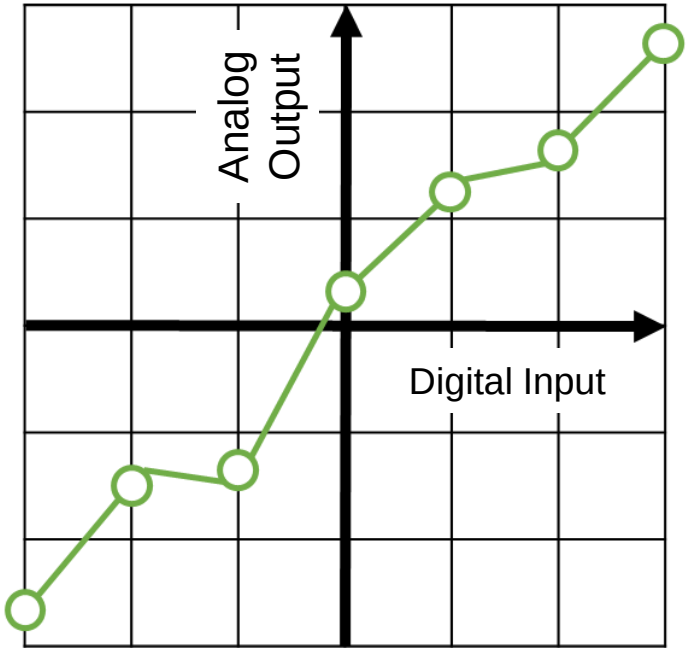
DAC input Digital	I_{out}
0	0
1	$I + e_0$
2	$2 \times I + (e_0 + e_1)$

Nonlinearity Problem of Multi-bit ΔΣ DAC

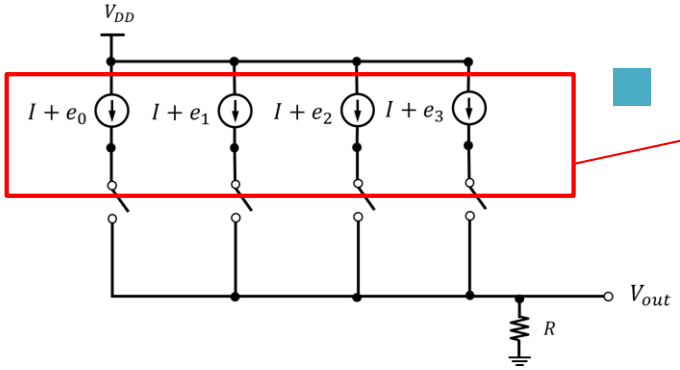
Ideal DAC



Real DAC



Multi-bit Output



- Currents are different due to process variation inside IC chip

- ΔΣDAC Nonlinearity Problem

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Unit Cell Current Average I

Unit cell current average : $I = \frac{1}{4}(I_0 + I_1 + I_2 + I_3)$

$$I_0 = I + e_0$$
$$I_1 = I + e_1$$
$$I_2 = I + e_2$$
$$I_3 = I + e_3$$

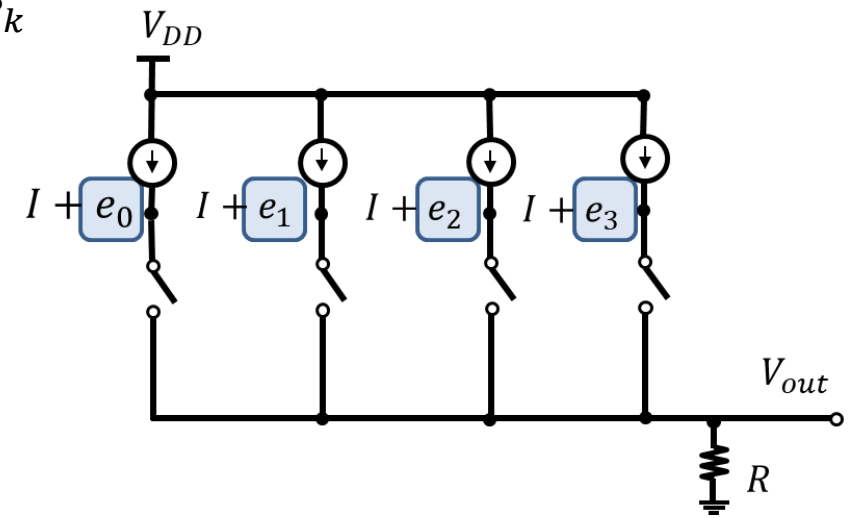
total sum

$$(I_0 + I_1 + I_2 + I_3) = 4I + (e_0 + e_1 + e_2 + e_3)$$

$$I = \frac{1}{4}(I_0 + I_1 + I_2 + I_3) - \frac{1}{4}(e_0 + e_1 + e_2 + e_3)$$

0

mismatch : e_k

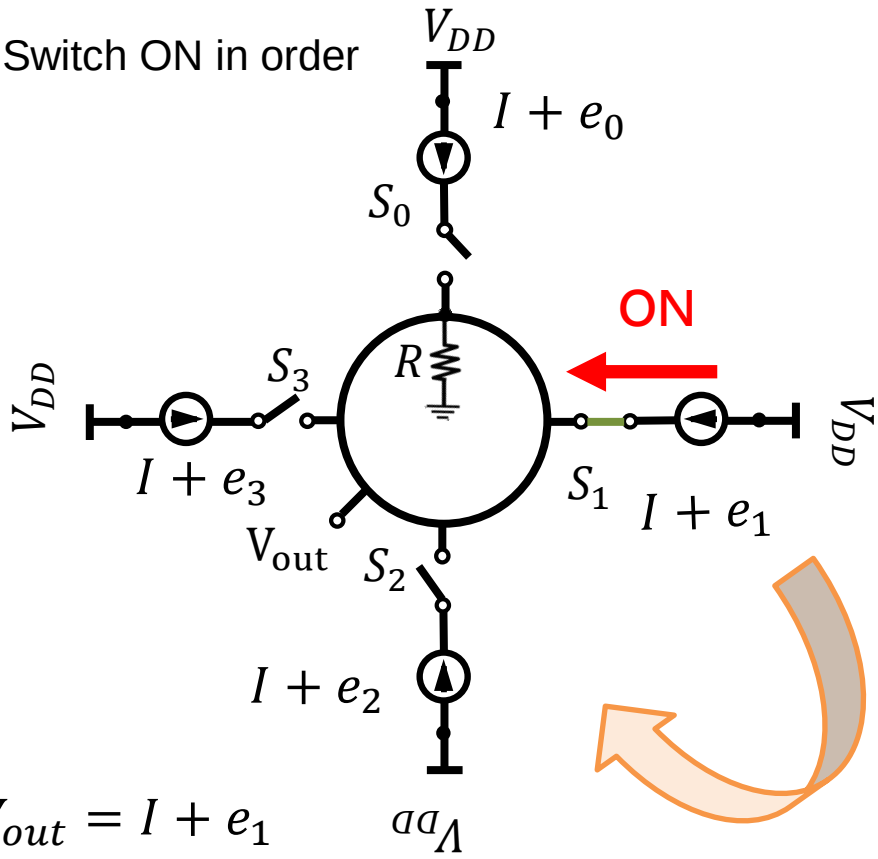


Multi-bit DAC + DWA I (1/2)

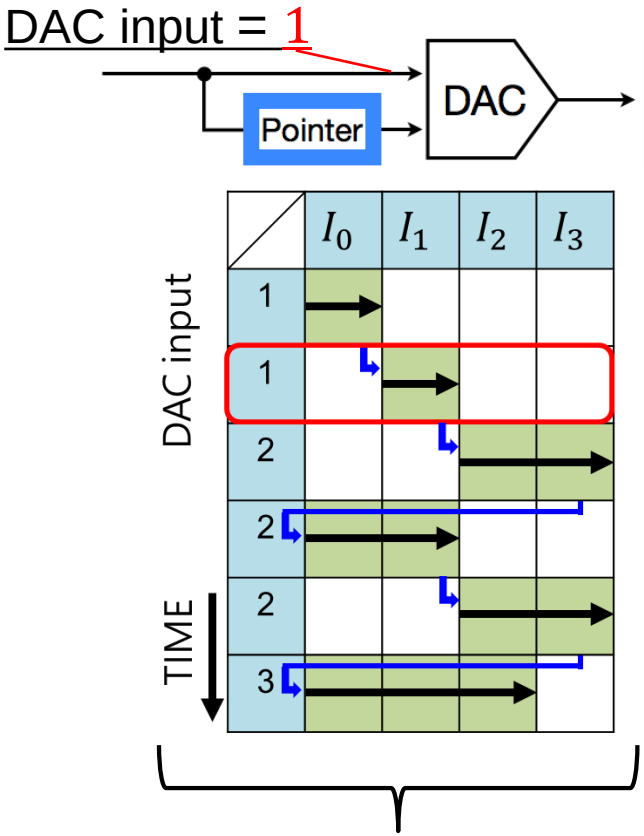
◆ DWA* DAC (*Data-Weighted Average)

$$I_{out} = I + e_1$$

※ Switch ON in order



$$V_{out} = I + e_1$$



Disperse mismatch of particular cells

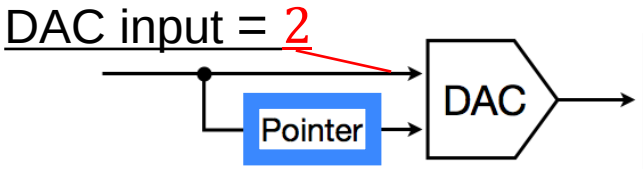
⇒Time-averaged

Linearity improvement ☺

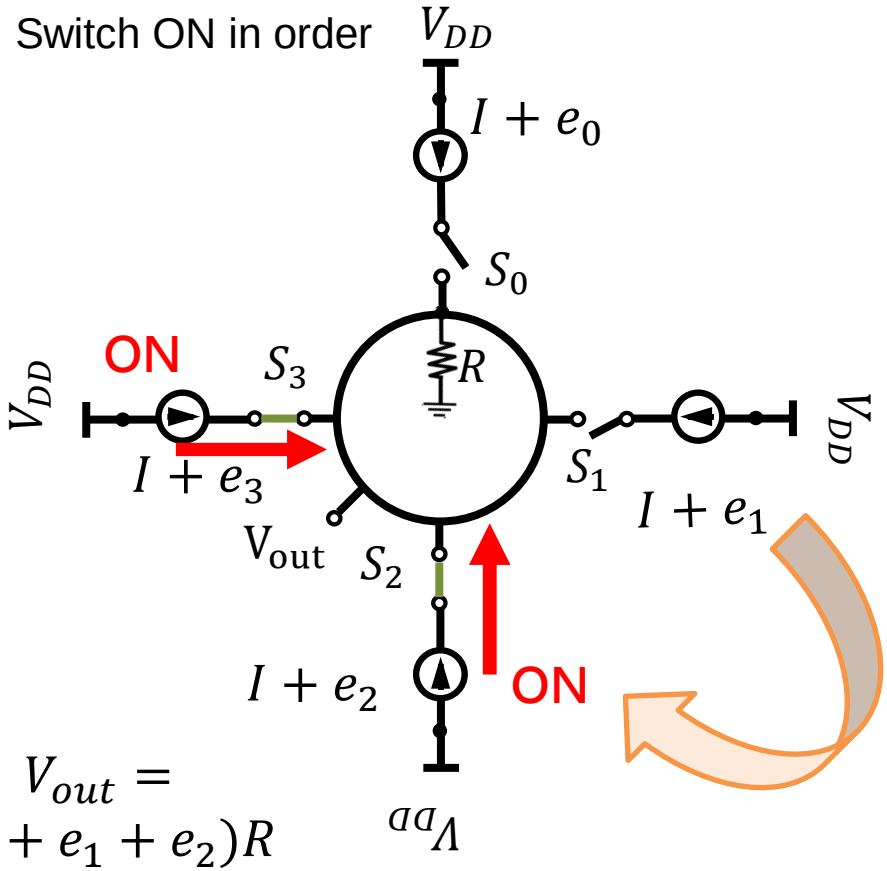
Multi-bit DAC + DWA I (2/2)

◆ DWA* DAC (*Data-Weighted Average)

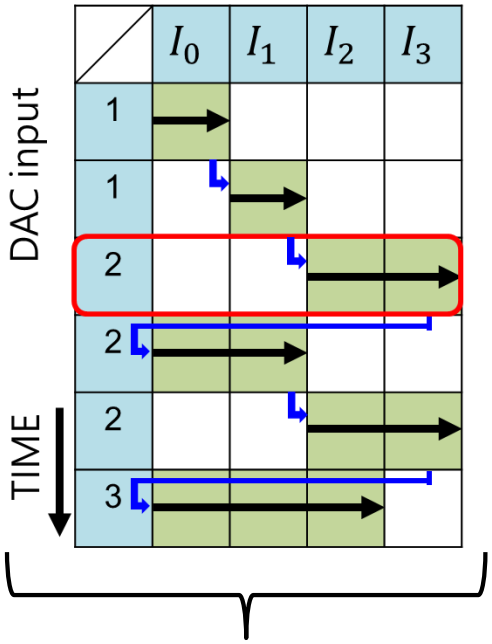
$$I_{out} = 2 \times I + (e_1 + e_2)$$



※ Switch ON in order



$$V_{out} = (2I + e_1 + e_2)R$$



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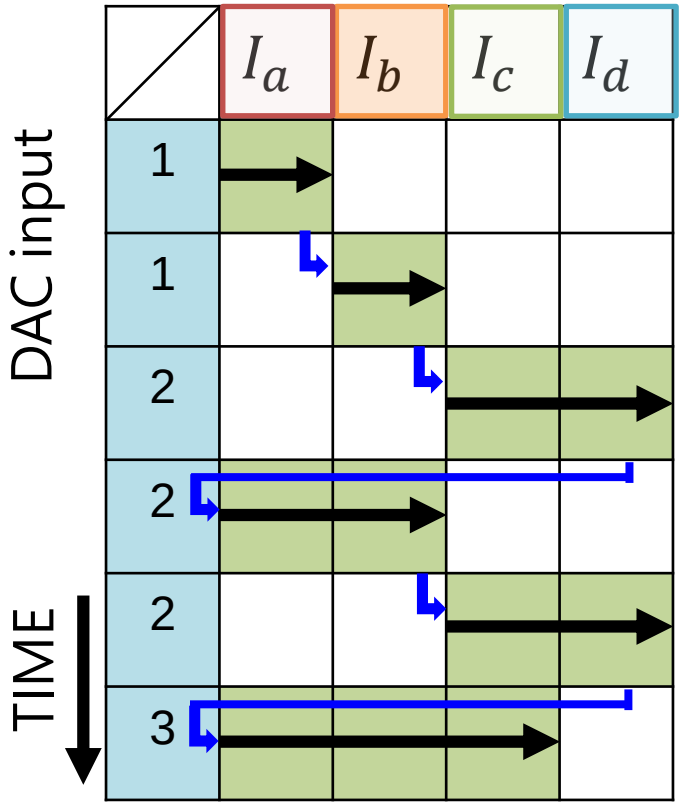
Unit Cell Re-ordering

Multi-bit ΔΣ DAC

Measure magnitude relation of current cells using comparator
Perform rearrangement in software



The smallest — The largest

$I_a < I_b < I_c < I_d$

1st 2nd 3rd 4th

Combination of four unit cells

There are 24 ways to sort at 5 levels

Analog output : $0, I, 2I, 3I, 4I$

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DAC Performance

SNDR

Signal-to-noise and distortion ratio

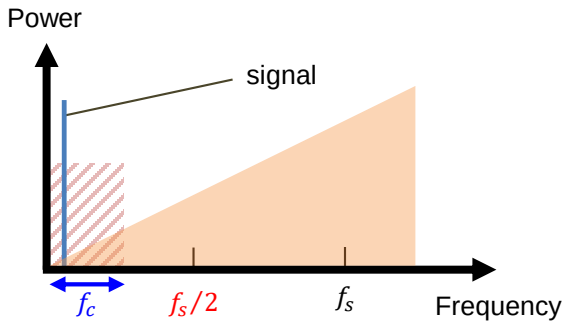
$$SNDR = \frac{P_{signal}}{P_{noise} + P_{distortion}}$$

P_{signal}:signal power P_{noise} : noise power $P_{distortion}$: distortion power

OSR

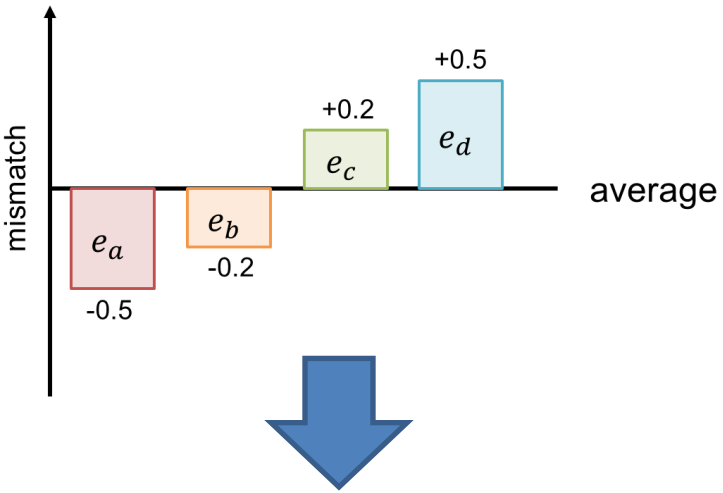
Over Sampling Ratio

$$OSR = \frac{\frac{f_s}{2}}{f_c}$$

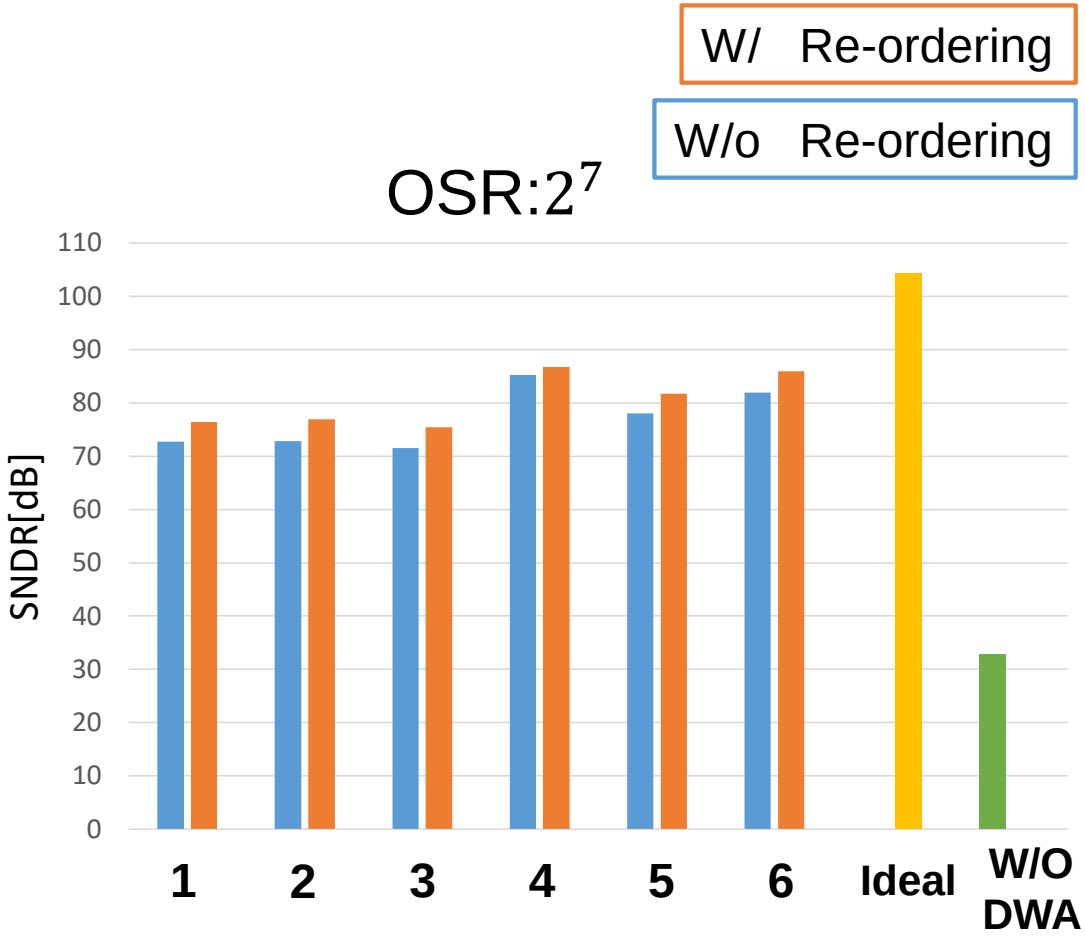


f_s : sampling frequency f_c : signal band

2nd-order ΔΣ DA Converter : LP type (1/3)



6 different mismatch patterns

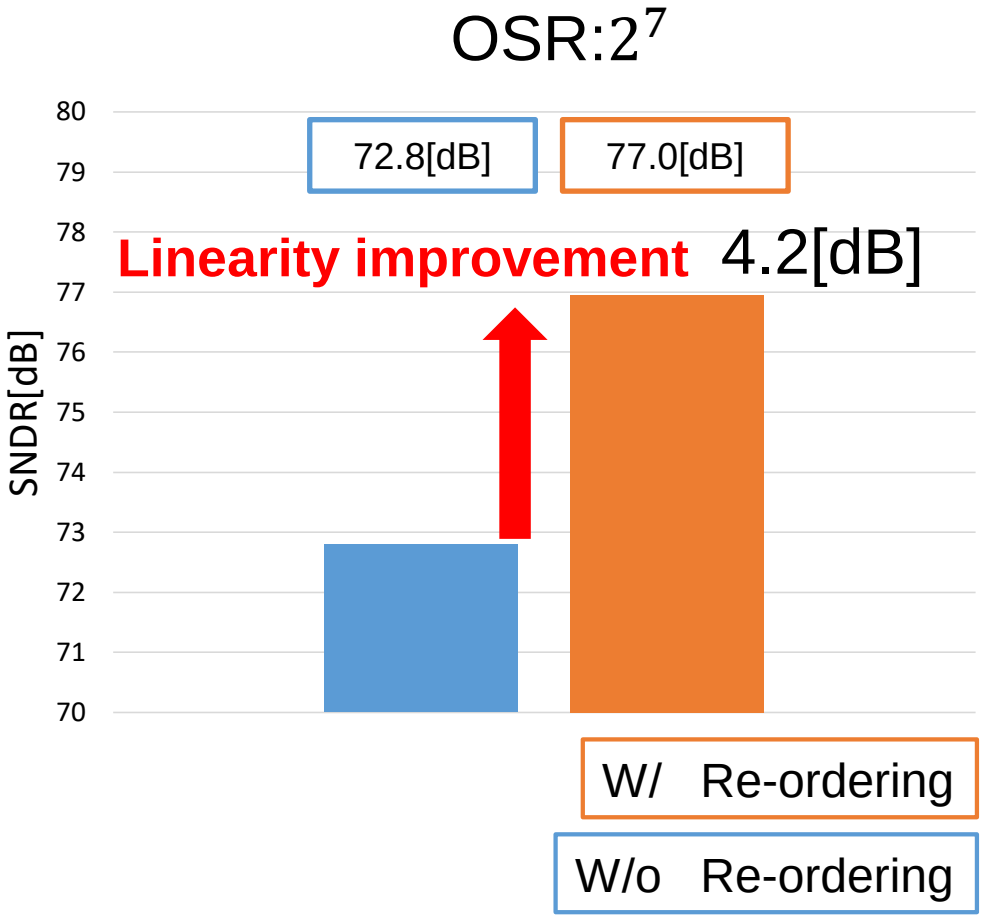


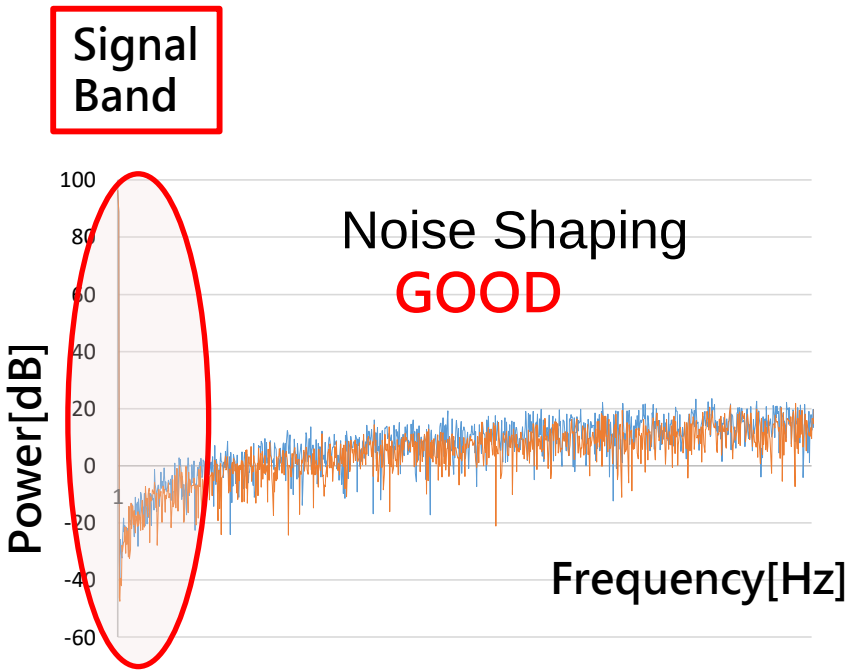
When 1st & 2nd , 2nd & 1st , 3rd & 4th , or 4th and 3rd
in order of combination is included

⇒ Good SNDR

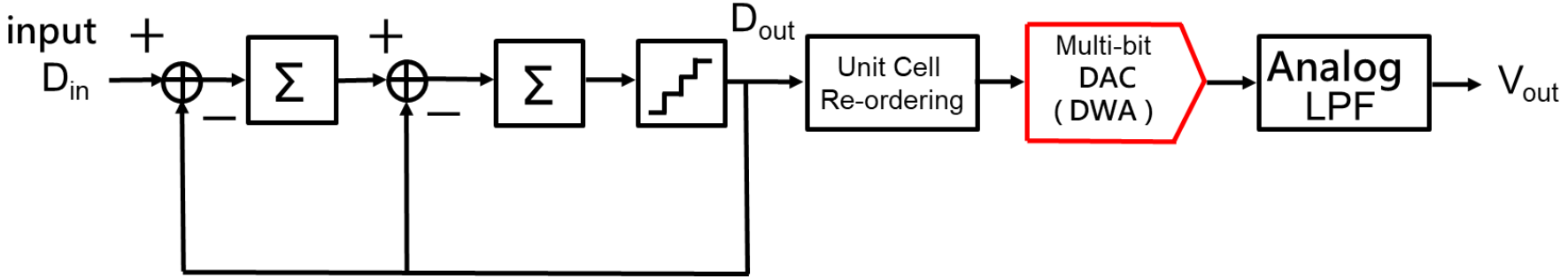
2nd-order ΔΣ DA Converter : LP type (2/3)

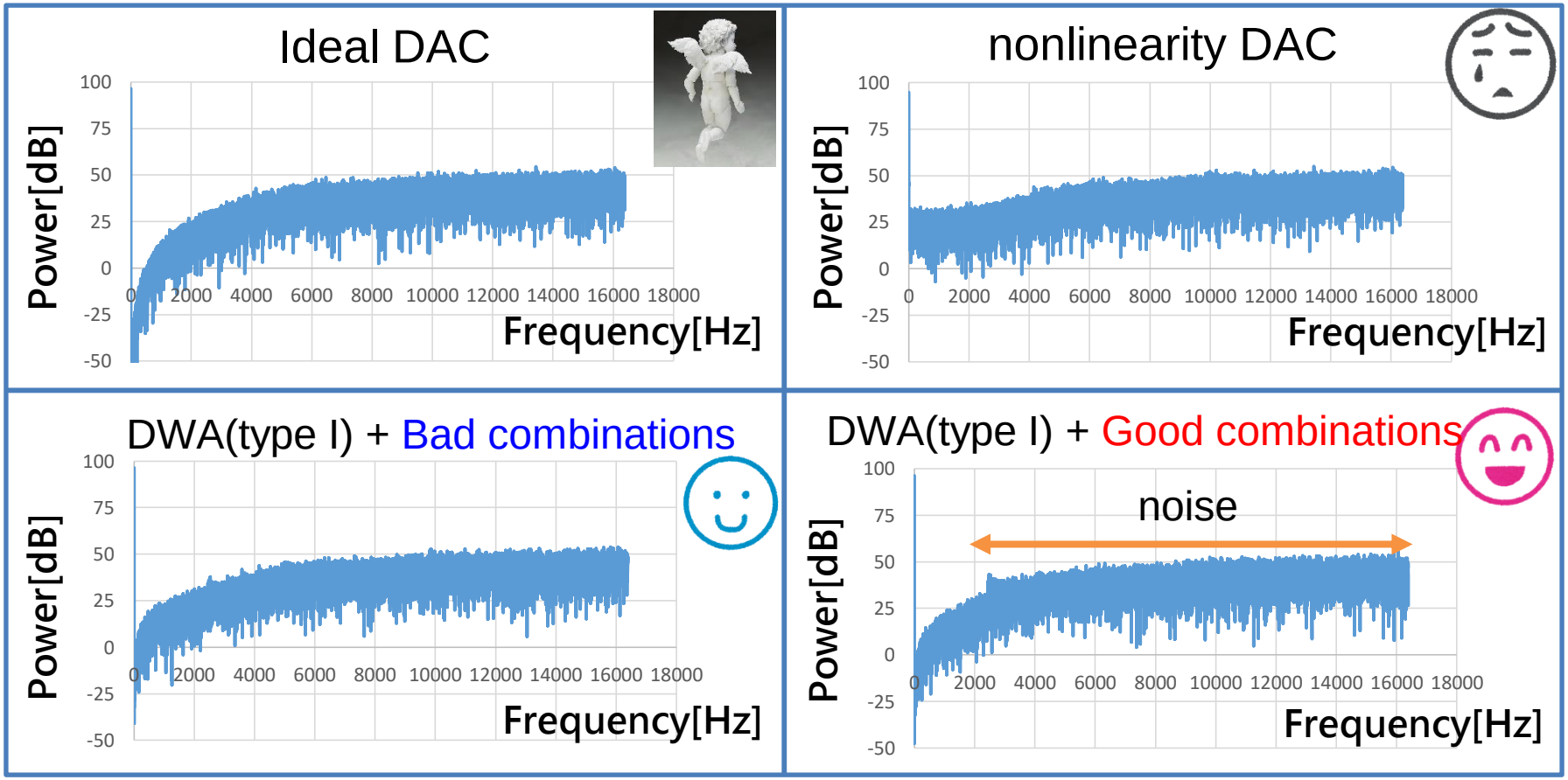
Deviation from the average current among unit current cells
Pattern 2





2nd-order ΔΣ DA Converter : LP type (3/3)





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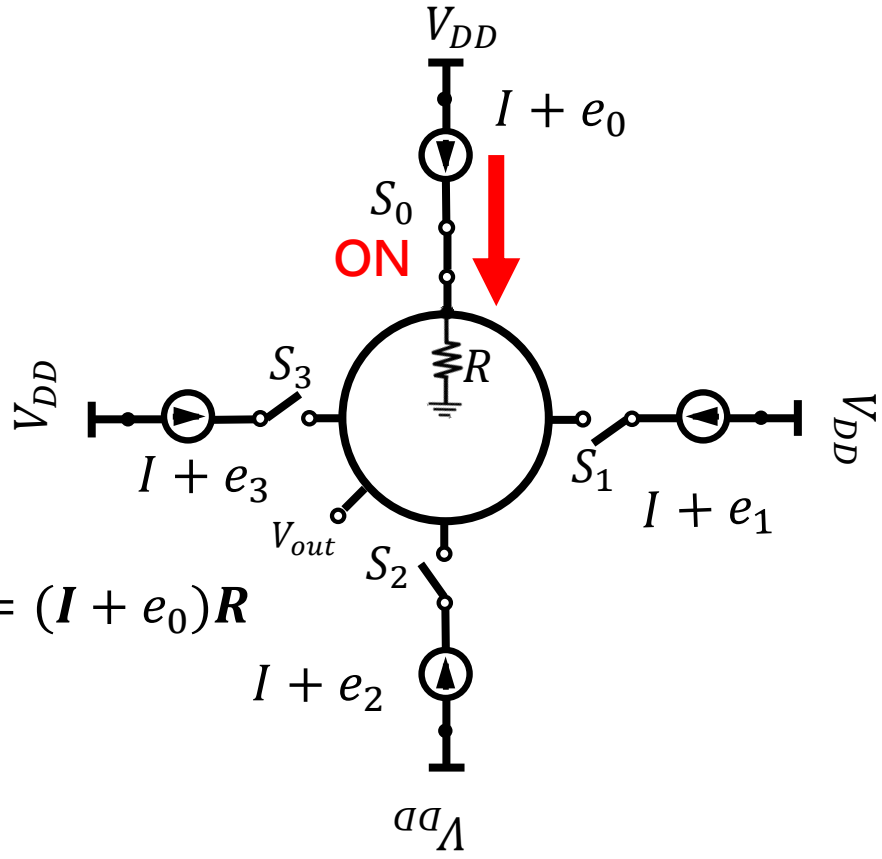
Multi-bit DAC + DWA II (1/2)

◆ DWA* II DAC (*Data-Weighted Average)

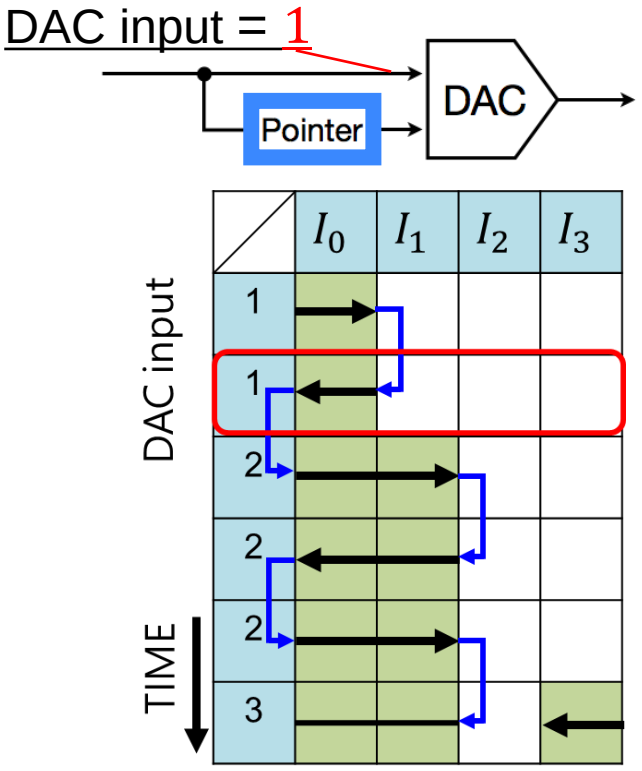
DAC input = 1

$I_{out} = I + e_0$

※ Switch ON in order



$\boldsymbol{V_{out} = (I + e_0)R}$



Back and forth

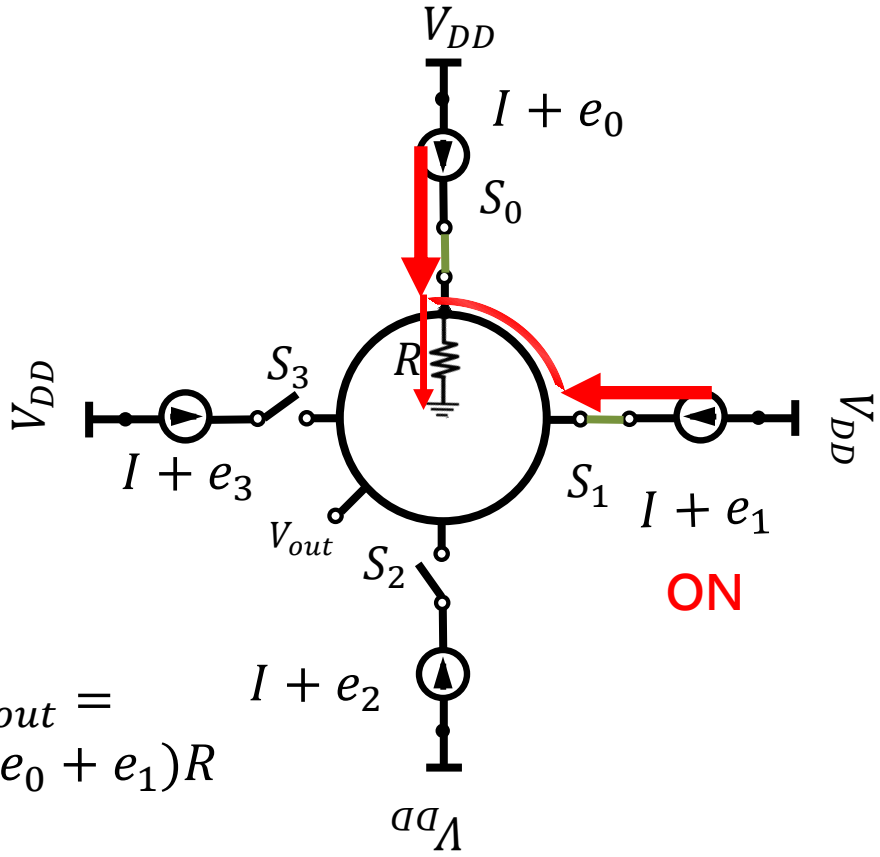
Multi-bit DAC + DWA II (2/2)

◆ DWA* II DAC (*Data-Weighted Average)

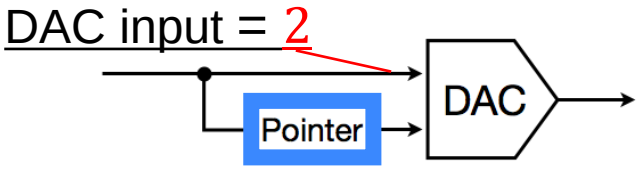
DAC input = 2

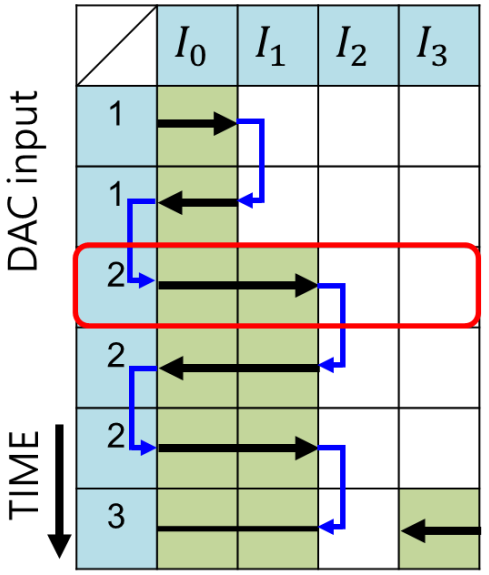
$I_{out} = 2 \times I + (e_0 + e_1)$

※ Switch ON in order



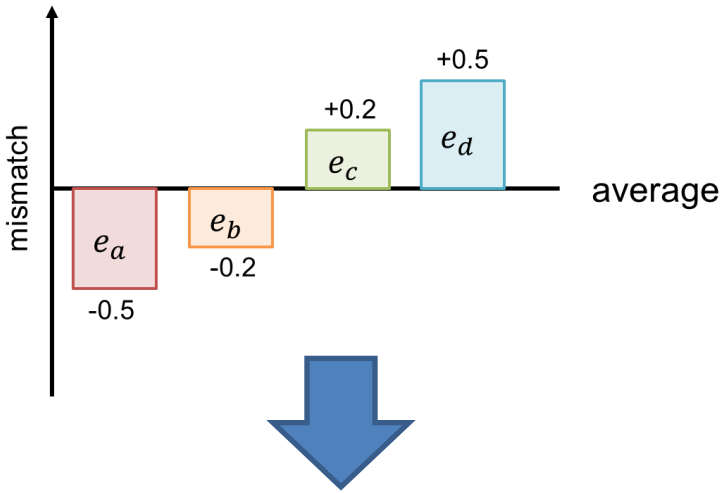
$V_{out} = (2I + e_0 + e_1)R$



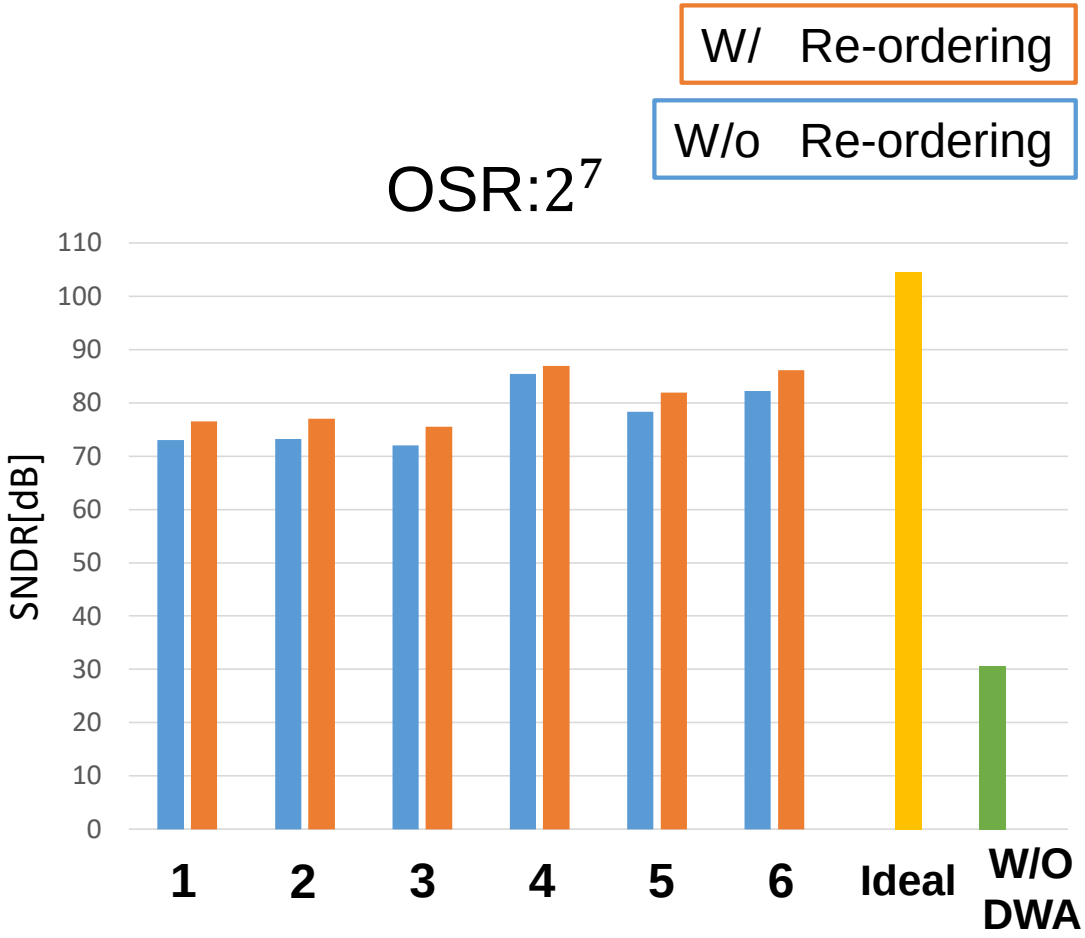


Back and forth

2nd-order ΔΣ DA Converter : HP type (1/3)



6 different mismatch patterns



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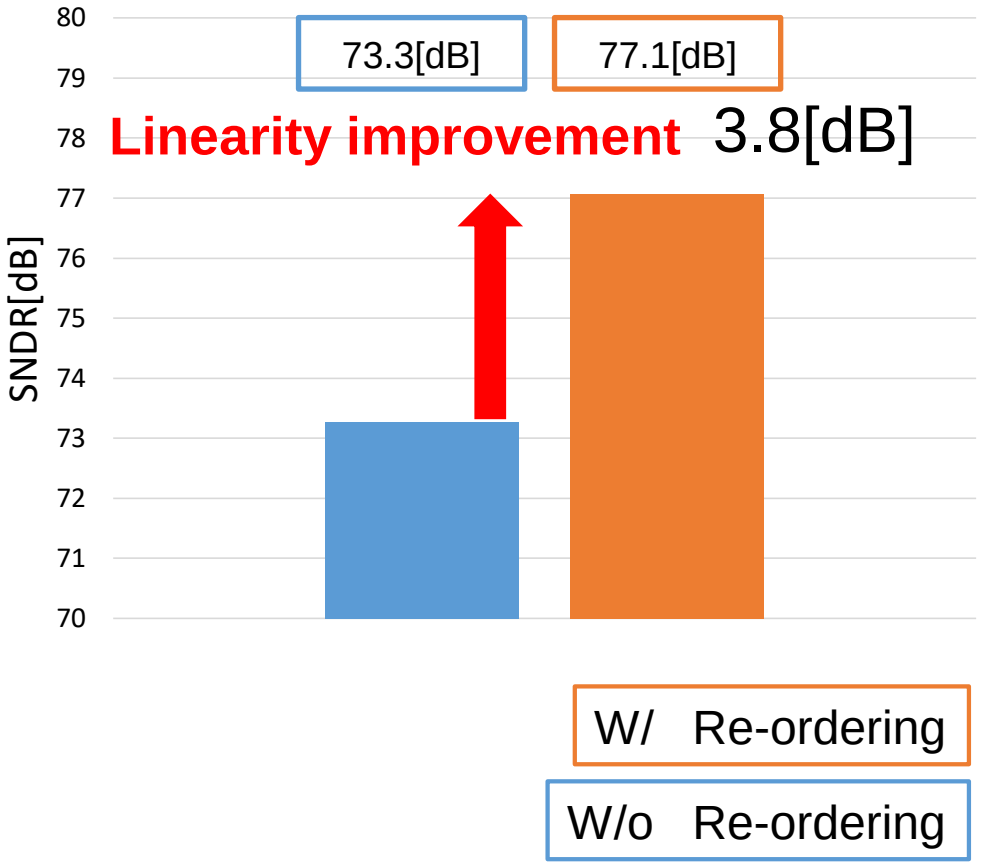
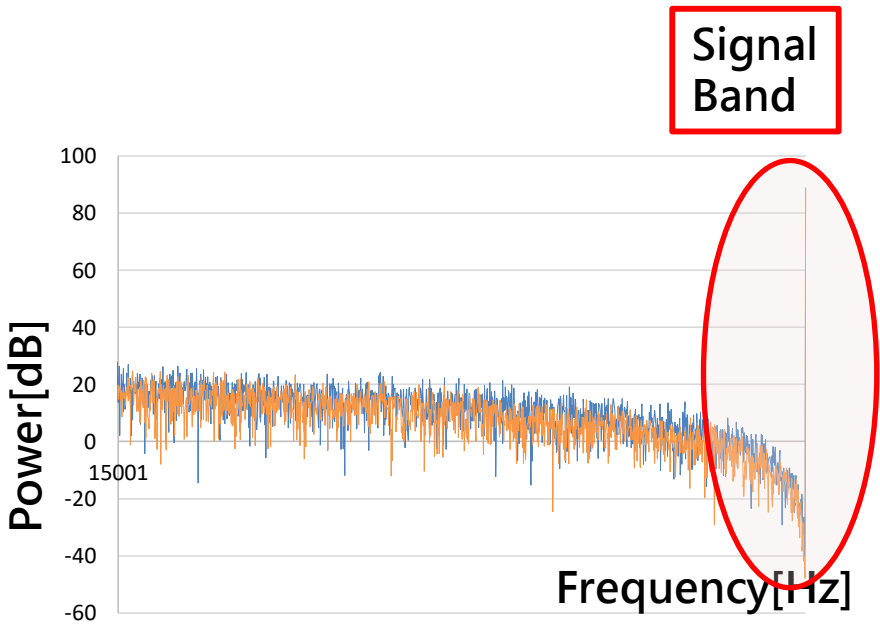
⇒ Good SNDR

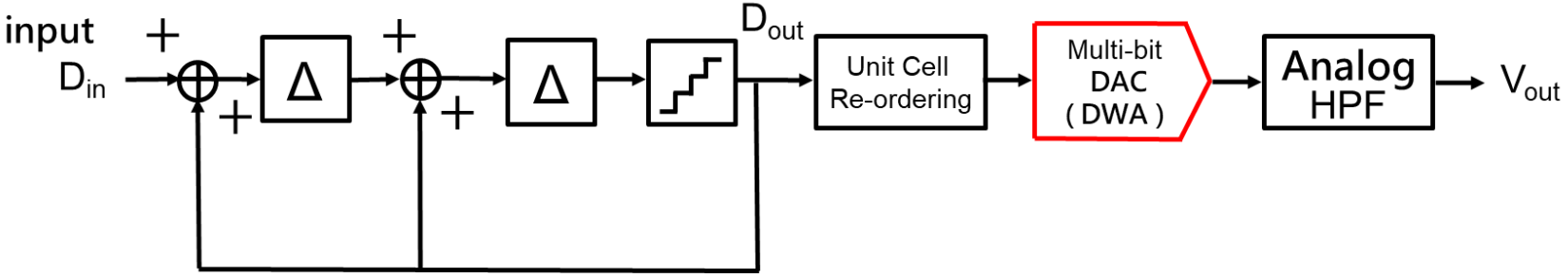
2nd-order ΔΣ DA Converter : HP type (2/3)

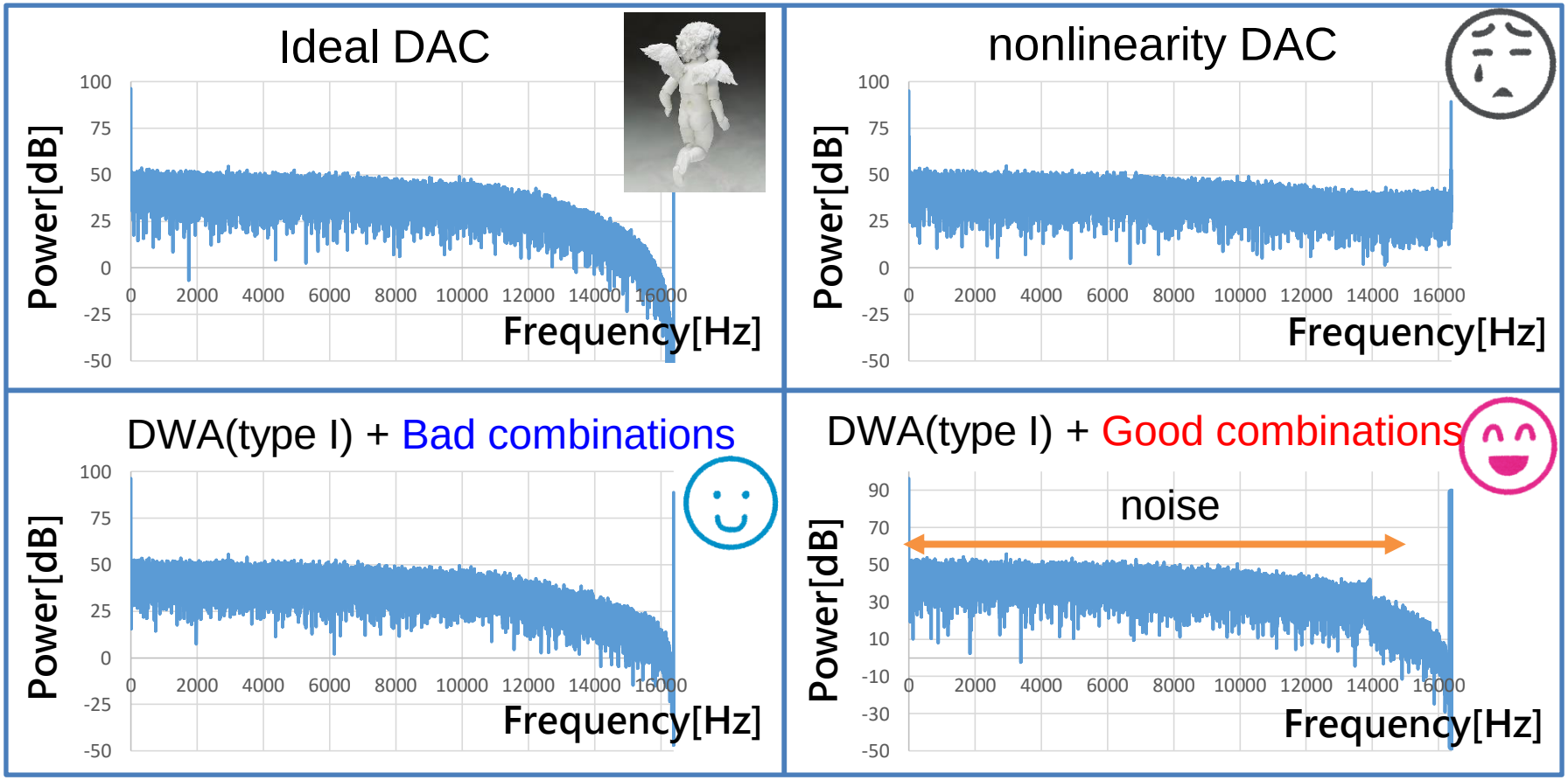
Deviation from the average current among unit current cells
Pattern 2





2nd-order ΔΣ DA Converter : HP type (3/3)





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Conclusion

- Multi-bit ΔΣ DAC

  Conventional:

  Not using anything or using only DWA

  Proposed:

  Using both unit cell re-ordering and DWA

  finding

  Significant linearity improvement