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Linearity Improvement Algorithms of Multi-bit ΔΣ DA Converter –Combination of Unit Cell Re-ordering and DWA

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Abstract. This paper presents several linearity improvement algorithms for multi-bit ΔΣ digital-to-analog converters (DACs), utilizing digital signal processing (DSP) techniques. The ΔΣ DACs are used for electronic measurement and automatic test equipment as well as audio systems, for their easy implementation of high resolution. However, their multi-bit configuration causes overall DAC non-linearity due to characteristics mismatches among multiple unit cells, even though they can be implemented with small hardware and power. It is known that the effect of this can be alleviated by the unit cell cyclic selection method. Furthermore, it showed that the linearity is further improved by executing the cyclic selection method (data weighted averaging: DWA) after rearranging the unit cell circuits. The proposed ΔΣDACs use DSP techniques and hence they are easy to implement.

1. Introduction

A ΔΣ DA converter consists of mostly digital circuits, and it is widely used for electronic measurement and test equipment as well as audio systems because it can produce highly linear DC and low frequency signal with high resolution. A multi-bit DAC has three merits. (i) High Signal-to Quantization Noise Ratio (SQNR) with the same oversampling ratio. (ii) Improvement of loop stability for high order modulators. (iii) Relaxed requirements of following analog filter requirements [1, 2].

Notice that a single-bit DAC is inherently linear, whereas the multi-bit configuration causes overall DAC non-linearity due to characteristics mismatches among multiple unit cells, even though the multi-bit ΔΣ DAC can be implemented with small hardware and power [3, 4, 5, 6, 7, 8, 9, 10, 11]. Then we have investigated a unit cell reordering method and a unit cell cyclic selection (data weighted averaging: DWA) as well as their combination to improve the overall ΔΣ DAC linearity. We show Scilab simulation results for low-pass (LP) and high-pass (HP) ΔΣ DA modulators to demonstrate the effectiveness of our proposed method.

2. ΔΣ DA modulator

2.1 ΔΣ DA modulator configuration

A LP ΔΣ DA modulator consists of all digital circuits with feedback configuration using an integrator and a truncator (Fig. 1). The error signal is accumulated at the integrator, and its MSB is the truncator output as well as the ΔΣ modulator output. Also the truncator output is fed back to the input. It is known in [1, 2] that the output power spectrum is noise-shaped; quantization noise is reduced at low frequency while increased at high frequency (Fig. 2).

Similarly, Fig. 3 shows a HP ΔΣ DA modulator. Compared with the LP ΔΣ DA modulator (Fig. 1), plus and minus signs at the feedback summation are reversed. Fig. 4 indicates that the output power spectrum is noise-shaped; quantization noise is reduced at high frequency while increased at low frequency.

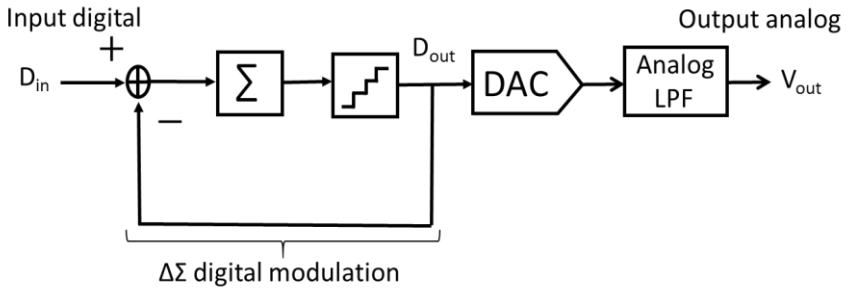


Fig. 1. Block diagram of the first-order LP ΔΣ DA converter.

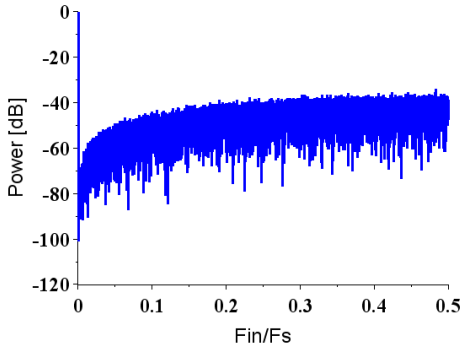


Fig. 2. Power spectrum of the LP ΔΣ modulator output.
(Input sine wave amplitude: 1, normalized frequency: 1)

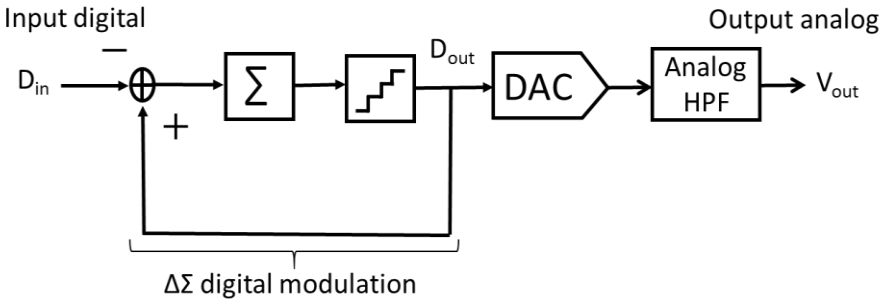


Fig. 3. Block diagram of the first-order HP ΔΣ DA converter.

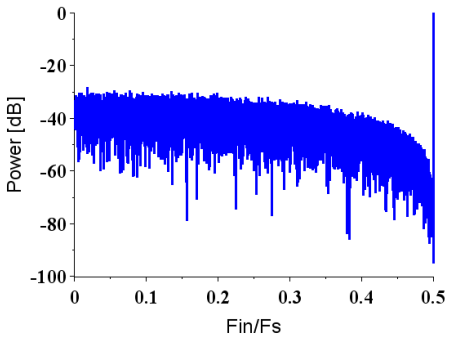
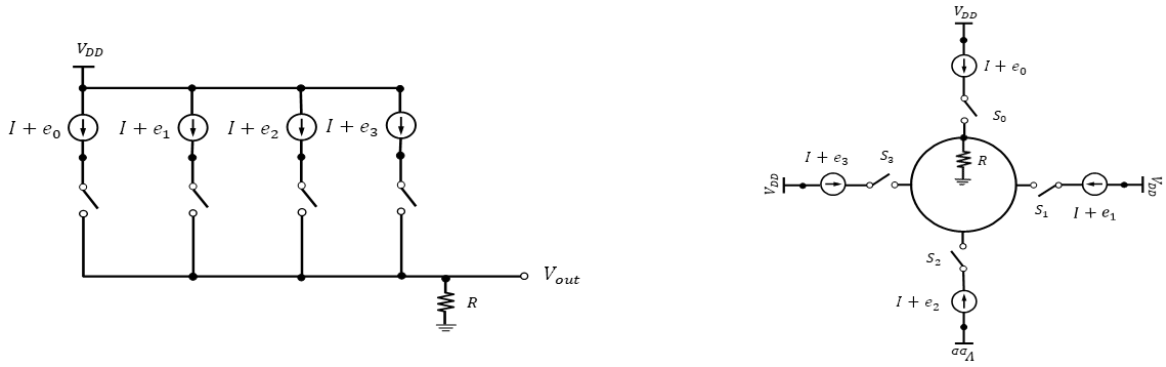


Fig. 4. Power spectrum of the HP ΔΣ modulator output.
(Input sine wave amplitude: 1, normalized frequency: 1)

2.2 Unit current cell mismatches of segmented DAC

We assume that a DAC which follows the modulator has 5-level resolution; its digital input takes the value of 0, 1, 2, or 3 (Fig. 5). Though ideally all currents should be equal, in reality they can be

slightly different due to such as process variation inside an IC chip. e_k in Fig. 5 indicates current mismatch of I_k. In case using Fig. 5(a), the mismatch effects cause almost flat power spectrum in the entire band as well as harmonic distortions.



(a) An 4-unit segmented current steering DAC. (b) Its ring configuration.

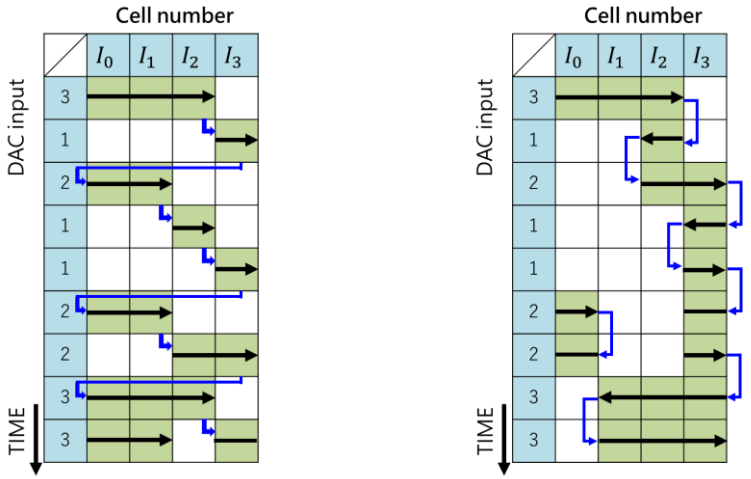
Fig. 5. Current DAC

2.3 Unit cell cyclic selection

In order to reduce the error caused by the nonlinearity of the DAC, consider the element cyclic selection method or data weighted averaging (DWA) algorithm [2]. The configuration is such that unit current cells in the segment type DAC are arranged in a ring shape (Fig. 5 (b)), and there each current source of the DAC is numbered and a pointer is provided to memorize the position of the current source that turns ON. Let the pointer in the DAC at time n be P (n). Multi-bit DAC nonlinearity error is noise-shaped by sequentially selecting DAC elements and averaging the number of use times of each element.

For type I, current cells I_0, I_1, I_2 are turned on when input signal is 3. $I_3$is on when next input data is 1. I_0, I_1 is on when next input data is 2. When the input signal is 0, all the current cells are OFF. In order to perform this operation, the current DAC input signal is stored in P (n) as a pointer value and it is used for the next operation of the unit cell selection in the DAC (Fig. 6 (a)).

In type II, current cells I_0, I_1, I_2 are turned on for the input signal 3. I_2 is on when next input data is 1. I_2, I_3 are on when the input data next is 2. When the input signal is 0, all the current cells are OFF. Then the current DAC input signal is stored in P (n) as a pointer and it is used for in the next operation of the unit cell selection in the DAC (Fig. 6 (b)).



(a) type Ⅰ (b) type Ⅱ

Fig. 6. Selection method of current cells with DWA.

2.4 Unit Cell Reordering

In order to reduce the error caused by the nonlinearity of the DAC in Fig. 7, the magnitude order among the current cells is measured using a current comparator, and the sort of the current cell is performed by software based on this information. As a rearrangement, e_k in Fig. 5 sets a mismatch (deviation from the average current) of the current source to a, b, c, d (first, second, third, fourth) in an ascending order. There are 24 ways to sort at 5 levels. We use these rearrangements for the unit cell re-ordering.

$$I_a < I_b < I_c < I_d \tag{1}$$

$$\mathrm{I}_{average} = \frac{I_a + I_b + I_c + I_d}{4} \tag{2}$$

$$\begin{aligned} I_a &= \mathrm{I}_{average} + e_a \\ I_b &= \mathrm{I}_{average} + e_b \\ I_c &= \mathrm{I}_{average} + e_c \\ I_d &= \mathrm{I}_{average} + e_d \end{aligned}$$

$$e_a + e_b + e_c + e_d = 0 \tag{3}$$

$$e_a < e_b < e_c < e_d \tag{4}$$

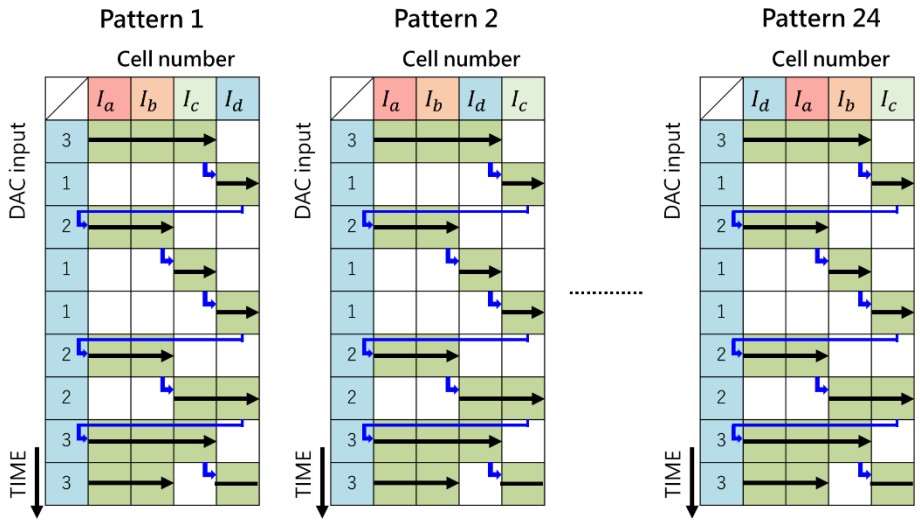


Fig. 7. Unit Cell Reordering.

3. Simulation results

3.1 Configuration of simulation circuit

In this section, we consider a second-order ΔΣ modulator using a combination of element cycling selection method and unit cell circuit rearrangement. We have compared 4 circuits, and verified the linearity improvement. Figure 9, 10 show ③ and ④ circuits. Initially we use current sources 0, 1, 2, 3 to simulate 24 kinds of rearrangement and confirm rearrangement with linearity improvement. Also we have checked the circuit in six ways.

For the LP modulator, the input signal with amplitude of 1.7 and the normalized frequency (fin/fs) of 1/32K is used whereas for the HP modulator, the input signal with amplitude of 1.7 and the normalized frequency of 16383/32K is used.

① 2nd-order (LP or HP) Δ Σ DA modulator + Ideal DAC
② 2nd-order (LP or HP) Δ Σ DA modulator + nonlinearity DAC
③ 2nd-order (LP or HP) Δ Σ DA modulator + nonlinearity DAC + Unit cell cyclic selection (type I or type II) + Bad sequence of combinations
④ 2nd-order (LP or HP) Δ Σ DA modulator + nonlinearity DAC + Unit cell cyclic selection (type I or type II) + Good sequence of combinations

Table. 1. Deviation from the average current among unit current cells

			Pattern					
			1	2	3	4	5	6
Deviation from average current	1th	e_a	-0.5	-0.4	-0.5	-0.1	-0.25	-0.2
	2th	e_b	-0.2	-0.3	-0.3	-0.005	-0.23	-0.13
	3th	e_c	0.2	0.5	0.2	-0.003	0.01	0.02
	4th	e_d	0.5	0.5	0.6	0.17	0.22	0.11

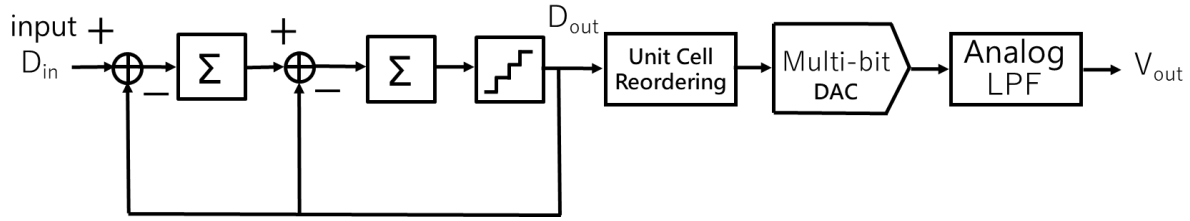


Fig. 8. Proposed LP model circuit with Unit Cell Cyclic Selection (type I) and Unit Cell Reordering.

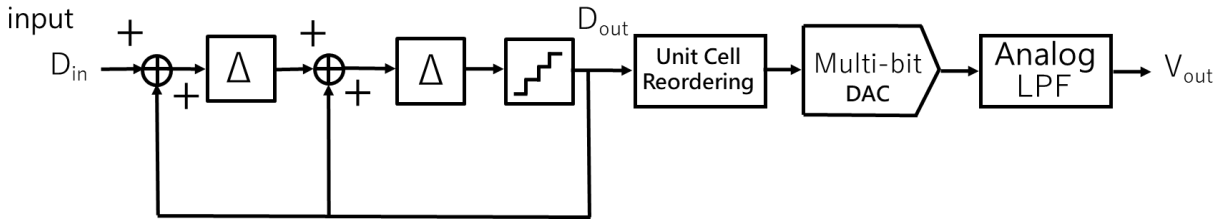


Fig. 9. Proposed HP model circuit with Unit Cell Cyclic Selection (type II) and Unit Cell Reordering.

3.2 SNDR evolution

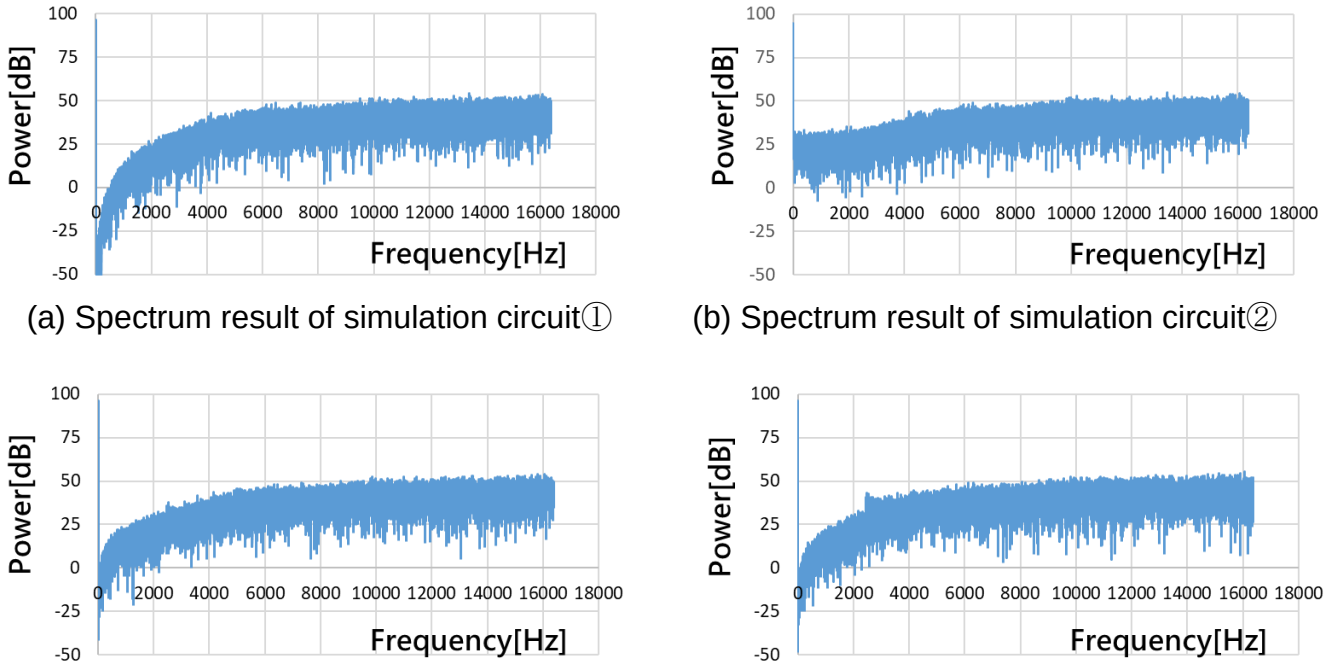
Signal to Noise and Distortion Ratio (SNDR) is one of the DAC performance indices. The DAC performance is considered better as its SNDR is improved.

3.3 SNDR improvement (LP model)

We have verified the effectiveness of the proposed technique using unit cell reordering and unit cell cyclic selection (type I). We use a sinusoidal signal input (D_{in}) whose period is 15K-point and its amplitude is 1.7 with the center value of zero. In practice, unit current cells have some errors (relative mismatches).

Fig. 11 (d) indicates that noise of the low frequency band is reduced. On the other hand, in Fig. 11(b), (c), the noise in the low frequency band is increased. Fig. 12 shows SNDR comparison where mismatch standard deviation: σ is varied. SNDRs are averaged values among 6 sets of the unit current cells. We see that the SNDR values of the proposed circuit ④ is higher than other circuits ②, ③.

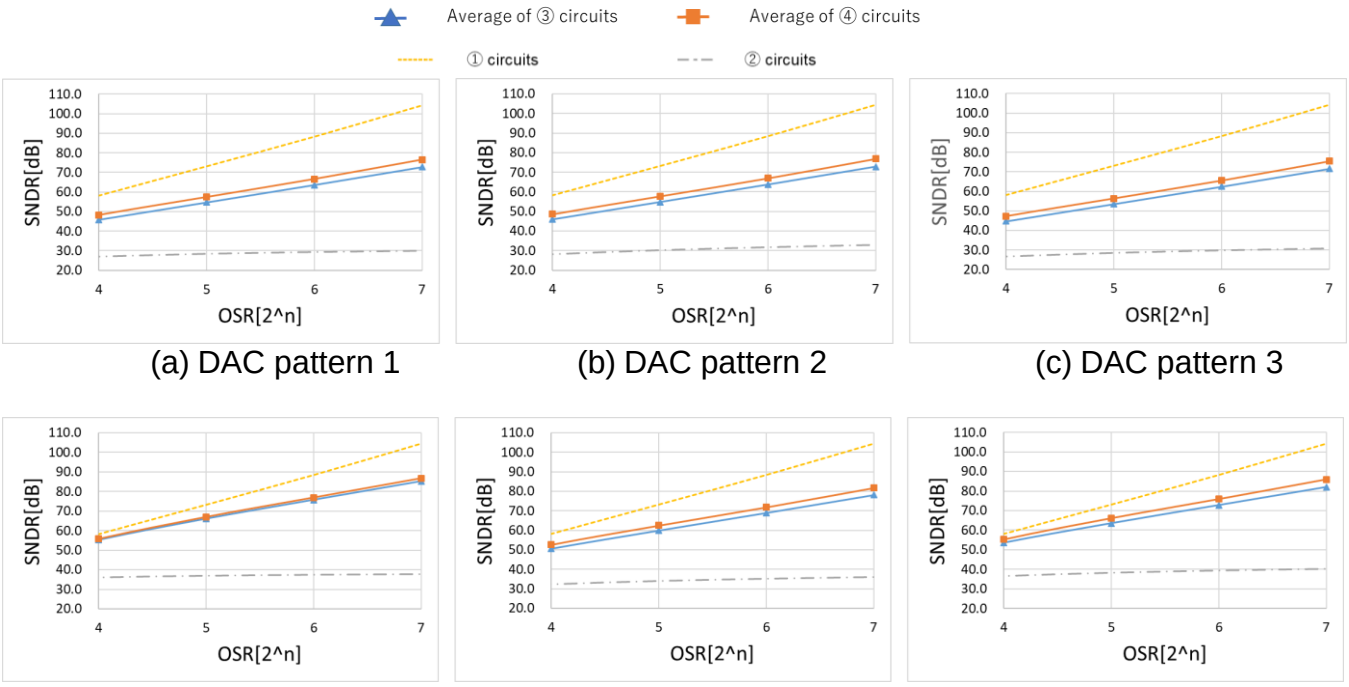
For the combination, the good SNDR was the case that the first and second, the second and the first, the third and the fourth, or the fourth and the third are included. If it did not contain these. SNDR is degraded.



(a) Spectrum result of simulation circuit① (b) Spectrum result of simulation circuit②

(c) Spectrum result of simulation circuit③ (d) Spectrum result of simulation circuit④

Fig. 10. Power spectrum of LP model circuits



(a) DAC pattern 1 (b) DAC pattern 2 (c) DAC pattern 3

(d) DAC pattern 4 (e) DAC pattern 5 (f) DAC pattern 6

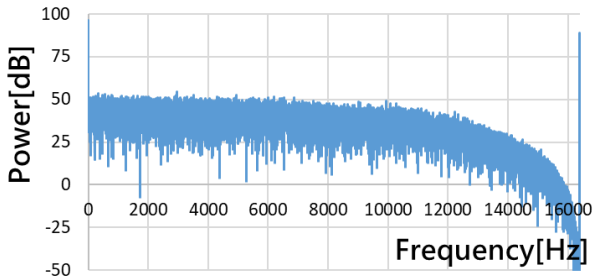
Fig. 11. SNDR result of each DAC pattern. (LP modulator)

3.4 SNDR improvement (HP model)

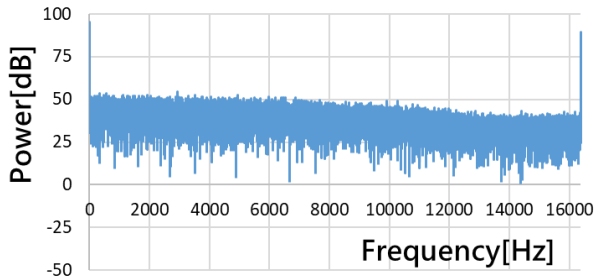
We have verified the effectiveness of the proposed technique using the unit cell reordering and the unit cell cyclic selection (type I). We use a sinusoidal signal input (D_{in}) whose period is 15K-point and its amplitude is 1.7 with the center value of zero. Unit current cells have some errors (mismatches).

In a similar manner, we confirm the effectiveness of the proposed HP model circuit using Unit cell cyclic selection (type II) and Unit Cell Reordering (Fig. 10). Fig. 13(d) indicates noise of the high frequency band is reduced. On the other hand, Fig. 13(b), (c) noise of the high frequency band is increased. Fig. 14 shows SNDR comparison and the SNDR values of the proposed circuit ④ is higher than other circuits ② and ③.

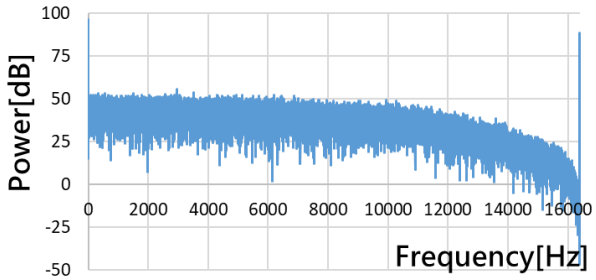
Similar to the LP modulator case, the good SNDR was the case that he first and second, the second and the first, the third and fourth, or the fourth and the third in order of combination is included; otherwise the SNDR is degraded.



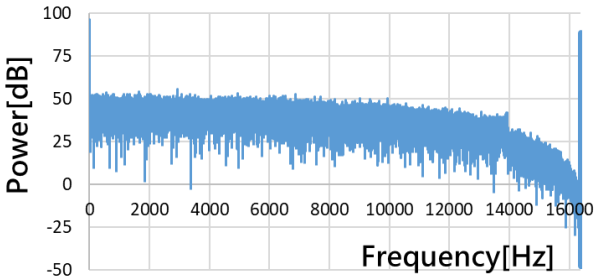
(a) Spectrum result of simulation circuit①



(b) Spectrum result of simulation circuit②

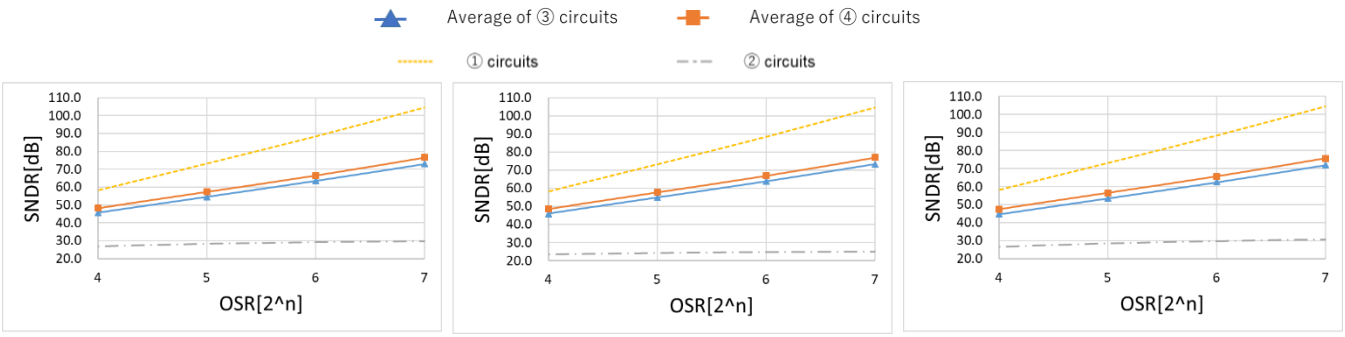


(c) Spectrum result of simulation circuit③

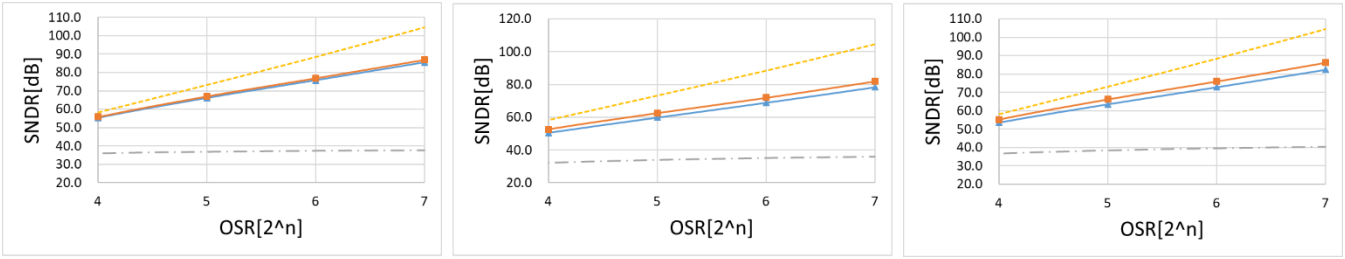


(d) Spectrum result of simulation circuit④

Fig. 12. Power spectrum of HP model circuits



(a) DAC pattern 1 (b) DAC pattern 2 (c) DAC pattern 3



(d) DAC pattern 4 (e) DAC pattern 5 (f) DAC pattern 6

Fig. 13. SNDR result of each DAC pattern.(HP modulator)

4. Conclusion

In this paper, we have proposed the combination of the unit cell reordering method and the element cell cycling selection method in order to improve the linearity of multi - bit ΔΣDA converter. We have investigated the algorithms how to reorder the unit cells to improve SNDR. We have confirmed that by using the proposed method, the SNDR is improved as compared with the conventional one.

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