*International Conference on Technology and Social Science 2018 (ICTSS 2018)*
*Invited*

# Low Switching Loss and Scalable 20-40 V LDMOS Transistors with Low Specific On-Resistance

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# Outline

1. Objective and Background
2. Conventional and Proposed LDMOS Transistor Structures
3. Simulation Results
   - Electric characteristics
     - $I_{DS}$-$V_{DS}$, $I_{DS}$-$V_{GS}$, Breakdown, Specific on-resistance vs. breakdown voltage
   - Hot carrier endurance
   - Total power dissipation
4. Summary

Simulation: 3D device simulator **Advance/DESSERT** developed by AdvanceSoft Corporation

# Objective and Background

**Objective:**

- To obtain scalable (low cost) 20-40 V LDMOS transistors for automotive applications to meet the requirements for **(1) wide SOA, (2) high hot carrier endurance, (3) low specific on-resistance, and (4) low switching loss**

**Uses of LDMOS transistors:**

- 20-40 V LDMOS transistors are widely used as switching devices of power converters for automotive as well as consumer applications including smartphones and tablets.
- Automotive applications operating in **harsh environments** have to meet the above requirements.

**Conventional devices:**

- We developed dual RESURF scalable 30-50 V LDMOS transistors based on a basic LDMOS transistor in 2015.
- These devices meet the above requirements **except for (4).**
- Thus we proposed a 40 V LDMOS transistor to meet **all the requirements** by improving the 30-50 V LDMOS transistors. ⇒ This is a single device.

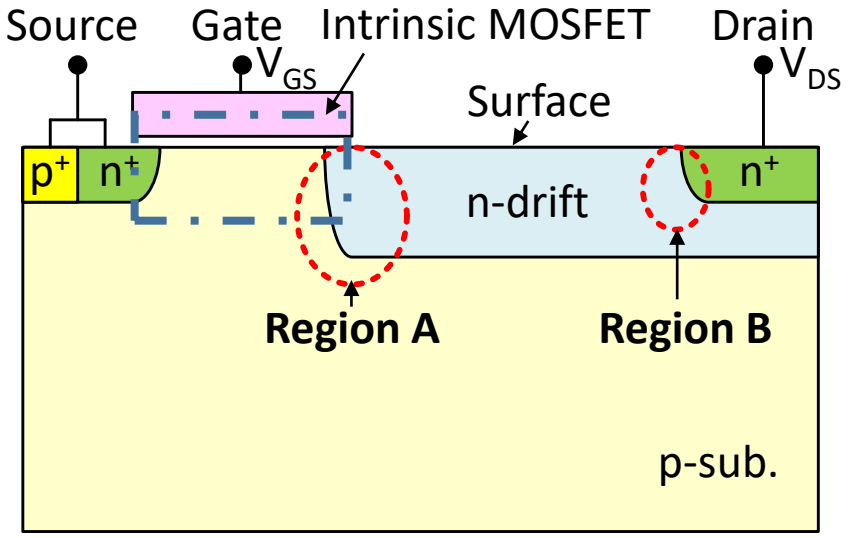
  ⇒ **Scalable (low cost) lower voltage devices are required to obtain circuit design flexibility**.

**Proposed device:**

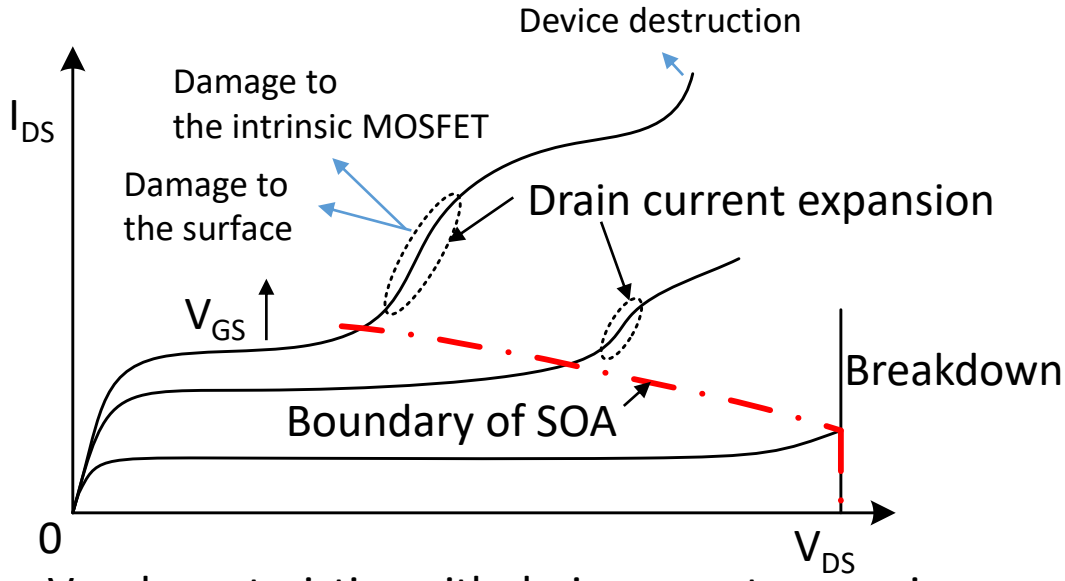
- **We propose 20-40 V LDMOS transistors by reducing the drift region of the 40 V LDMOS transistor.**

Note: SOA (safe operating area), RESURF (reduced surface field)

# Problems of a Basic LDMOS Transistor




A cross-section of a basic n-LDMOS transistor




$I_{DS}$-$V_{DS}$ characteristics with drain current expansion

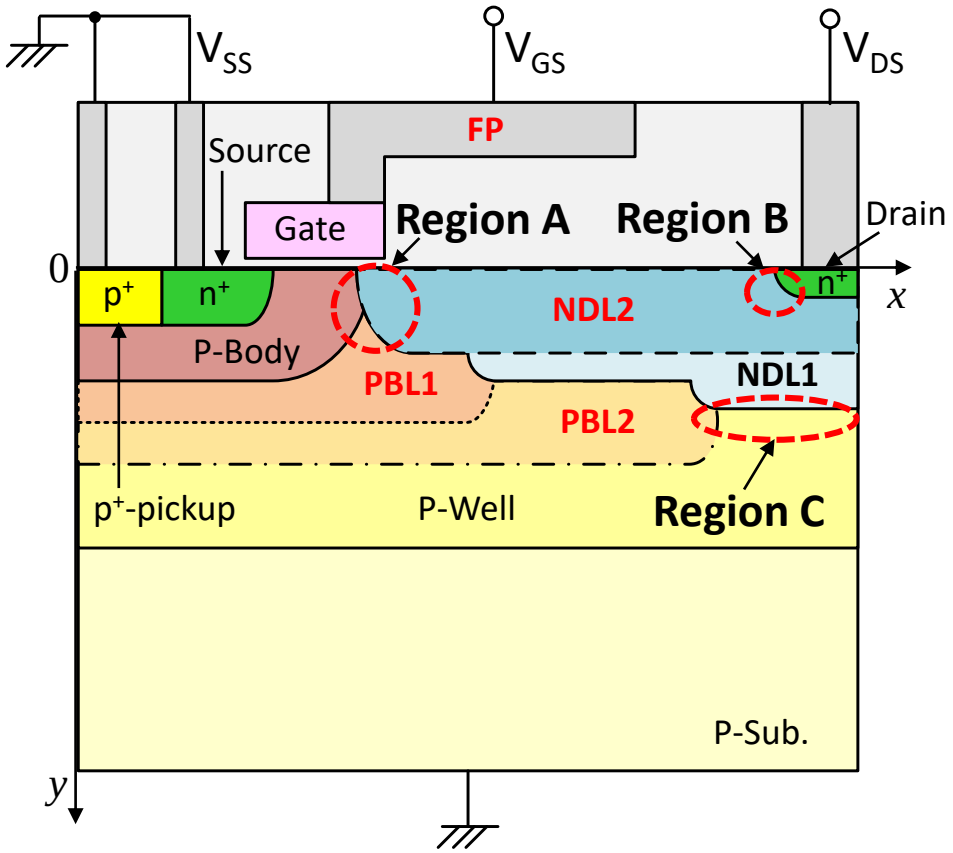
**Problems**

(1) **Low hot carrier endurance** due to **DAHC** (drain avalanche hot carriers)
⇒ Caused by a high electric field in **Region A**

(2) **Drain current expansion (CE) leading to a narrow SOA**
⇒ Caused by a high electric field in **Region B due to the Kirk effect**

(3) **High specific on-resistance**
⇒ Caused by a low impurity concentration in the n-drift region

# Conventional LDMOS Transistor Structure




A cross-section of the conventional device
(One cell size: 3.725 µm × 0.3 µm)
**0.35 µm CMOS compatible process**

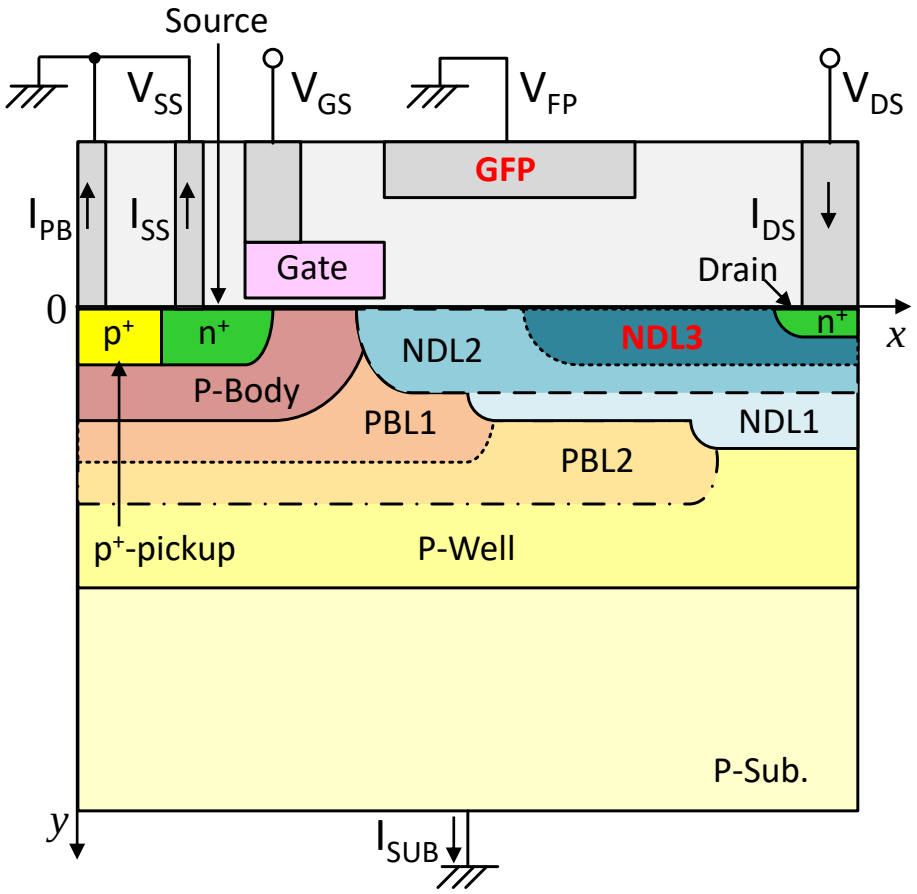
■ P-buried Layers (**Dual RESURF** Structure)
- **PBL1**: Enhances the RESURF effect in **Region A, leading to high hot carrier endurance**
- **PBL2**: ① Causes a uniform electric field in the drift region
  ② Avoids premature breakdown in **Region C**

■ N-drift Layers
- NDL1: The basic layer of the drift region
- **NDL2**: **Reduces specific on-resistance and suppresses CE due to a low electric field in Region B**

■ Field Plate (**connected to the gate**)
- Complements the RESURF effect in the drift region
- **Increases the Miller capacitance, leading to a large switching loss**

**Reduction of the switching loss is required.**

# Proposed LDMOS Transistor Structure

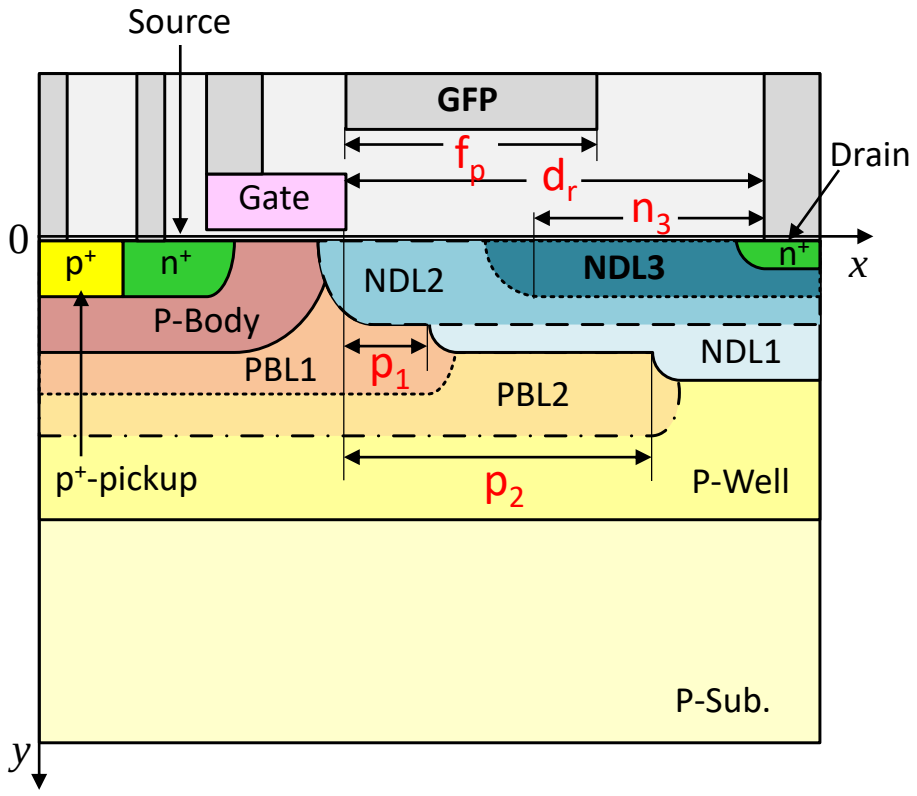



A cross-section of the proposed device
(One cell size: 3.555 µm × 0.3 µm)
**0.18 µm CMOS compatible process**

- P-buried Layers (Dual RESURF Structure)
  - PBL1 and 2: Same as the conventional device
- N-drift Layers
  - NDL1 and 2: Same as the conventional device
  - **NDL3: Reduces specific on-resistance and suppresses CE**
    (Needed to reduce the specific on-resistance increased by GFP)
- Field Plate (**connected to the ground**): **GFP (Grounded Field Plate)**
  - Complements the RESURF effect in the drift region
  - **Reduces the Miller capacitance, leading to a low switching loss**
- Single LDMOS transistor (only for 40 V operation)
  - **limits the flexibility of circuit design**

**Scalable (low cost) lower voltage devices are required to enhance the flexibility of circuit design.**

# How to Make Scalable LDMOS Transistors

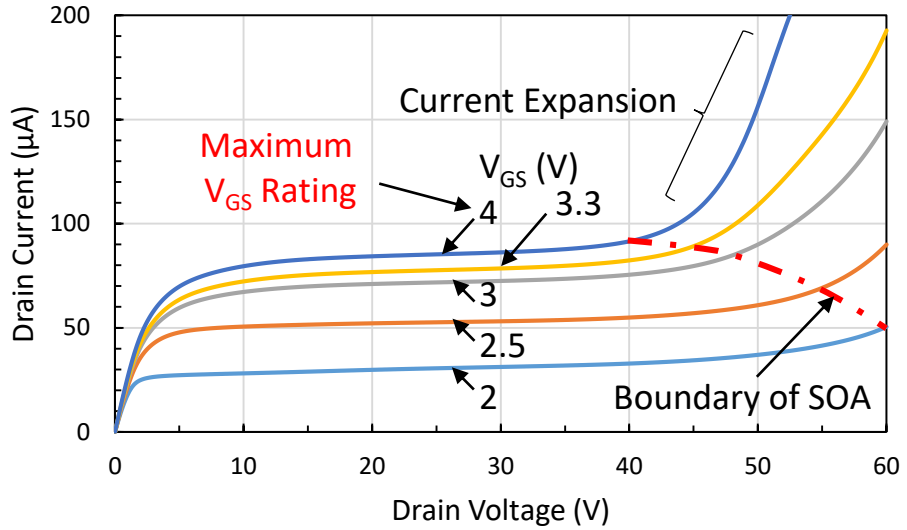



■ Reduction of the Drift Region Length (DRL)

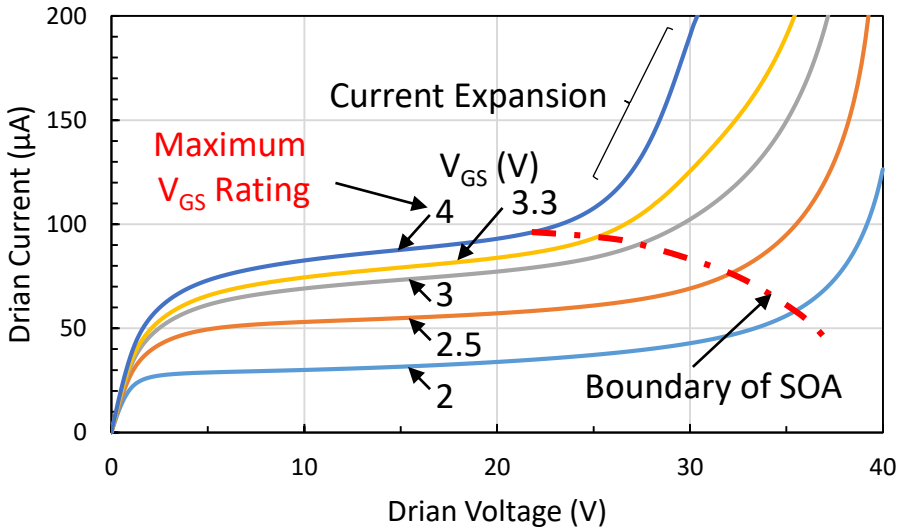
- **Each of $p_1$, $p_2$, and $f_p$ is scaled down in proportion to the change in $d_r$ (DRL).**
- **$n_3$ is not changed** to avoid an increase in the electric field near the gate-side drift region edge.

$f_p$: the length of GFP over the drift region
$d_r$: the length of the drift region (DRL)
$n_3$: the length of NDL3
$p_1$: the length of PBL1 under the drift region
$p_2$: the length of PBL2 under the drift region

# $I_{DS}$-$V_{DS}$ Characteristics of the Proposed Devices




DRL Reduction




(a) No DRL reduction device (One Cell: 3.555μm × 0.3μm)

(b) 50 % DRL reduction device (One Cell: 2.23μm × 0.3μm)

■ **SOA** excluding the CE region

⇒ **Sufficiently satisfies an operation $V_{DS}$ of 40 V**

■ **Specific on-resistance**

⇒ **$R_{on}A$ = 40.9 mΩ·mm²** at $V_{GS}$ = 3.3 V

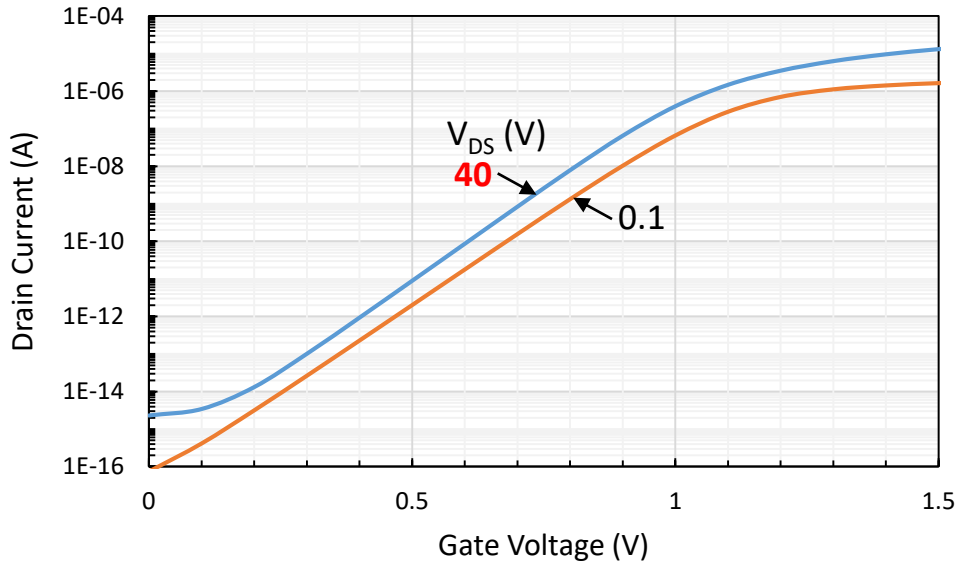
■ **SOA** excluding the CE region

⇒ **Sufficiently satisfies an operation $V_{DS}$ of 20 V**

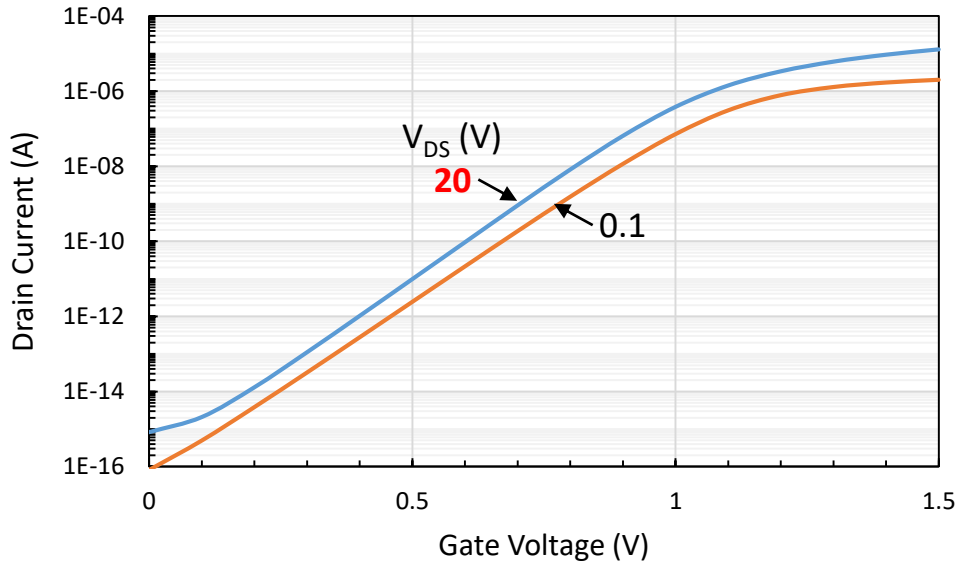
■ **Specific on-resistance**

⇒ **$R_{on}A$ = 18.4 mΩ·mm²** at $V_{GS}$ = 3.3 V

# $I_{DS}$-$V_{GS}$ Characteristics of the Proposed Devices




DRL Reduction



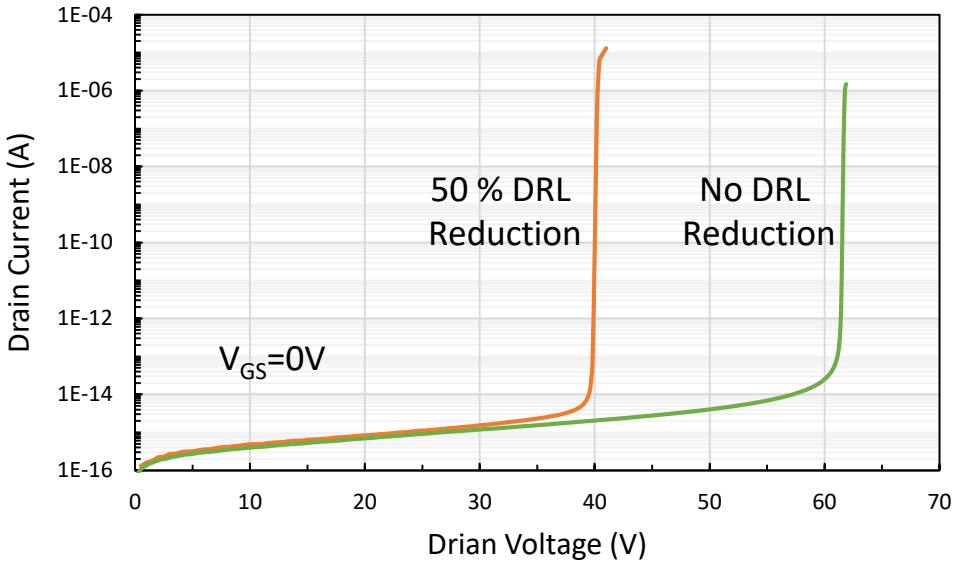

(a) No DRL reduction device (One Cell: 3.555μm × 0.3μm)

- Threshold voltage $V_{TH}$
  $V_{TH}$ (at $I_{DS}$= 0.1 μA and $V_{DS}$ = 0.1 V) =1.026 V
- $V_{TH}$ reduction due to a $V_{DS}$ increase
  $\Delta V_{TH}$ ($V_{DS}$ = 0.1V → 40 V) = 0.104 V
- **Very low leak current even at $V_{DS}$ = 40 V**

(b) 50 % DRL reduction device (One Cell: 2.23μm × 0.3μm)

- Threshold voltage $V_{TH}$
  $V_{TH}$ (at $I_{DS}$= 0.1 μA and $V_{DS}$ = 0.1 V) =1.023 V
- $V_{TH}$ reduction due to a $V_{DS}$ increase
  $\Delta V_{TH}$ ($V_{DS}$ = 0.1V → 20 V) = 0.100 V
- **Very low leak current even at $V_{DS}$ = 20 V**

# Breakdown Characteristics of the Proposed Devices




Breakdown Characteristics of the Proposed Devices

■ Breakdown voltage **$BV_{DS}$** (at $I_{DS}$ = 1 × $10^{-13}$ A)

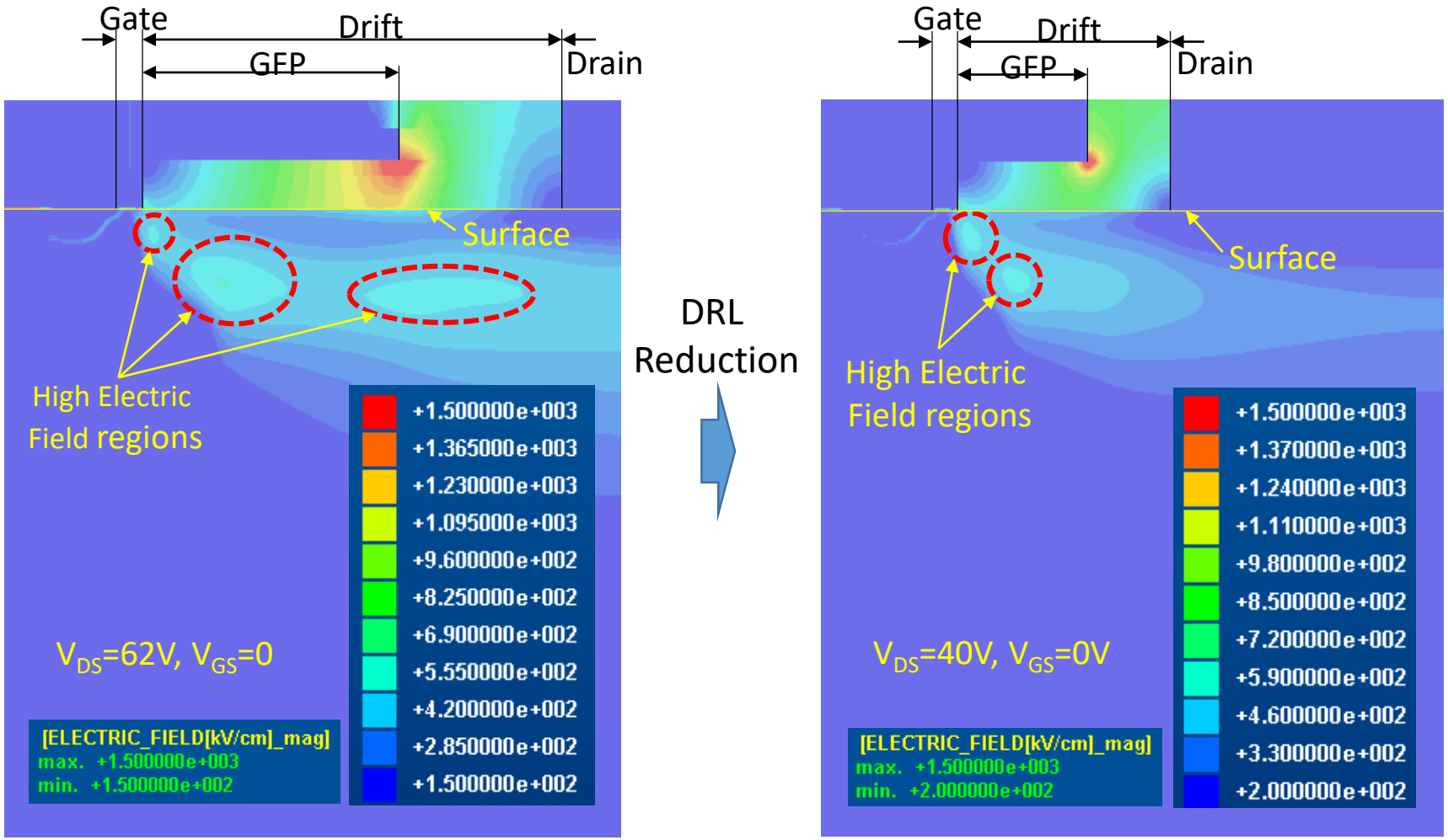
- **50 % DRL** reduction device: **$BV_{DS}$ =39.8 V**

  ⇒ **Ensures sufficient margin for an operation $V_{DS}$ of 20 V**

- **No DRL** reduction device: **$BV_{DS}$ =61.9 V**

  ⇒ **Ensures sufficient margin for an operation $V_{DS}$ of 40 V**

# Electric Field Distributions upon Breakdown




DRL Reduction




(a) No DRL reduction device

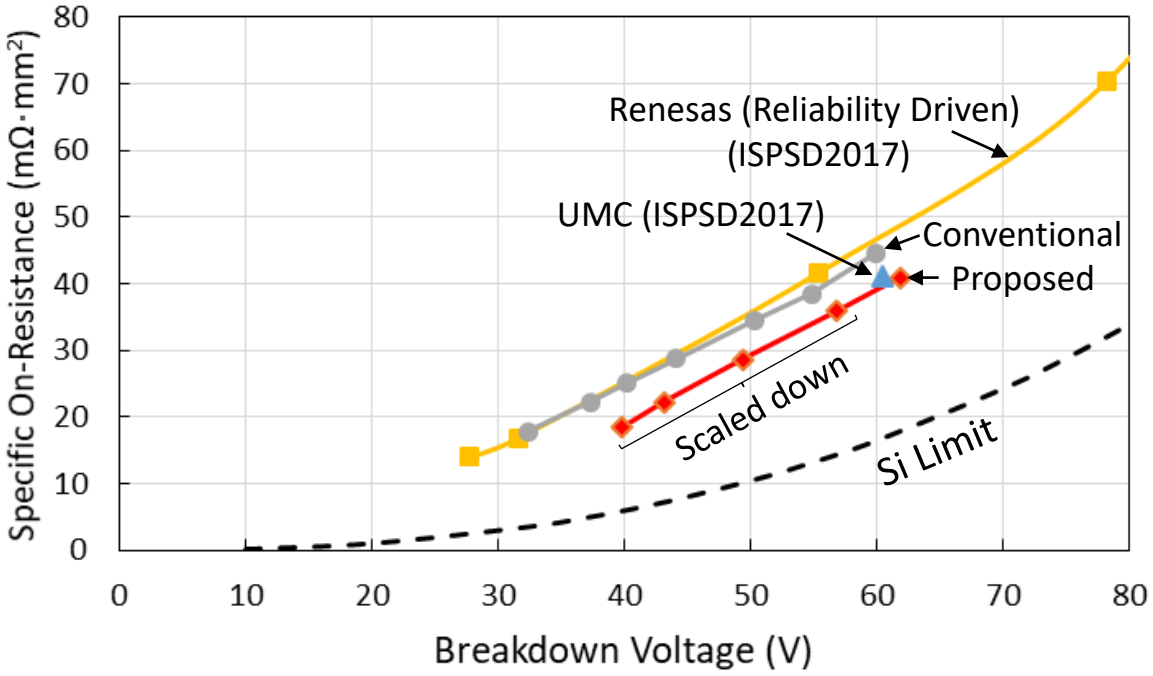
(b) 50 % DRL reduction device

- High electric field regions (Breakdown locations)

  ⇒ **All in the bulk** for both devices

Even repetitive **ESD** events **would not cause damage** to the surface and the intrinsic MOSFET

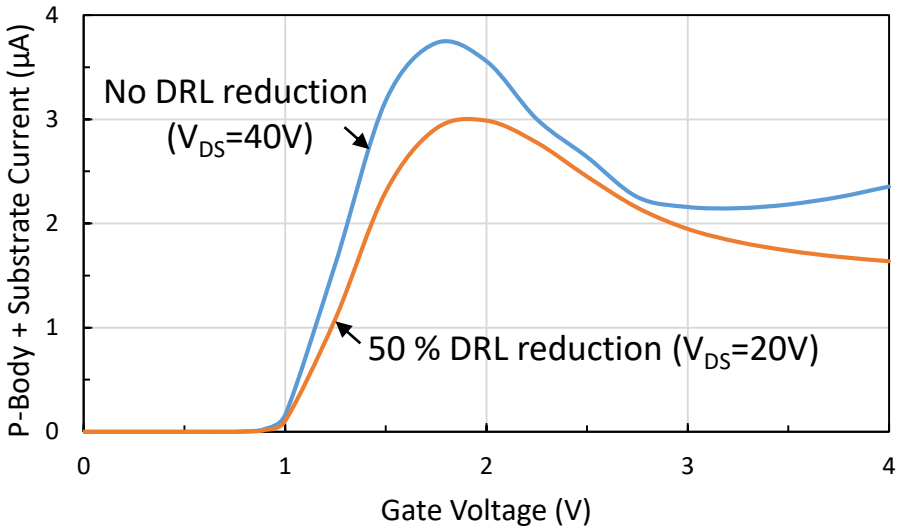
# $R_{on}A$-$BV_{DS}$ Characteristics

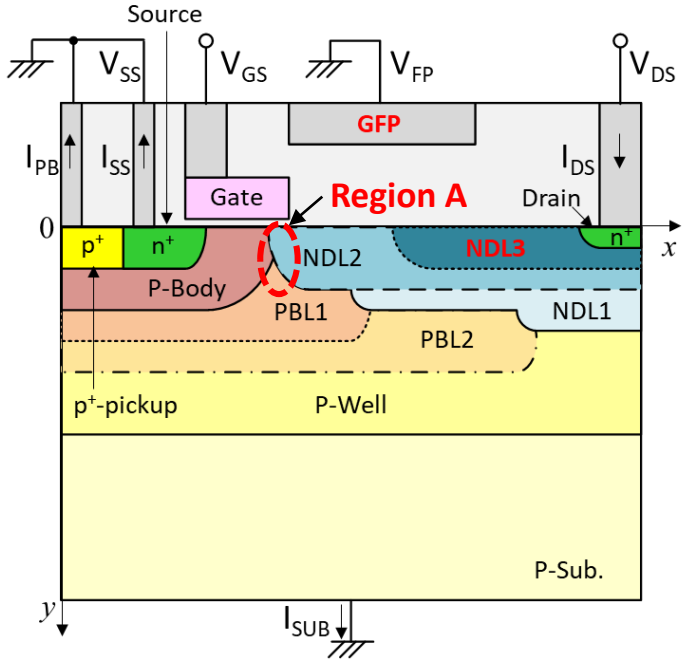



■ $R_{on}A$-$BV_{DS}$ of the proposed device
⇒ Almost the same as
that presented by UMC at ISPSD2017
⇒ **State-of-the-art level**

Note: In this simulation, contact and wiring resistances are not considered.

# $V_{GS}$ Dependence on $I_{PB}$ + $I_{SUB}$ (Total Hole Current)



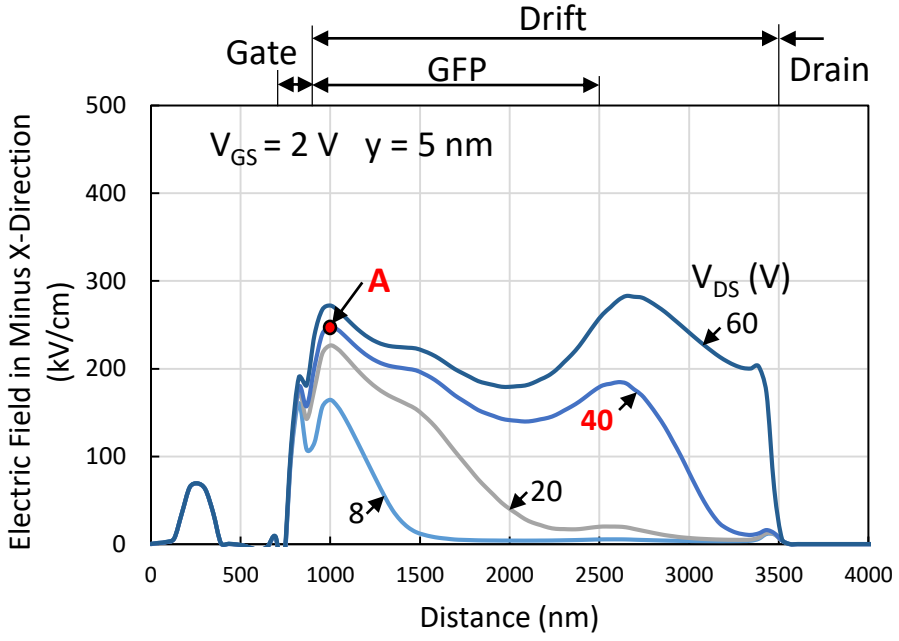




A cross-section of the proposed device

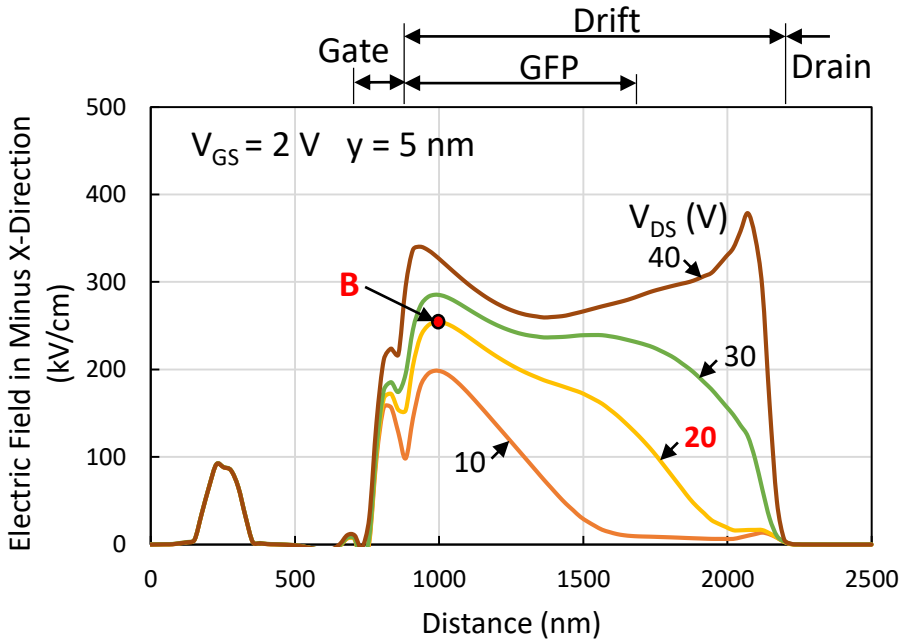
- The peak hole currents for both devices
  - Occur near $V_{GS}$ = 2 V where the intrinsic MOSFET operates in the saturation mode
  - Caused by **DAHC** generated by impact ionization **in Region A**

**The damage due to hot carriers becomes the maximum near $V_{GS}$ = 2 V for both devices.**

# Electric Field Profiles along the Surface ($V_{GS}$ = 2 V)




(a) No DRL reduction device




(b) 50 % DRL reduction device

| DRL | -$E_{xx}$ (kV/cm) | $I_{SS}$ (μA) | $V_{DS}$ (V) | $V_{GS}$ (V) |
|---|---|---|---|---|
| No Reduction | 248 (A) | 30.9 | 40 | 2 |
| 50 % Reduction | 254 (B) | 30.7 | 20 | 2 |

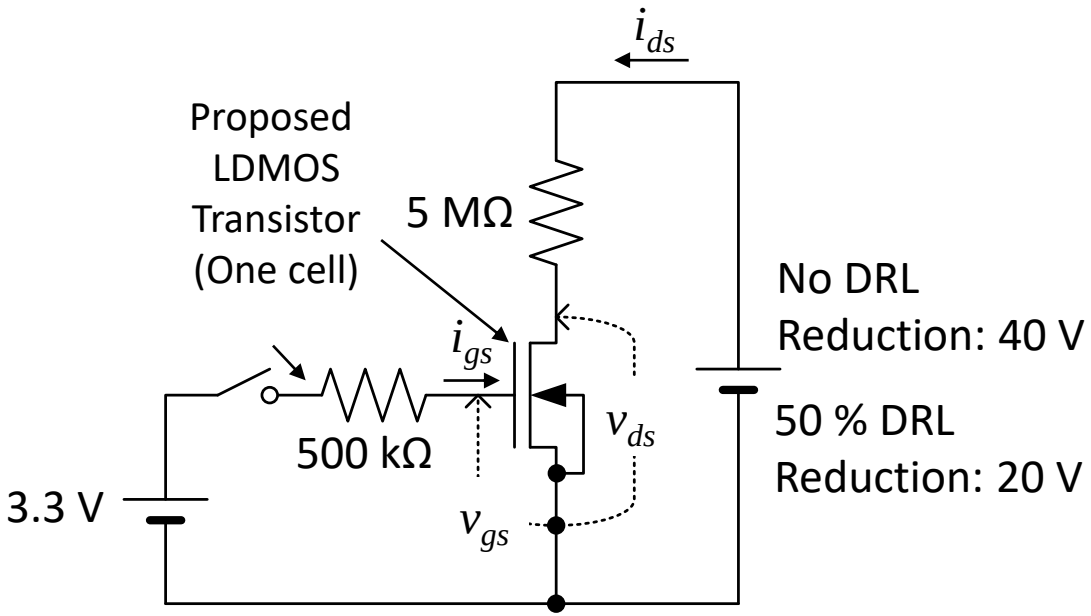
**$E_{xx}$: Electric field in the x-direction at x = 1000 nm**

**$I_{SS}$: Source current (Electron current) for one cell**

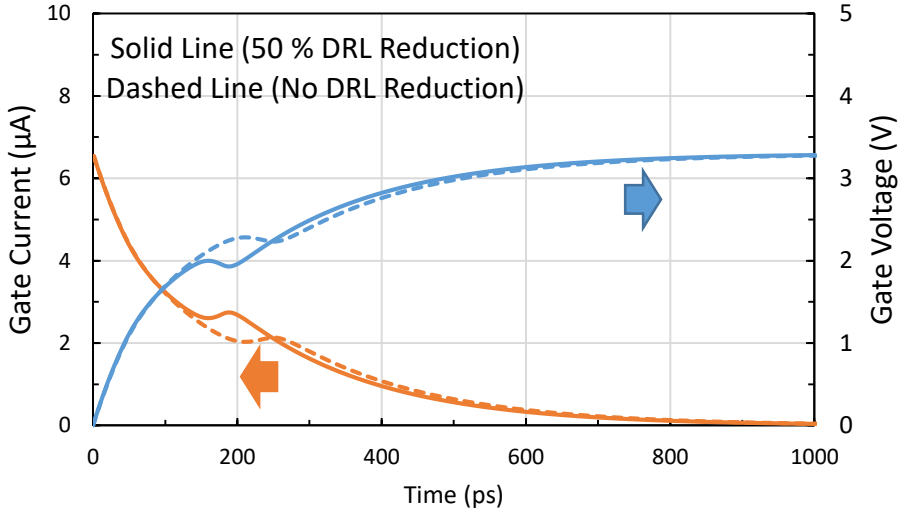
Note: Hole current by impact ionization = F($E_{xx}$, $I_{SS}$)

- Both of the proposed devices
  - ⇒ would have almost the same hot carrier endurance
  - ⇒ would likely be able to have **high hot carrier endurance** due to **the dual RESURF structure**

# Turn-On Characteristics and FOM




The circuit used to obtain turn-on characteristics




Turn-on characteristics of the gate current and the gate voltage (one cell)

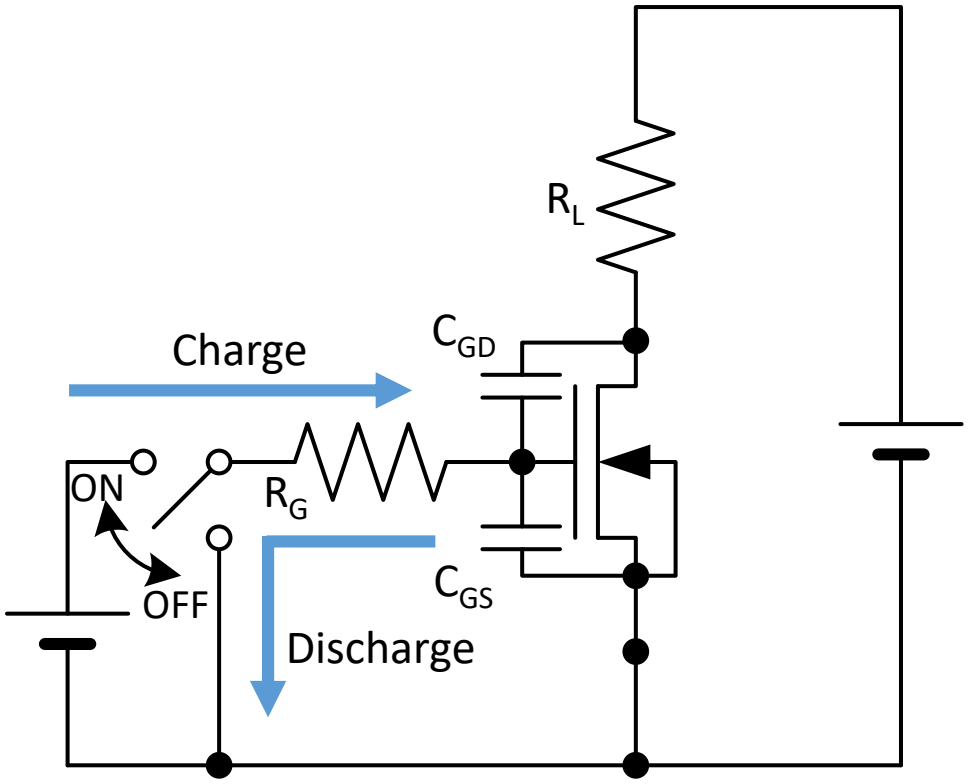
FOM (on-resistance × gate charge)

| Drift Region Length | $Q_g/A$ (nC/mm$^2$) | $R_{on}A$ (mΩ·mm$^2$) | FOM (mΩ·nC) |
|---|---|---|---|
| No Reduction | 1.18 | 40.9 | 48.2 |
| 50 % Reduction | 1.86 | 18.4 | 34.2 |

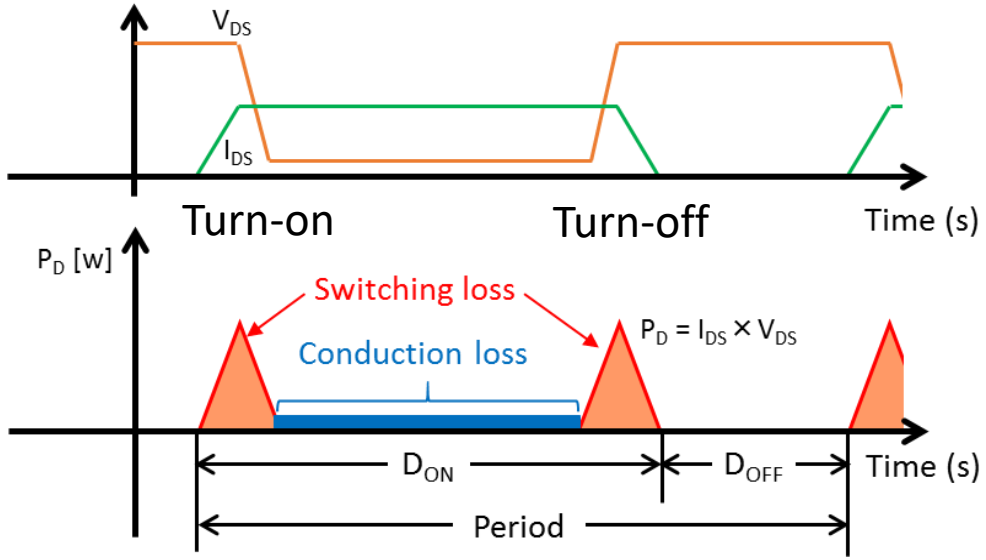
$Q_g/A$: Gate charge density

- FOM of the no DRL reduction device
  ⇒ **about 1/3 that of the conventional device** (**141 mΩ·nC**)
- FOM of the 50 % DRL reduction device
  ⇒ much lower than that of the no DRL reduction device due to the lower specific on-resistance

# Total Power Dissipation




Gate charge during turn-on and gate discharge during turn-off




Switching and conduction losses

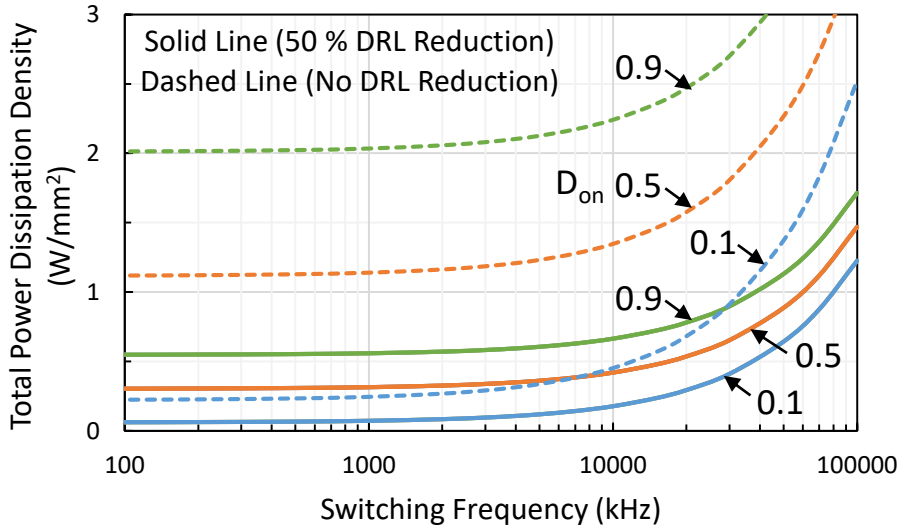
■ The total power dissipation consists of

(1) Gate driving loss due to charging and discharging the gate capacitances ($C_{GS}$ and $C_{GD}$) through $R_G$

(2) Switching loss during turn-on and turn-off

(3) Conduction loss

# Switching frequency dependence of $P_{TD}$




The switching frequency dependence of the total power dissipation density $P_{TD}$ for the proposed devices

Components of the switching energy loss density per switching cycle $\mathbf{E_{SW}}$ for the proposed devices

| Drift Region Length | $E_{GD}$ [J/mm²] | $E_{ON/OFF}$ [J/mm²] | $E_{sw}$ [J/mm²] |
|---|---|---|---|
| No Reduction | $3.89 \times 10^{-9}$ | $1.91 \times 10^{-8}$ | $2.30 \times 10^{-8}$ |
| 50 % Reduction | $6.14 \times 10^{-9}$ | $5.52 \times 10^{-9}$ | $1.17 \times 10^{-8}$ |

■ The $P_{TD}$ of the 50 % DRL reduction device
⇒ Much lower than that of the no DRL reduction device for each $D_{on}$ (due to lower $\mathbf{R_{on}A}$)
⇒ Further lower in a high switching frequency region (due to lower $\mathbf{E_{SW}}$)

# Summary

**Each of the proposed 20-40 V LDMOS transistors**

- Has a **wide SOA** enough for 20-40 V operations, respectively
- Has a **state-of-the-art level characteristic** for $R_{on}A$ -$BV_{DS}$
- Has a **very low FOM** representing high suppression of conduction and switching losses
- Would likely be able to have **high hot carrier endurance**
- **Adequate for harsh environment automotive applications**
- **Enhances the flexibility of circuit design.**

# Acknowledgement

We would like to express sincere thanks to **AdvanceSoft Corporation** for lending us 3D TCAD simulator.

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# Thank you very much for your kind attention!