ICSICT-2018
2018 IEEE 14th International Conference on Solid-State and Integrated Circuit Technology
Oct. 31- Nov. 3, 2018
Huangdao Sheraton Hotel, Qingdao, China

S32-1　Analog Circuits II
13:30-14:00 PM
Nov. 2, 2018 (Fri)

Unified Methodology of Analog/Mixed-Signal IC Design Based on Number Theory

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群馬大学
GUNMA UNIVERSITY

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Statement of This Paper

Number theory ⇨ Can be one of unified methodology of mixed-signal IC design

- Analog filter theory
  based on beautiful mathematics

- However, currently
  no unified design methodology
  for ADC/DAC/TDC

- Here our several research examples
  are introduced.

C. F. Gauss

Number theory is
Queen of mathematics

Contents

[1] Y. Kobayashi, H. Kobayashi,
"Redundant SAR ADC Algorithm Based on Fibonacci Sequence",
Key Engineering Materials (2016).

Fibonacci Sequence

Definition (n=0,1,2,3…)

$$F_0 = 0$$
$$F_1 = 1$$
$$F_{n+2} = F_n + F_{n+1}$$

Example of numbers(Fibonacci number)

0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89…

Leonardo Fibonacci (around 1170-1250)

Property

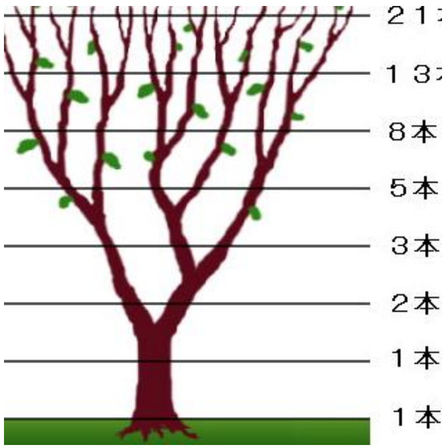
The closest terms ratio converges to *"Golden Ratio"* !

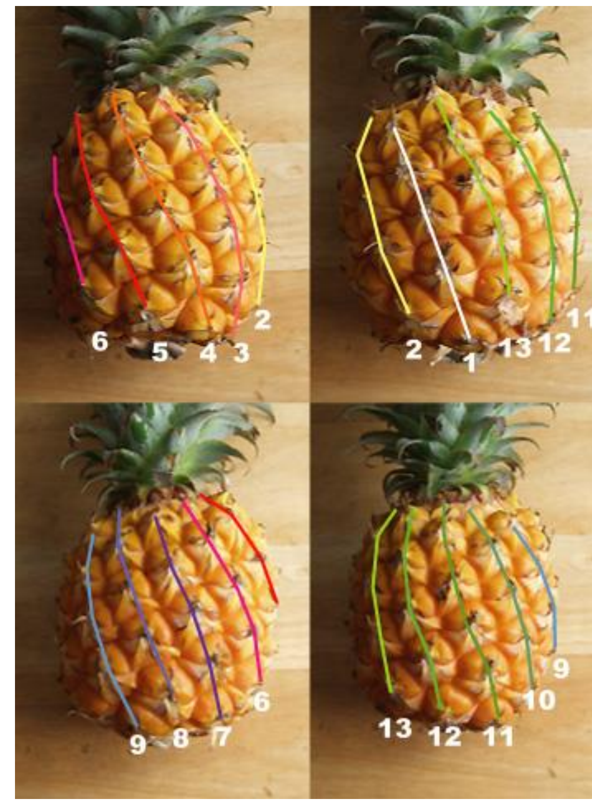
$$\lim_{n\to\infty} \frac{F_n}{F_{n-1}} = 1.618033988749895 = \varphi$$

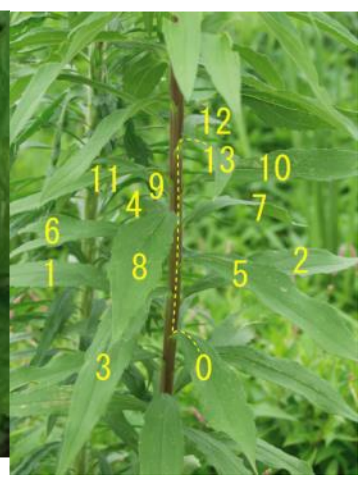
Fibonacci Numbers

0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144…

We can see Fibonacci numbers in nature, especially in plants.







Fibonacci Number is Mysterious !

Definition (n=0,1,2,3…)

$$F_0 = 0$$
$$F_1 = 1$$
$$F_{n+2} = F_n + F_{n+1}$$

Leonardo Fibonacci
(around 1170-1250)

Fibonacci number

00, 01, 01, 02, 03, 05, 08, 13, 21, 34, 55, 89…

One example:

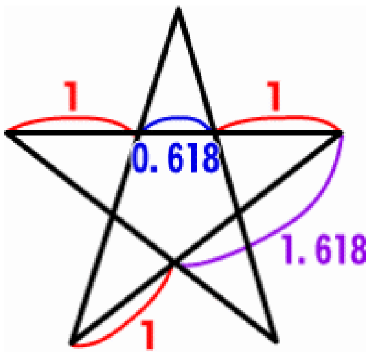
1/9899 =

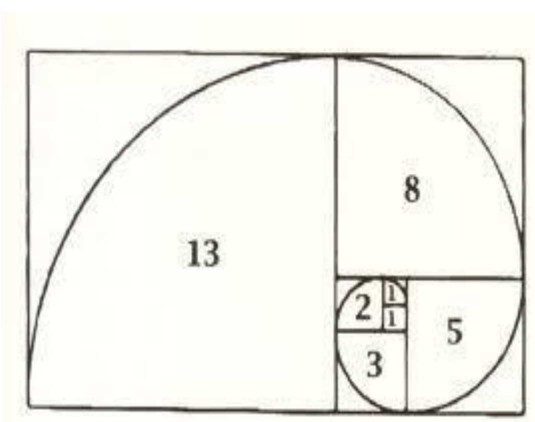
1/0.0001010203050813213455 89…

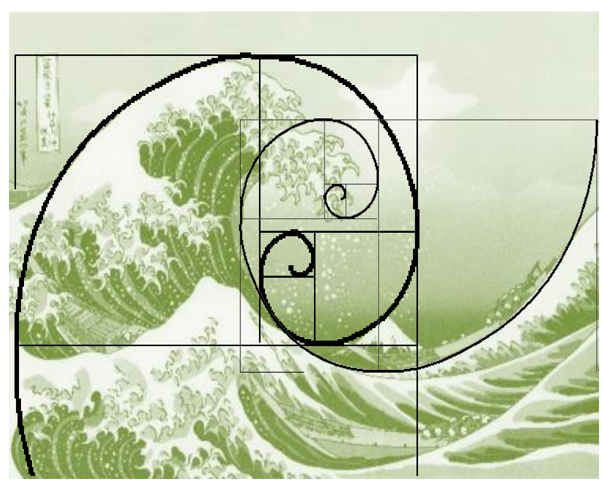
Golden Ratio

$$\textbf{Golden Ratio}: \lim_{n\to\infty} \frac{F_n}{F_{n-1}} = 1.618033988749895 = \varphi$$

The most beautiful ratio







Research Background

Automotive Electronics are in spotlight

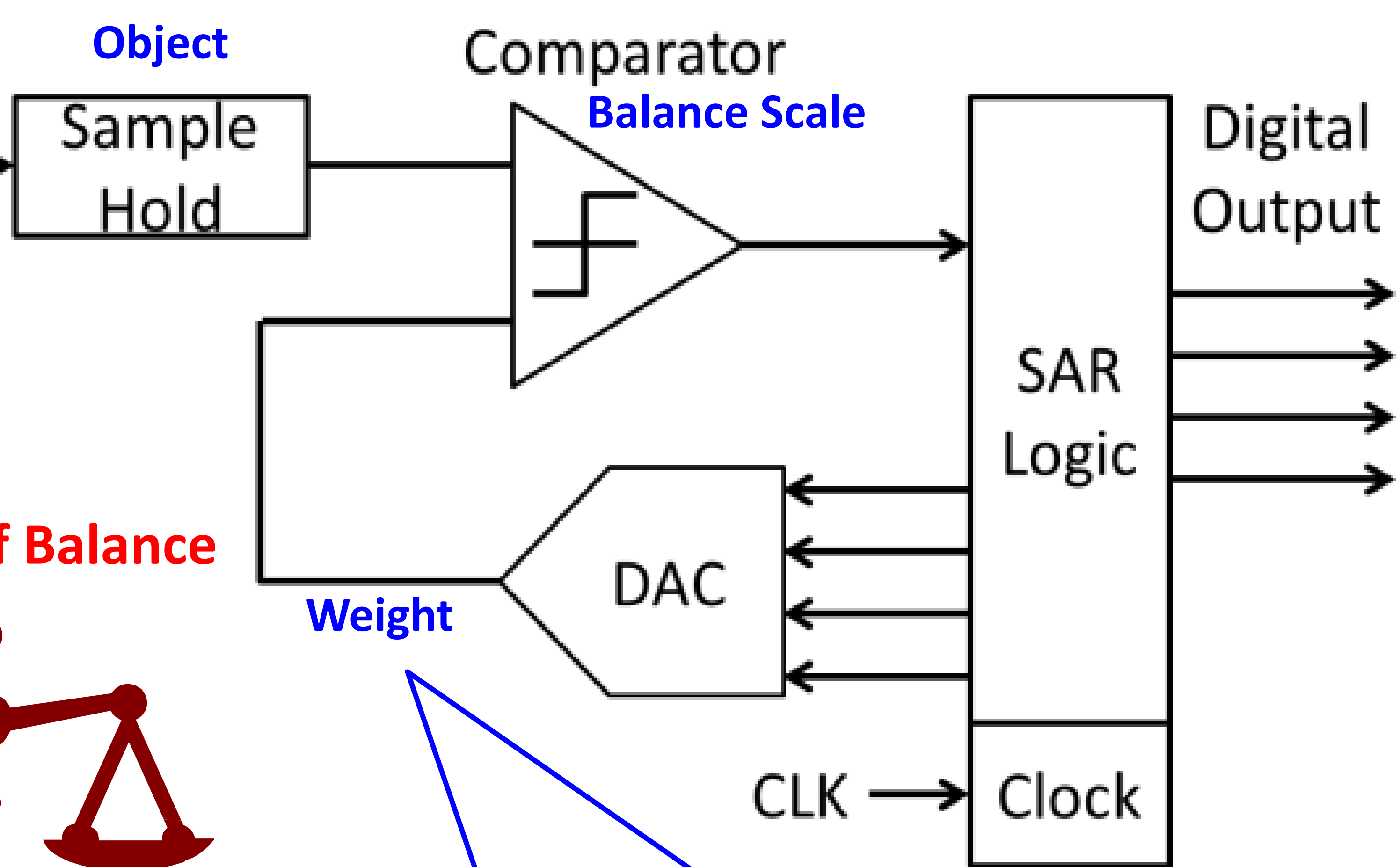
High-speed, Reliable
“SAR ADC” in microcontroller is needed

Redundancy design for error correction

Design issues 

SAR ADC : Successive Approximation Register type Analog to Digital Converter

Binary SAR ADC



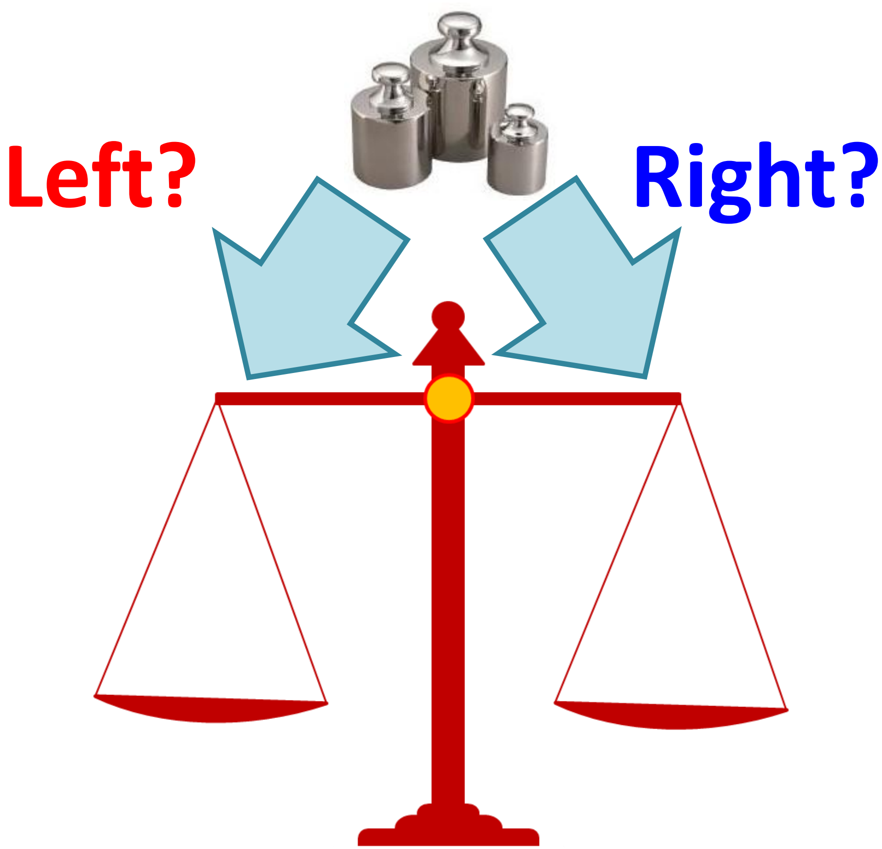
Based on
Principle of Balance

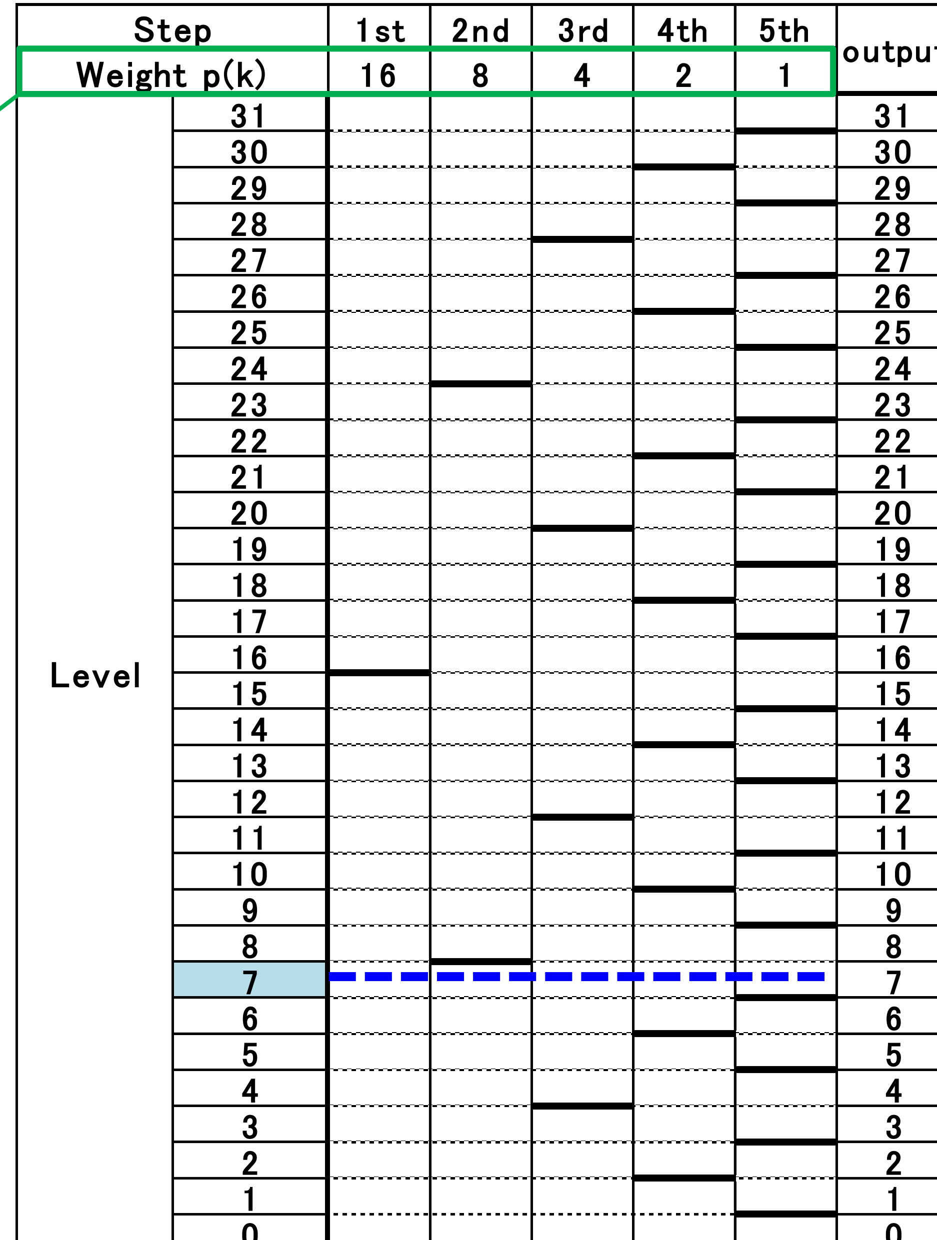
Generally use binary weight
(1 , 2 , 4 , 8 , 16 , 32, 64, …)

Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input : 7.3 [V]
- Binary weight :
  16, 8, 4, 2, 1



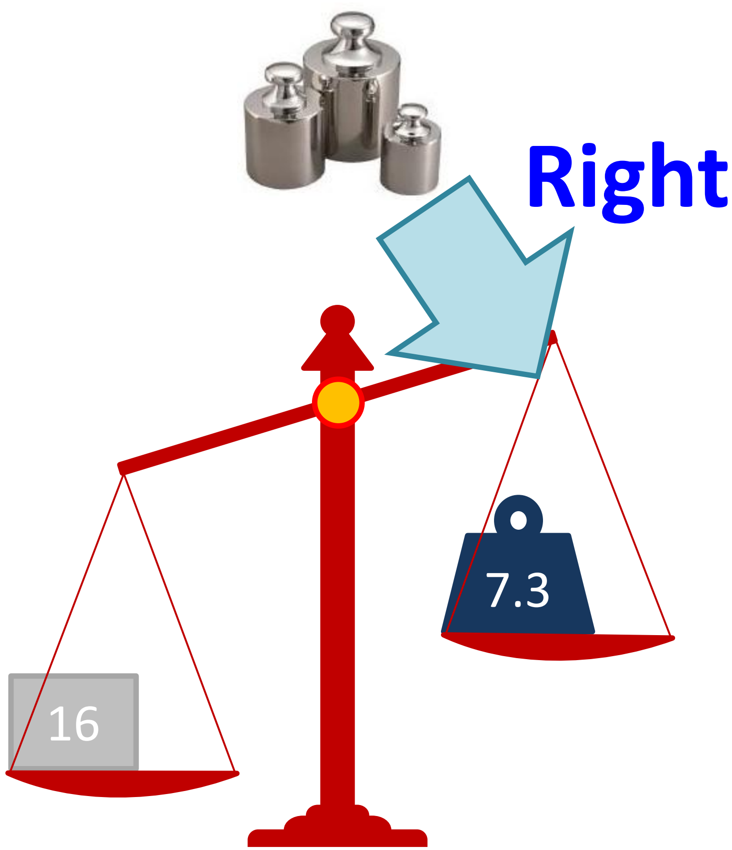


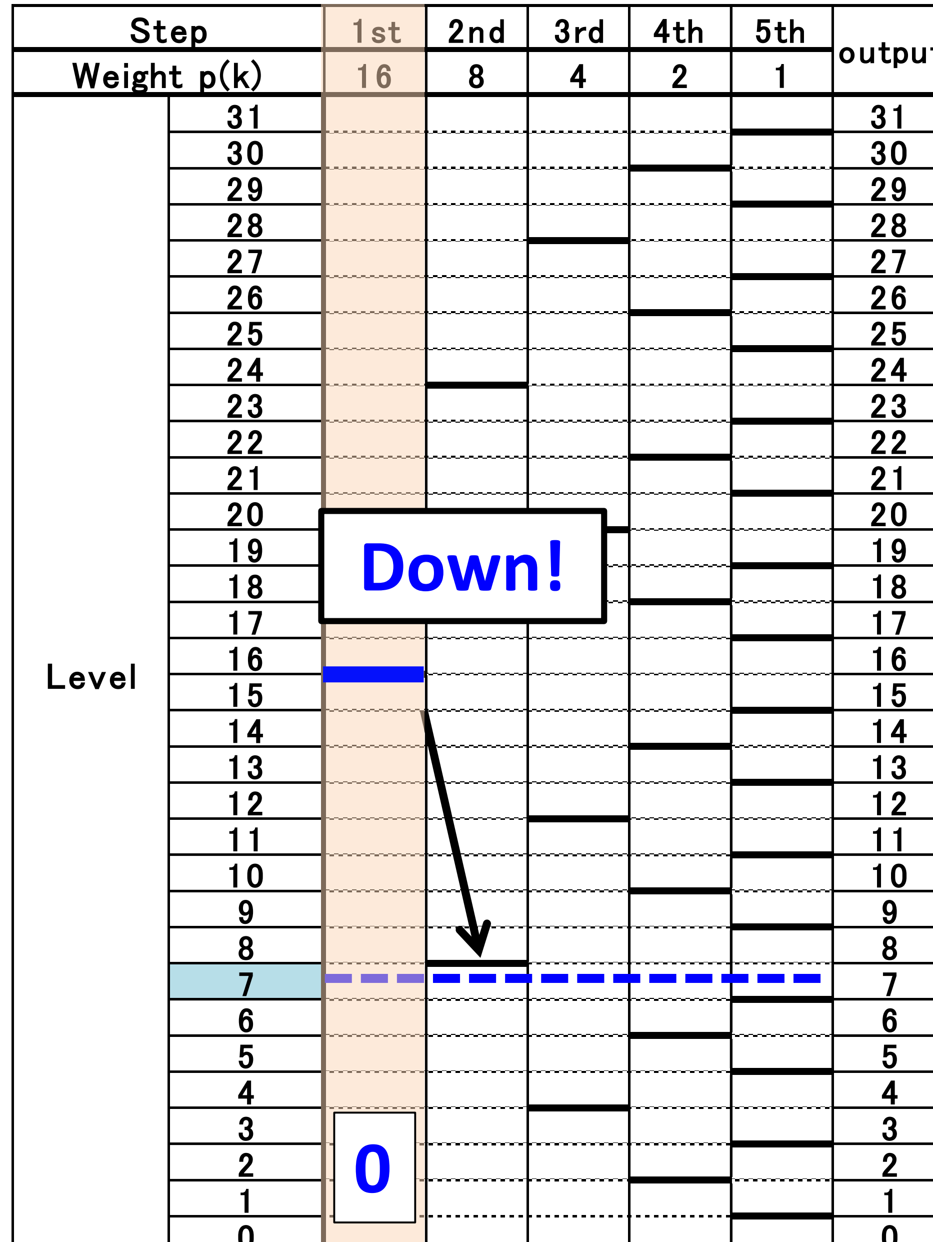
Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input :   [V]
- Binary weight :

  8, 4, 2, 1





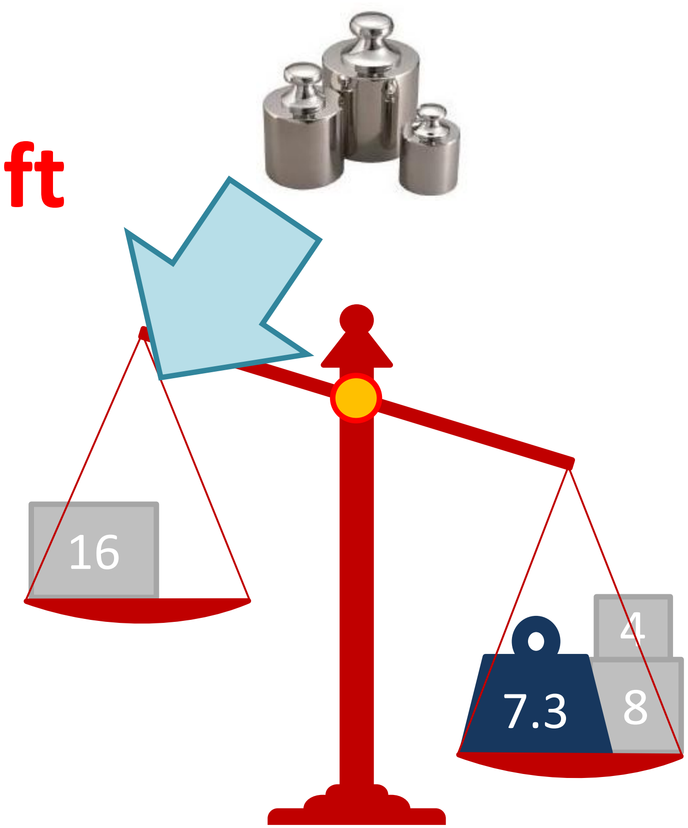
Binary Search SAR ADC Operation

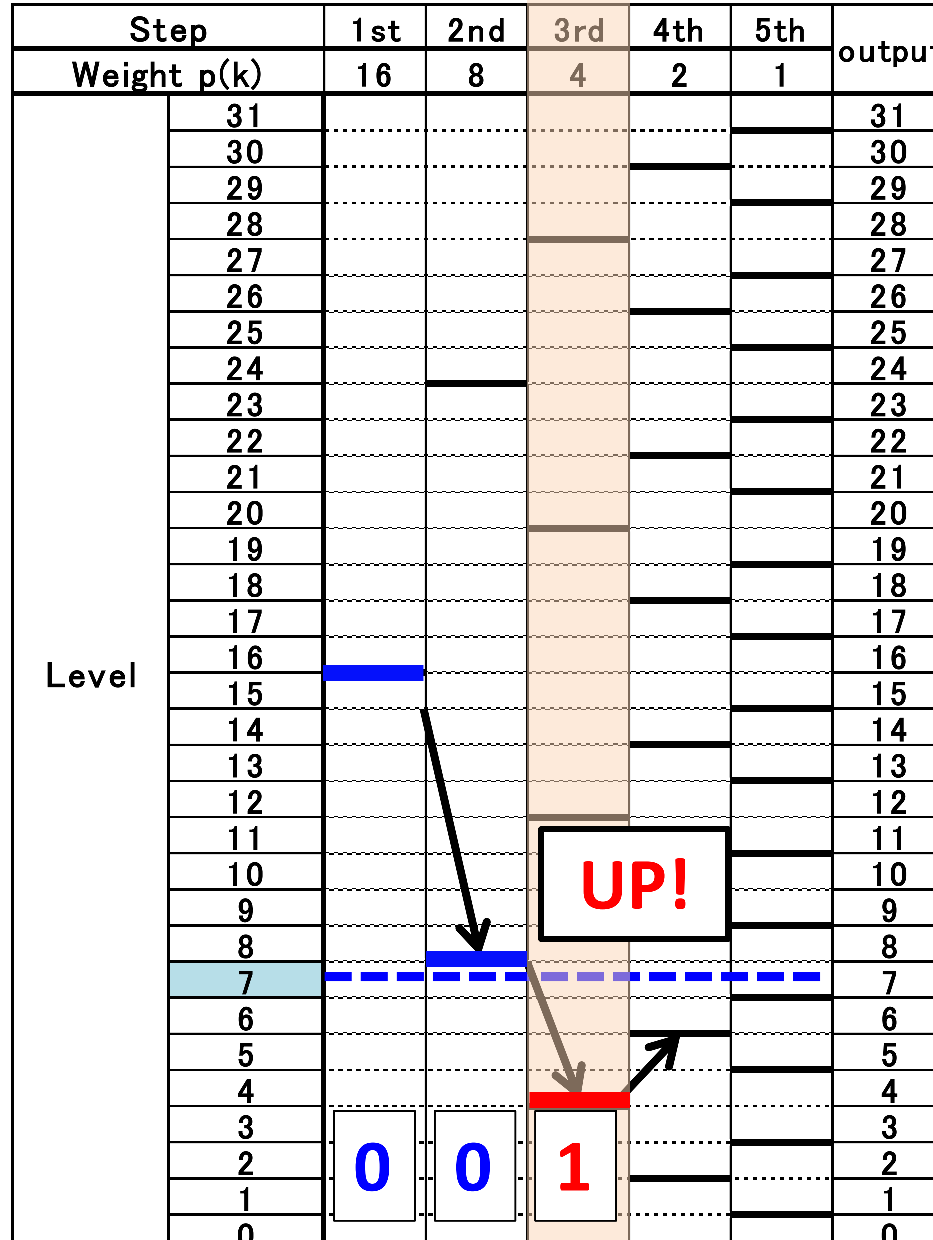
5bit-5step SAR ADC

- Analog Input :   [V]
- Binary weight :

2, 1

Left





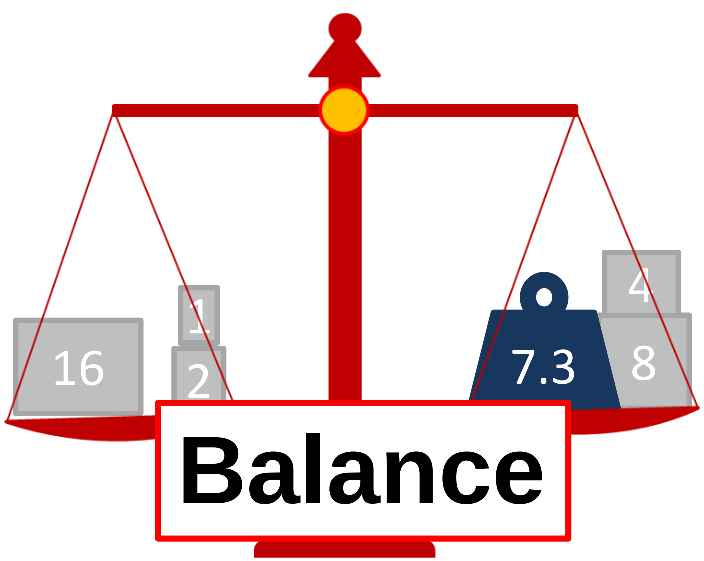
Binary Search SAR ADC Operation

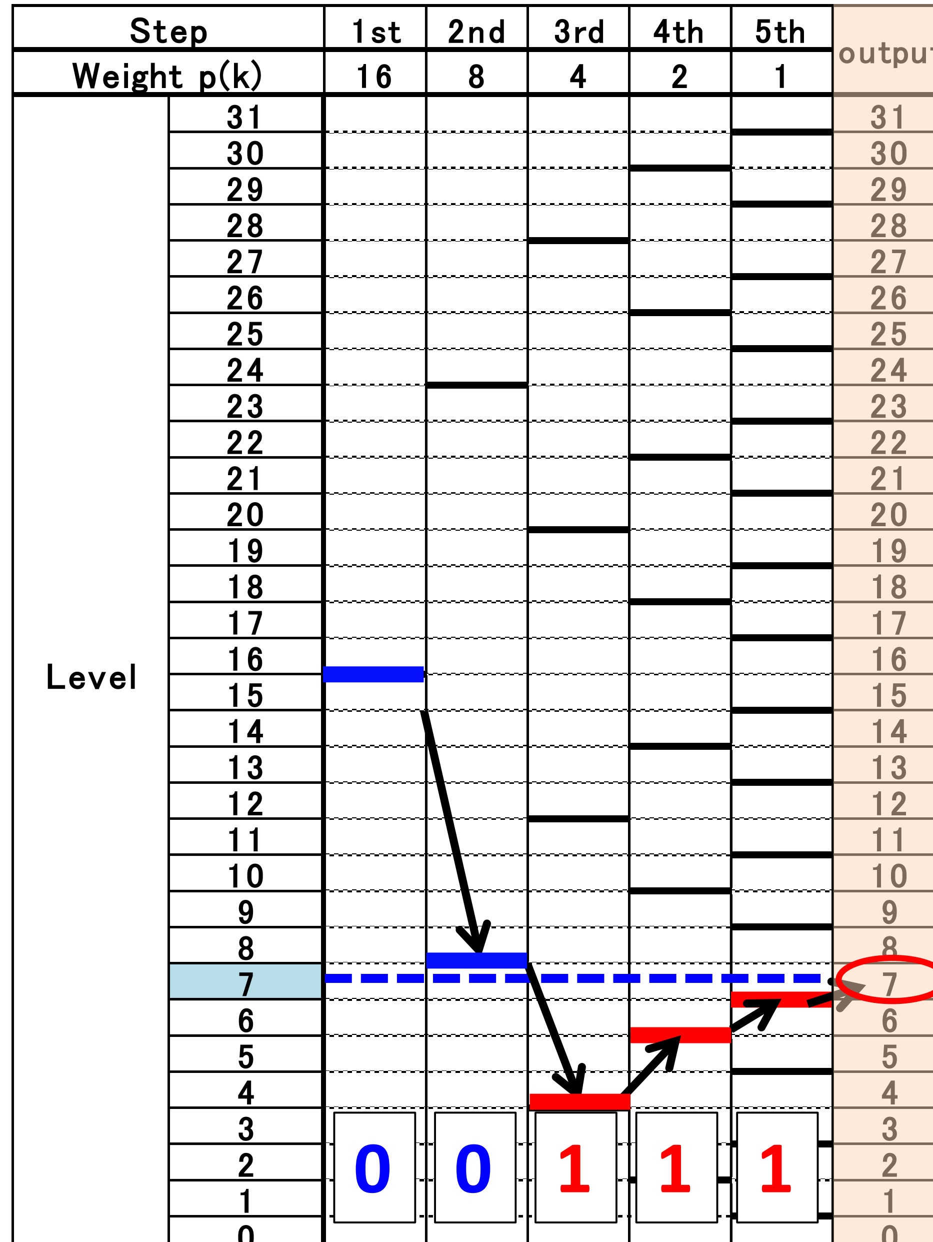
5bit-5step SAR ADC

- Analog Input : [V]
- Binary weight :

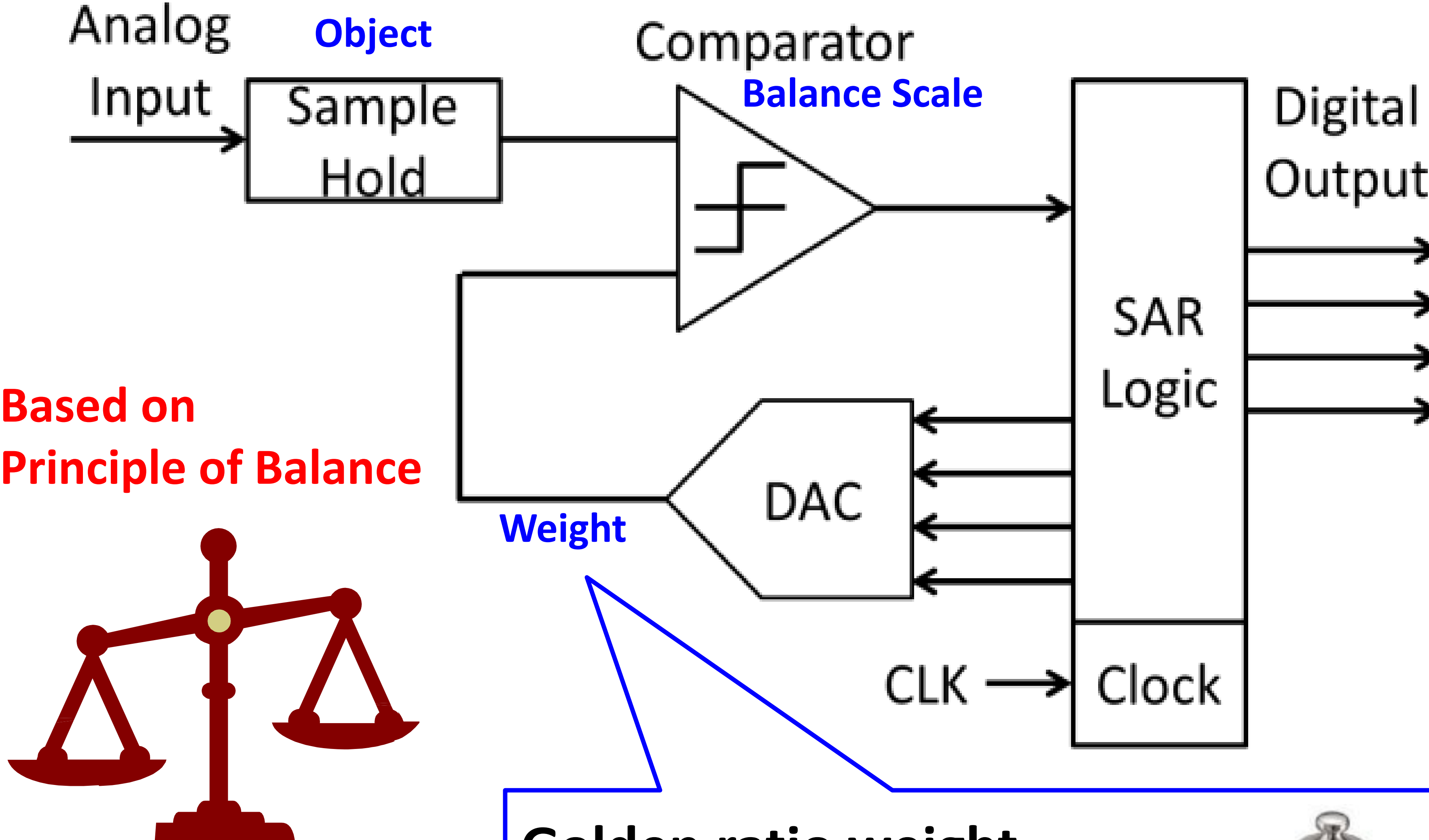
7.3⇒00111⇒7

16 − 8 − 4 + 2 + 1 + 0.5 − 0.5 = **7**





Golden Ratio SAR ADC



Based on
Principle of Balance

Golden ratio weight
(1 , 2 , 3 , 5, 8, 13, 21, 34, …)

Redundancy Design Operation(No Error)

4bit-5step SAR ADC

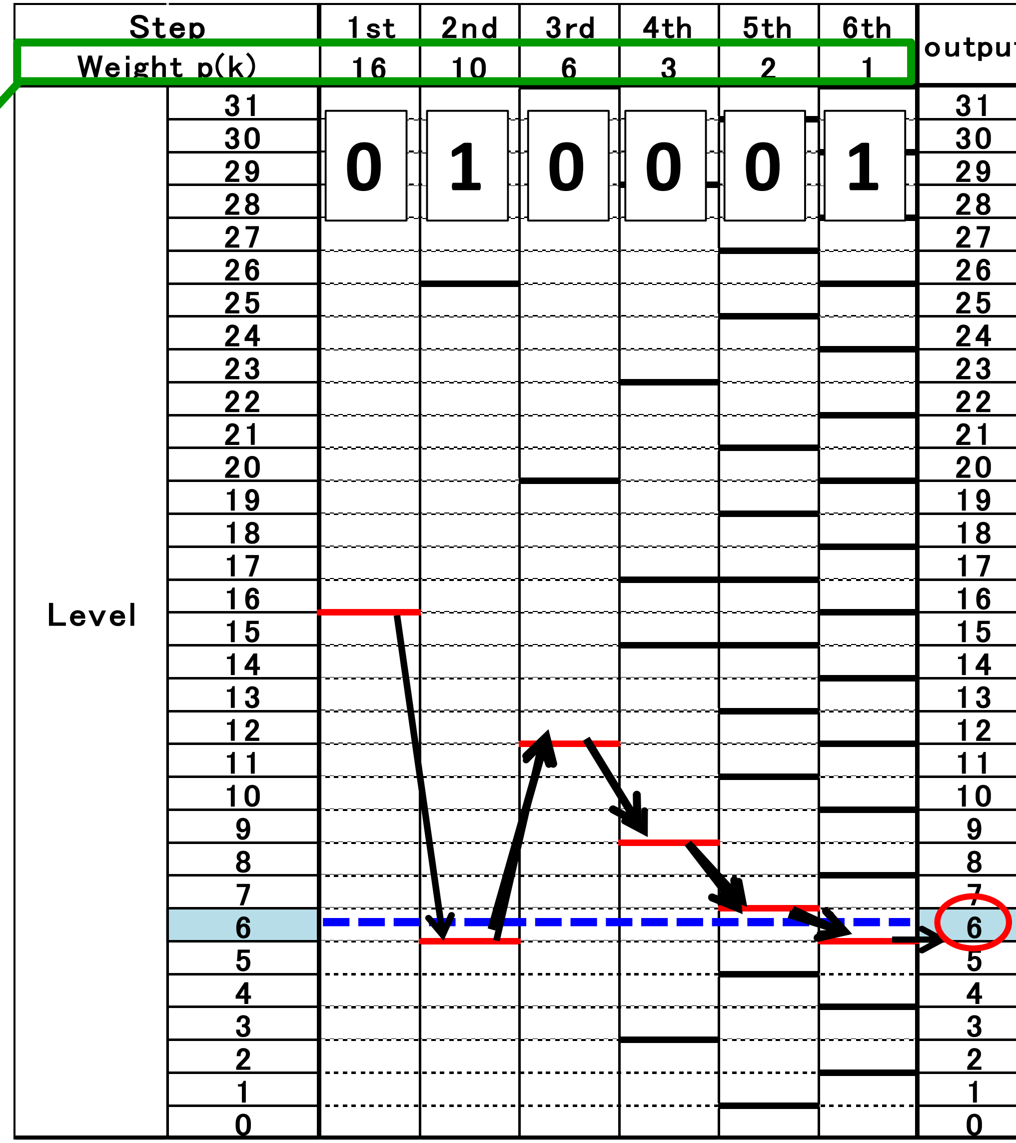
- Analog input : 6.3
- Redundant weight :
  16, 10, 6, 3, 2, 1

Correctable expression

6.3⇒010001⇒6

$$16 - 10 + 6 - 3 - 2 - 1 + 0.5 - 0.5$$

$$= \mathbf{6}$$



Redundancy Design Operation(One Error)

4bit-5step SAR ADC

- Analog input : 6.3
- Redundant weight :
  16, 10, 6, 3, 2, 1

Correctable expression

6.3⇒010001⇒6

Another expression

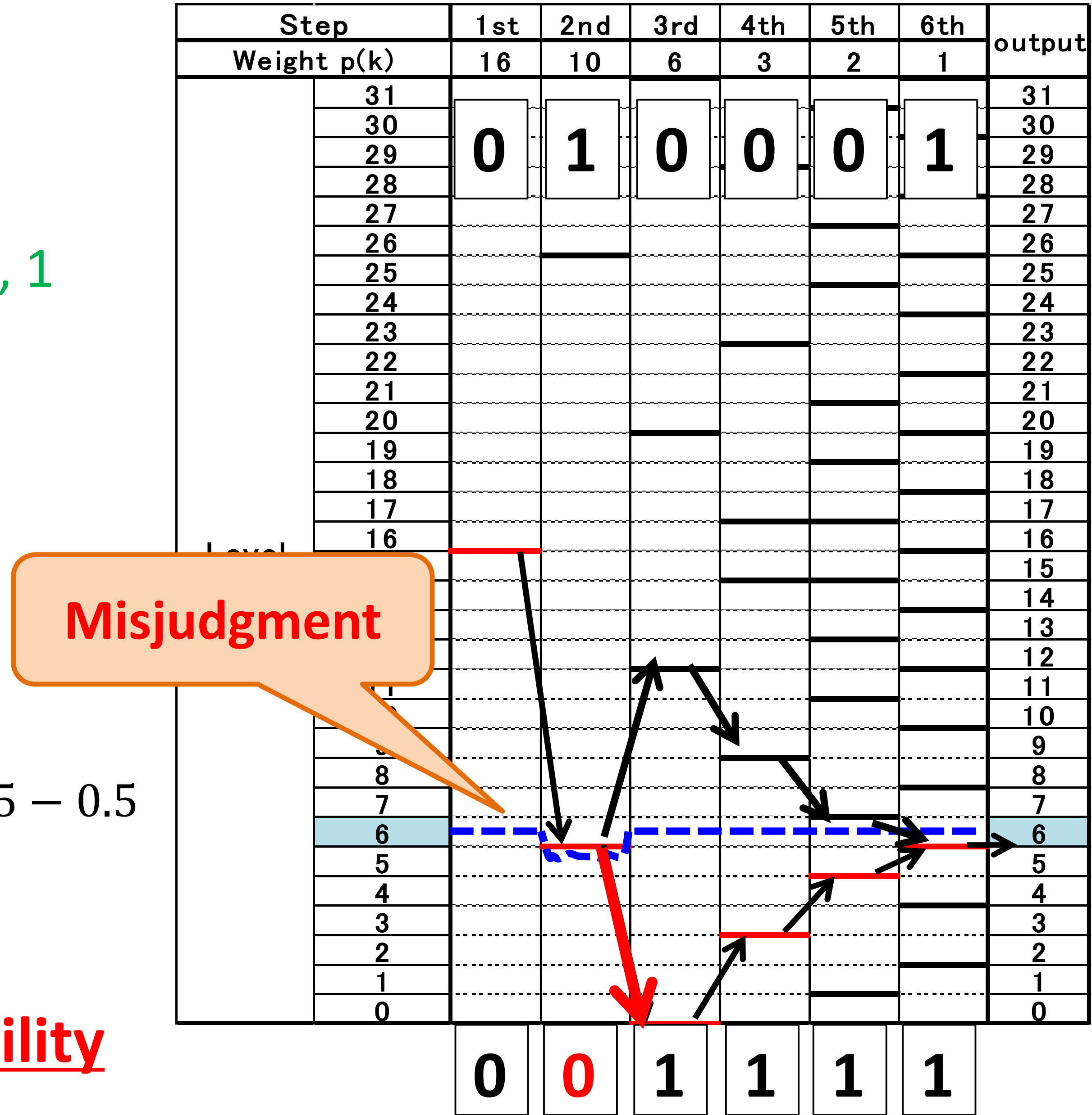
6.3⇒001111⇒6

$16 - 10 - 6 + 3 + 2 + 1 + 0.5 - 0.5$

$= \mathbf{6}$

Error correction

⇨ **High-Reliability**



Fibonacci Weights

We select N bit and M step SAR ADC k-th step reference voltage p(k).
here $p(1) = 2^{N-1}$

Proposed solution

Using Fibonacci sequence for p(k): $p(k) = F_{M-k+1}$

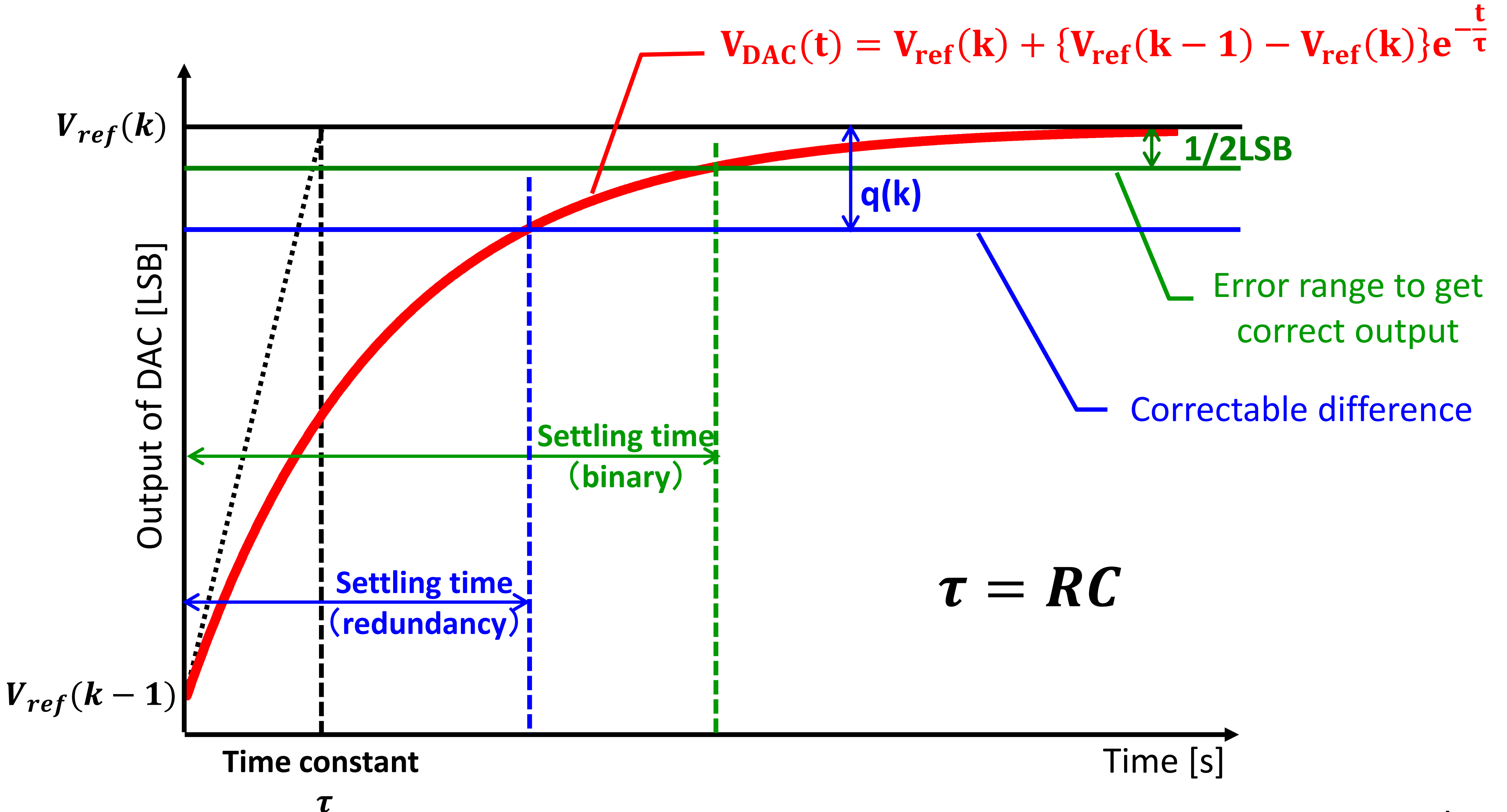
		×2	×2	×2			
Binary Weight	64	32	16	8	4	2	1
		×1.8	×1.8	×1.8			
Radix 1.8 Weight	34.0	18.9	10.5	5.8	3.2	1.8	1
		×1.62	×1.62	×1.62 = Golden ratio			
Fibonacci Weight (Radix 1.62 Weight)	13	8	5	3	2	1	1

Property converging to Golden Ratio

⇨ Realize **Radix 1.62 Weight** by using **only integer** !

Internal DAC Settling Time

DAC Settling model by a simple first-order RC circuit



SAR ADC Speed and DAC Settling

Redundancy → **Incomplete settling**

5bit SAR ADC

Binary search (complete settling)

Step1	Step2	Step3	Step4	Step5

time

Redundant search (incomplete settling)

Step1	Step2	Step3	Step4	Step5	Step6	Step7

Error correction time

Fibonacci search (incomplete settling)

Step1	Step2	Step3	Step4	Step5	Step6	Step7

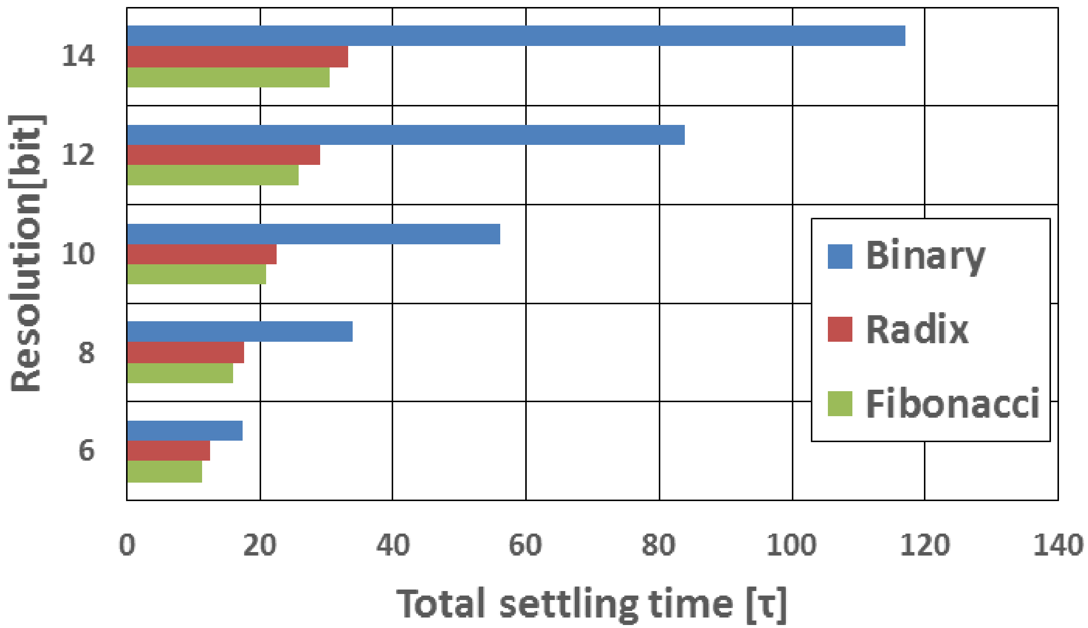
Error correction time

The shortest AD conversion time !!

Fibonacci Weights SAR ADC

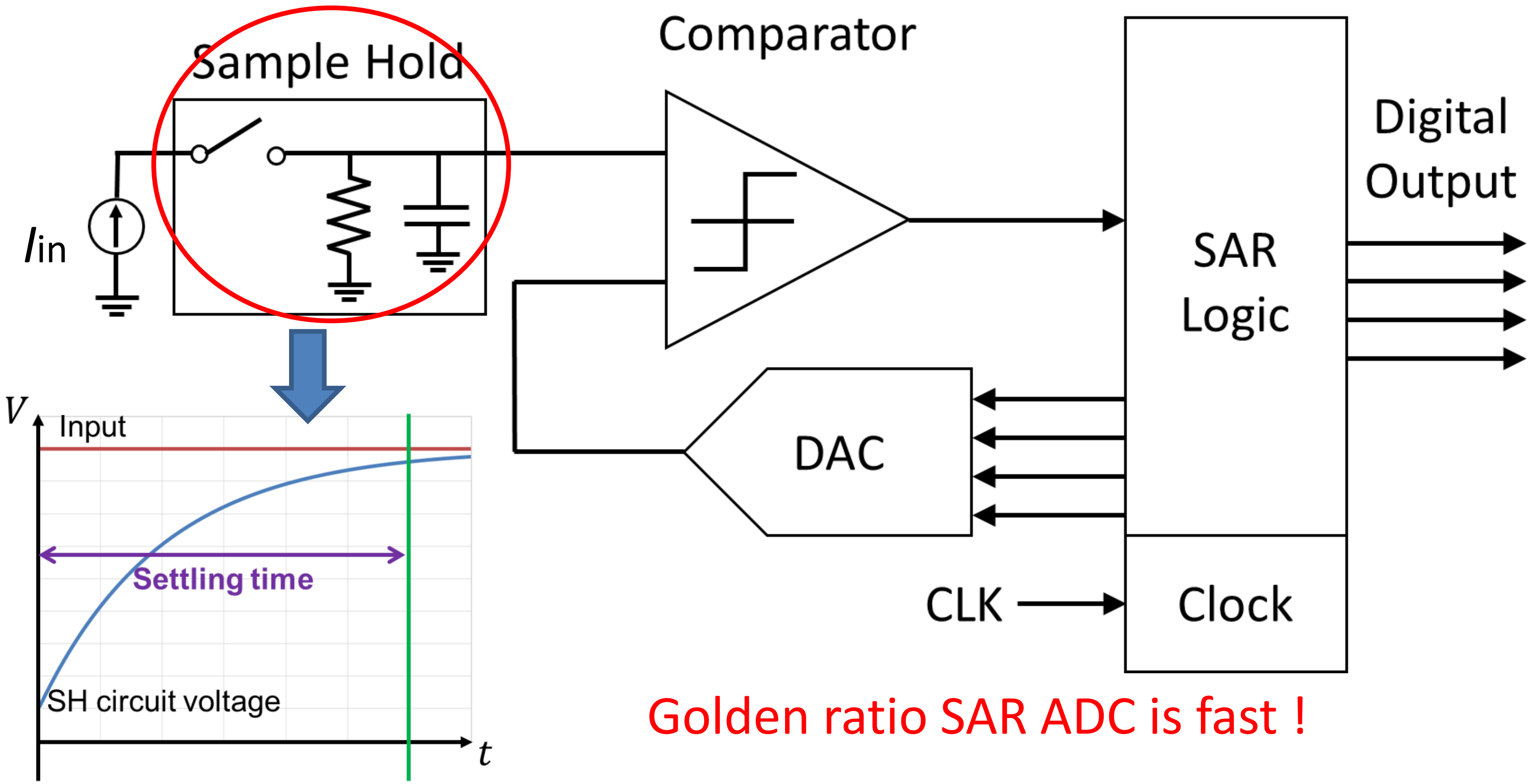
We have found the following:

- **Reliable**
  Comparator decision errors can be recovered with redundancy.
- **Fastest SAR AD Conversion**
  In case the internal DAC incomplete settling is considered.



Minute Current Measurement

SH Circuit Settling time → Long



Golden ratio SAR ADC is fast !

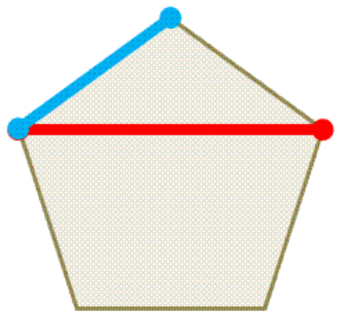
[2] H. Arai, H. Kobayashi, et. al., " Redundant SAR ADC Algorithm for Minute Current Measurement", Journal of Technology and Social Science (accepted)

Contents

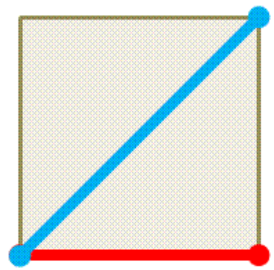
[3] Y. Kobayashi, T. Arafune, S. Shibuya, H. Kobayashi "SAR ADC Algorithm With Redundancy Using Pseudo-Silver-Ratio", IEEJ Trans. Electronics, Information and Systems (Feb. 2017)

Silver Ratio : Japanese Beauty

$$\sqrt{2}/1 = 1.414 = \textbf{Silver Ratio}$$

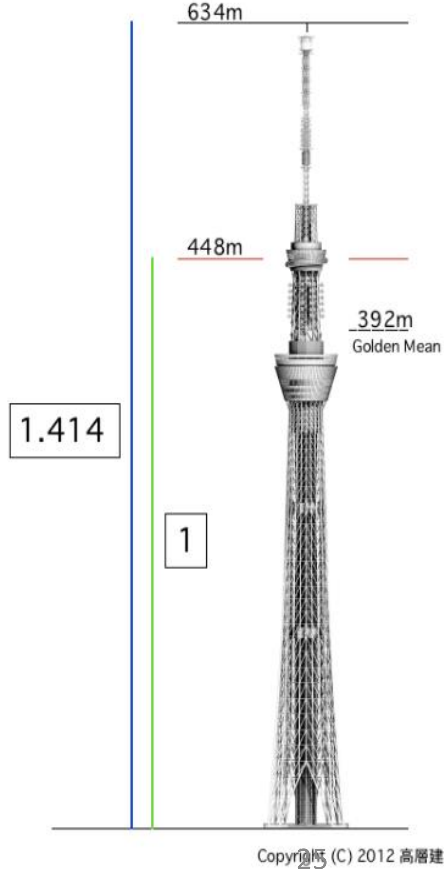


Golden ratio
1 : 0.618

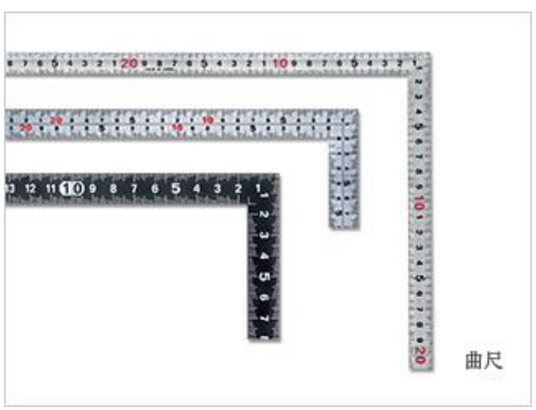


Silver ratio
1 : 1.414

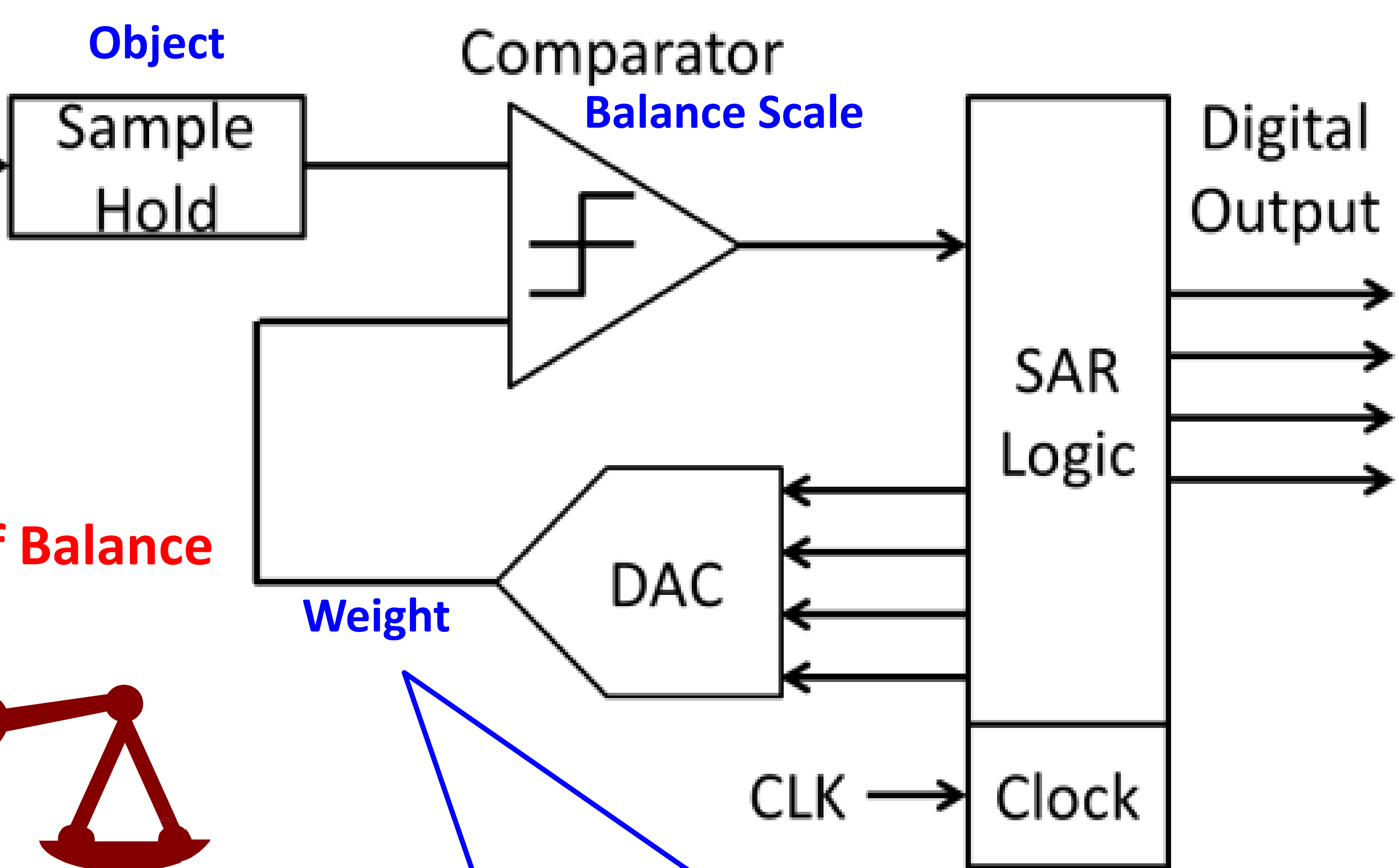
Tokyo Sky Tree



Japanese old tools



Silver Ratio SAR ADC



Based on
Principle of Balance

Silver ratio weight
(1 , 1 , 1 , 2, 2, 4, 4, 8, 8, 16,..

Silver Ratio Weighted SAR ADC

5-bit 8-step SAR ADC

p(M) =1

p(M-1) =1

p(M-2) =1

p(M-3) =2

p(M-4) =2

p(M-5) =4

p(M-6) =4

p(M-7) =8

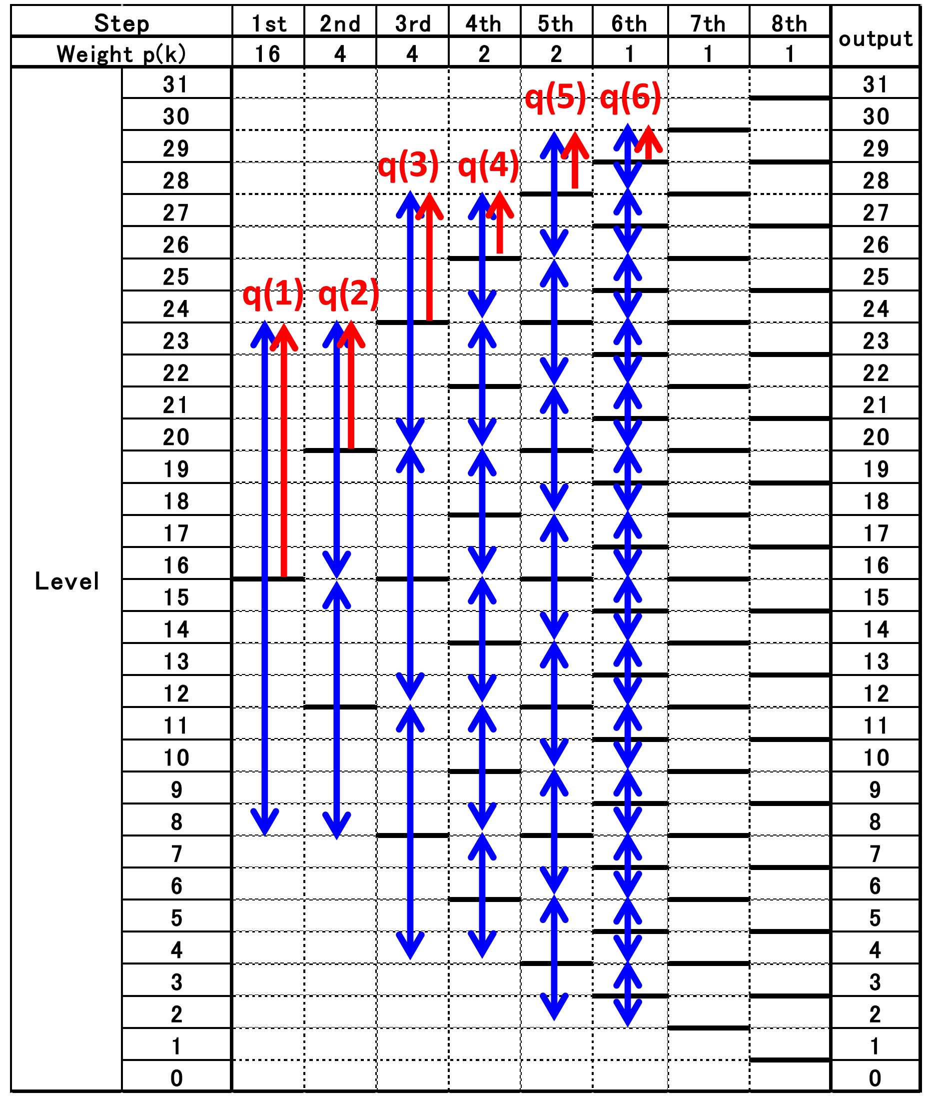
p(M-8) =8

p(M-9) =16

p(M-10) =16

×1 ×2 ×1 ×2 ×1 ×2

$\times\sqrt{2}$ $\times\sqrt{2}$ $\times\sqrt{2}$ $\times\sqrt{2}$ $\times\sqrt{2}$ $\times\sqrt{2}$



Fixed clock period: Golden ratio SAR ADC is the fastest.

Variable clock period: Silver ratio SAR ADC is the fastest.

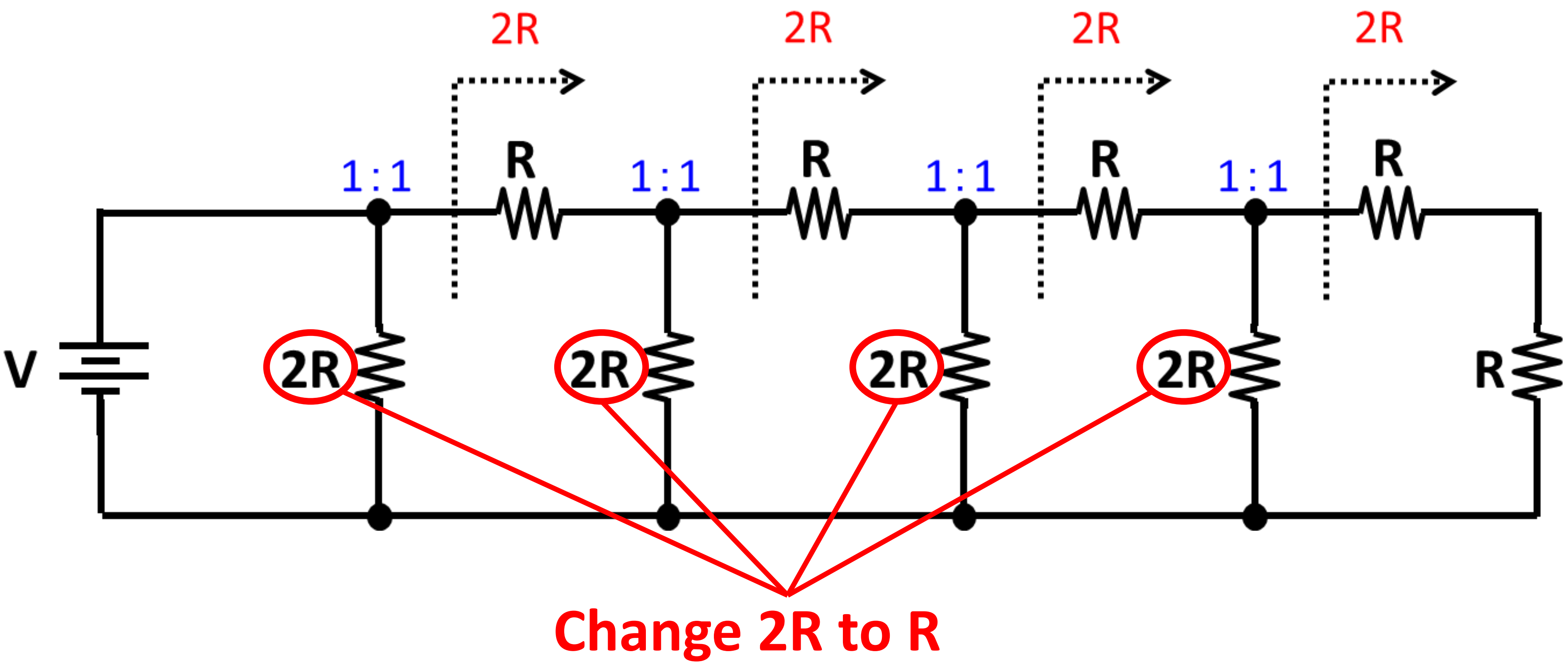
Contents

[4] Y. Kobayashi, H. Kobayashi, et. al.,
"SAR ADC Design Using Golden Ratio Weight Algorithm", ISCIT (Oct. 2015).
[5] T. Arafune, Y. Kobayashi, H. Kobayashi , et. al., "Fibonacci Sequence Weighted SAR ADC Algorithm and its DAC Topology," IEEE ASICON (Nov. 2015).

R-2R Resistor Ladder

R-2R Resistor ladder network

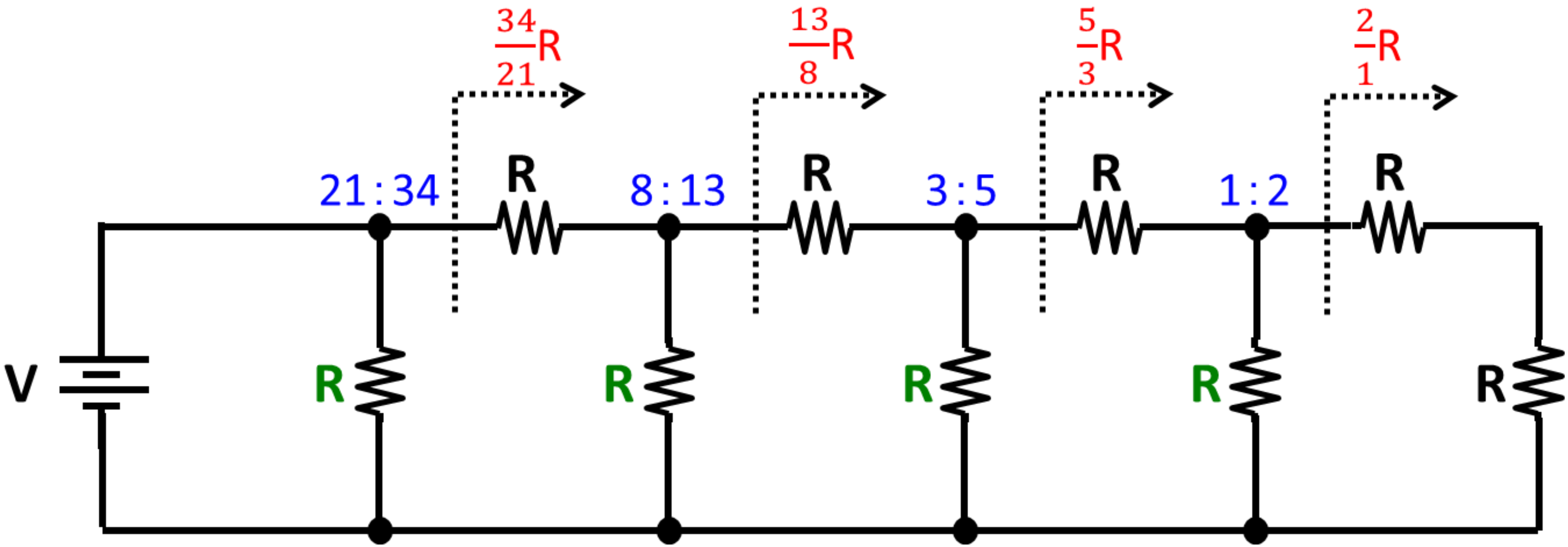
- Divides current into halves in each node
- Used for **binary** DAC



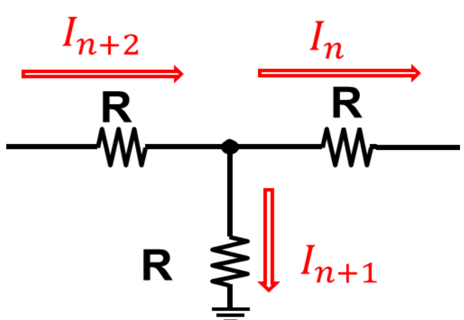
R-R Resistor Ladder

<u>R-R Resistor ladder network</u>

- Divides current into **Fibonacci ratio** in each node



<u>Principle</u>



$$I_{n+2} = I_{n+1} + I_n$$

$$F_{n+2} = F_{n+1} + F_n$$

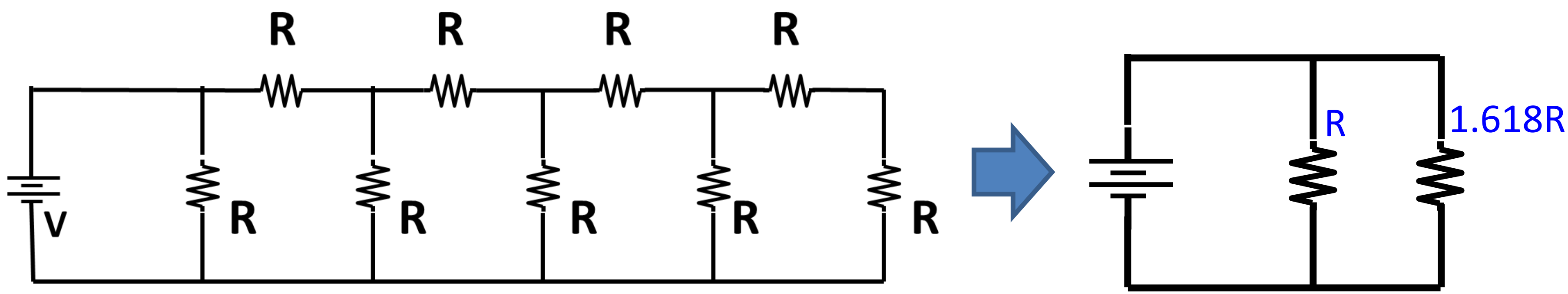
Golden Divide Resistor Ladder Network

R-R Resistor ladder network

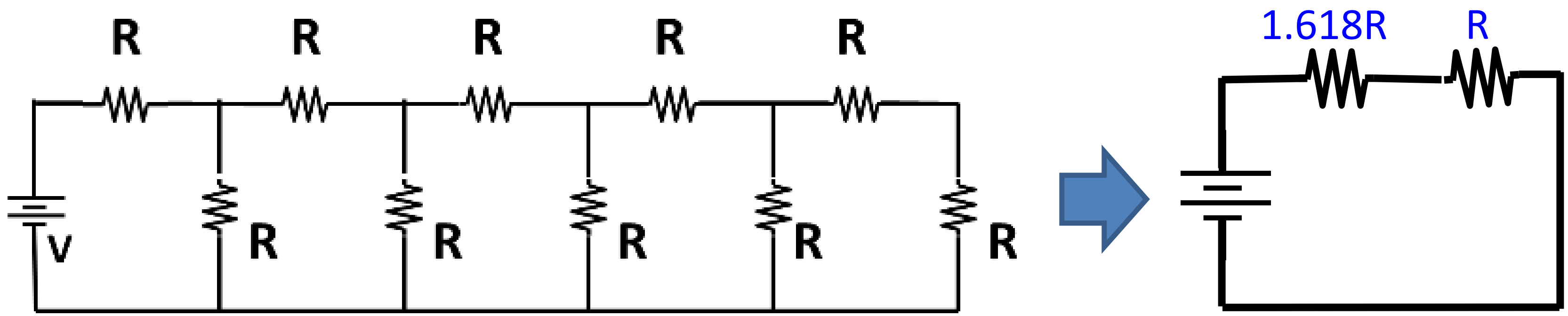
- Realize Golden divide of voltage or current
- High precision Golden divide

⇒Use for Fibonacci redundant SAR ADC

◆Current-dividing circuit



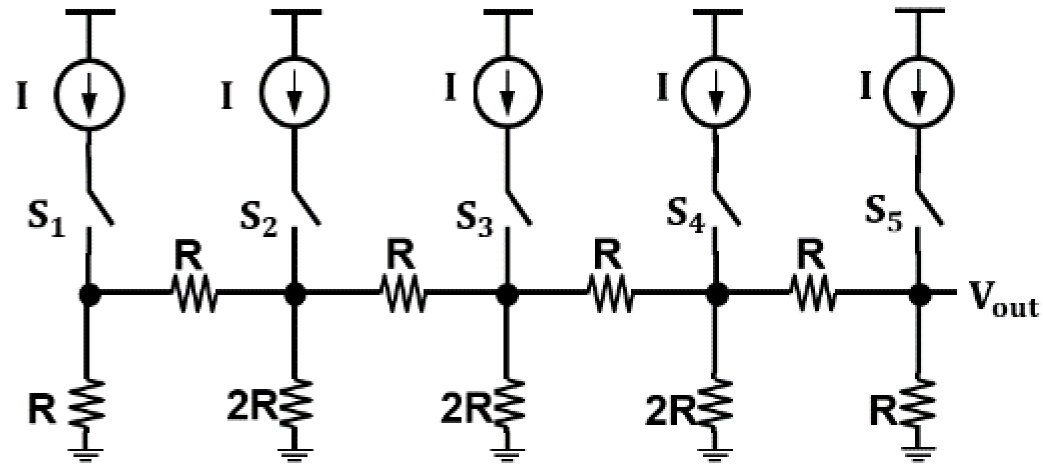
◆Voltage-dividing circuit



Proposal of Fibonacci DAC

R-2R resistor ladder

generates **binary** voltage



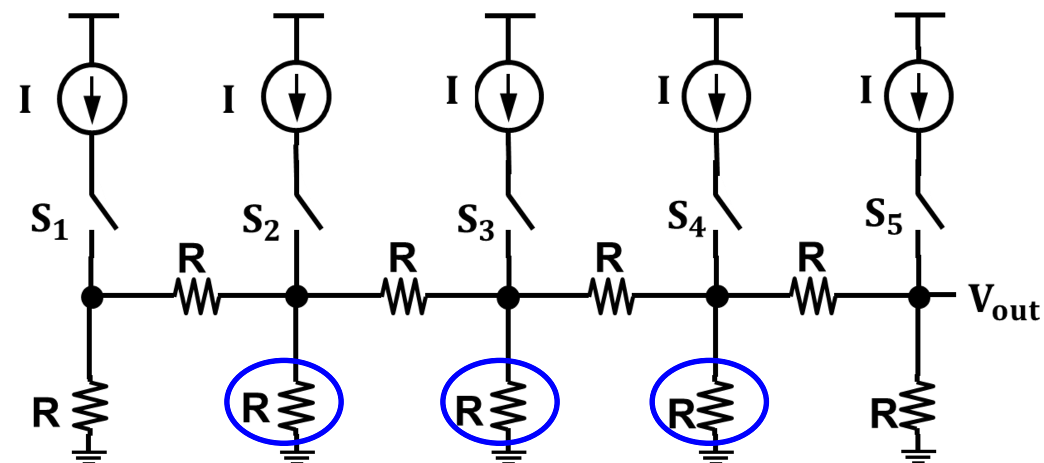
Only use R

Proposal

R-R resistor ladder

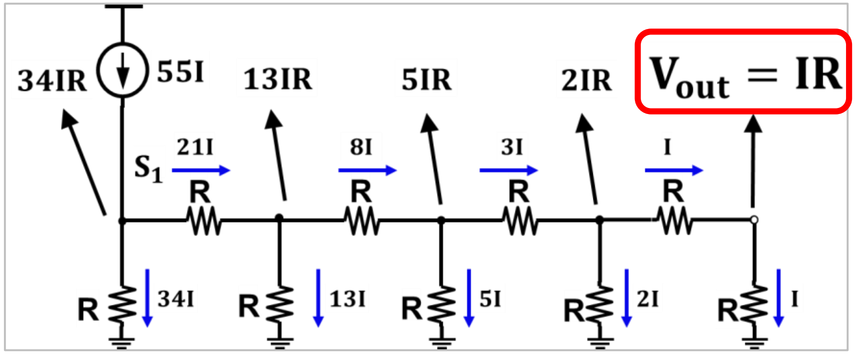
generates **Fibonacci** voltage

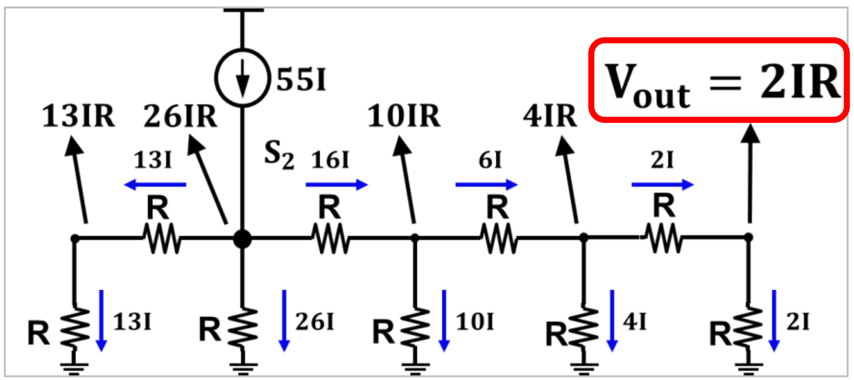
Realize Fibonacci DAC
by using simple circuit

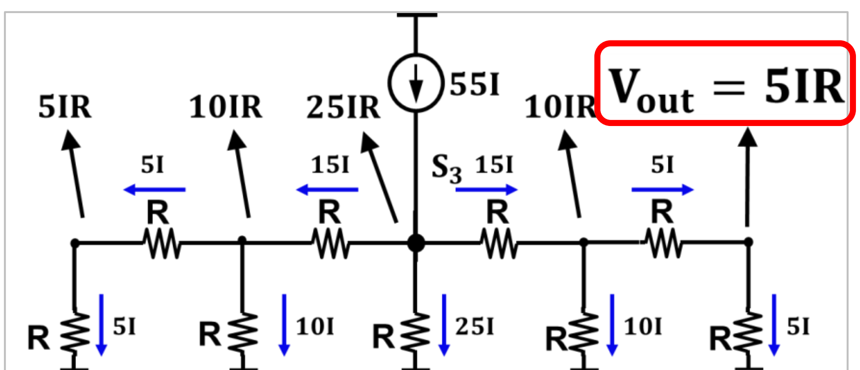


R-R resistor ladder network

Analysis of Fibonacci DAC







Output voltage

$$V_{out}(m) = \left(\frac{F_{2(N-m)+1}}{F_{2N}}\right) IR$$

N: the number of nodes

m: a connected node number from the left

Odd term of Fibonacci sequence

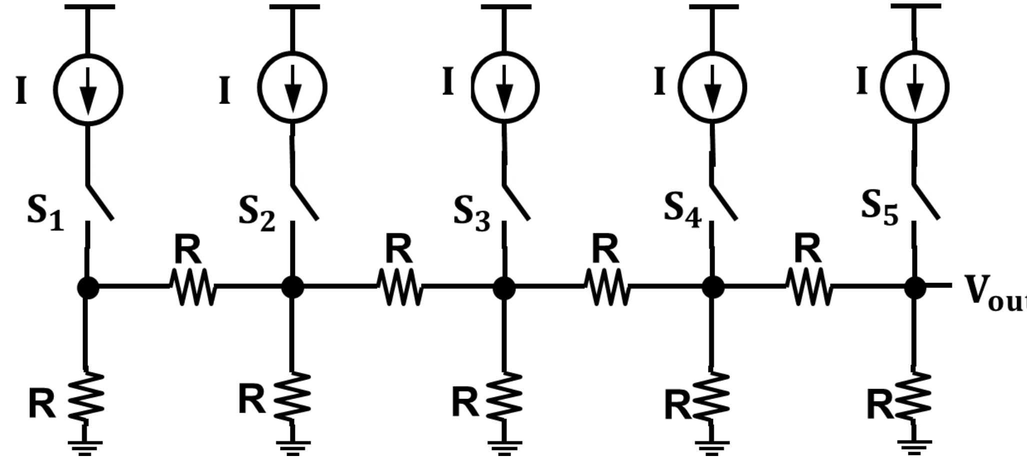
1, 1, 2, 3, 5, 8,...

We also need even term

Proposal of R//R Fibonacci DAC

R-R resistor ladder

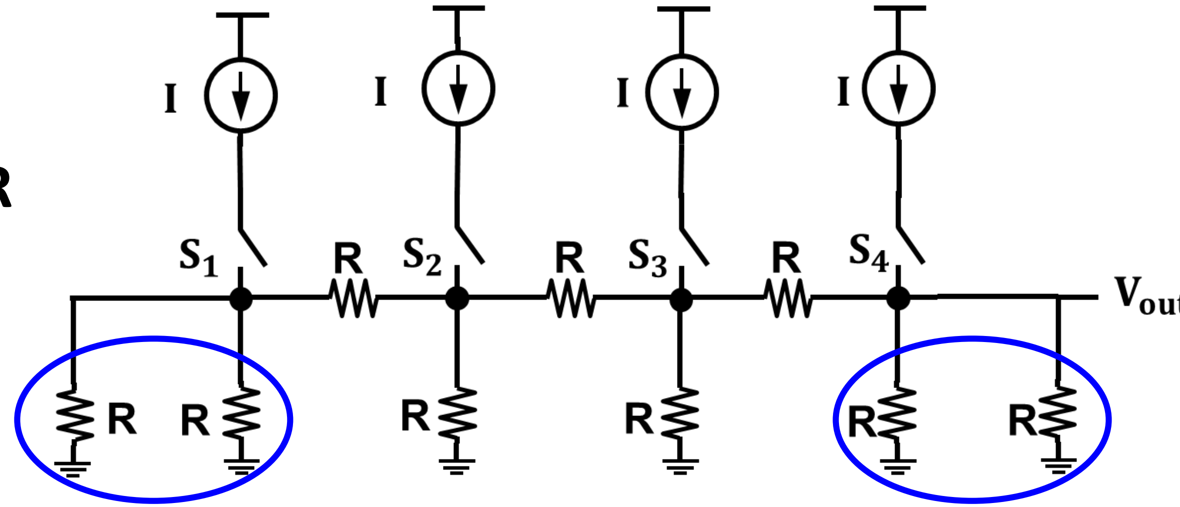
Generate Fibonacci voltage of **odd** term



Change terminal resistor to parallel resistors

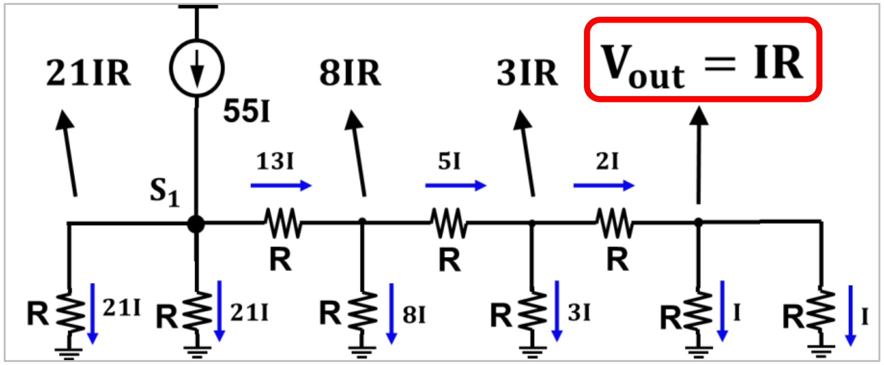
Proposal

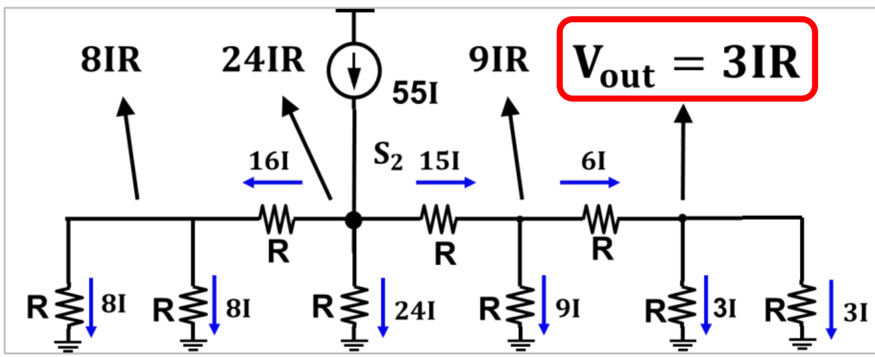
R-R resistor ladder with terminations of R//R

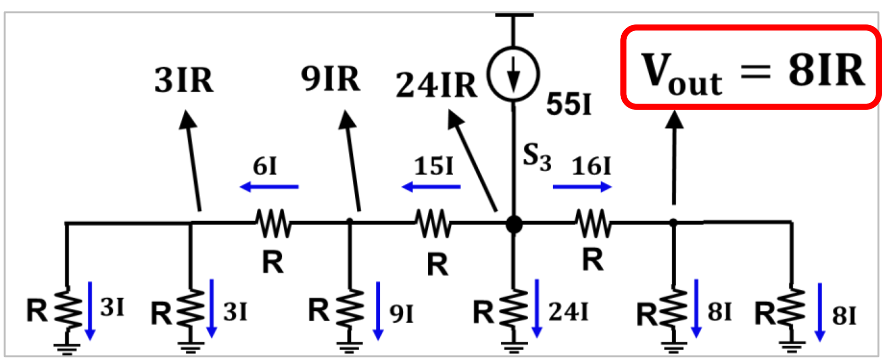


Generate Fibonacci voltage of **even** term

Analysis of Fibonacci DAC







Output voltage

$$V_{out}(m) = \left(\frac{F_{2(N-m+1)}}{F_{2(N+1)}}\right) IR$$

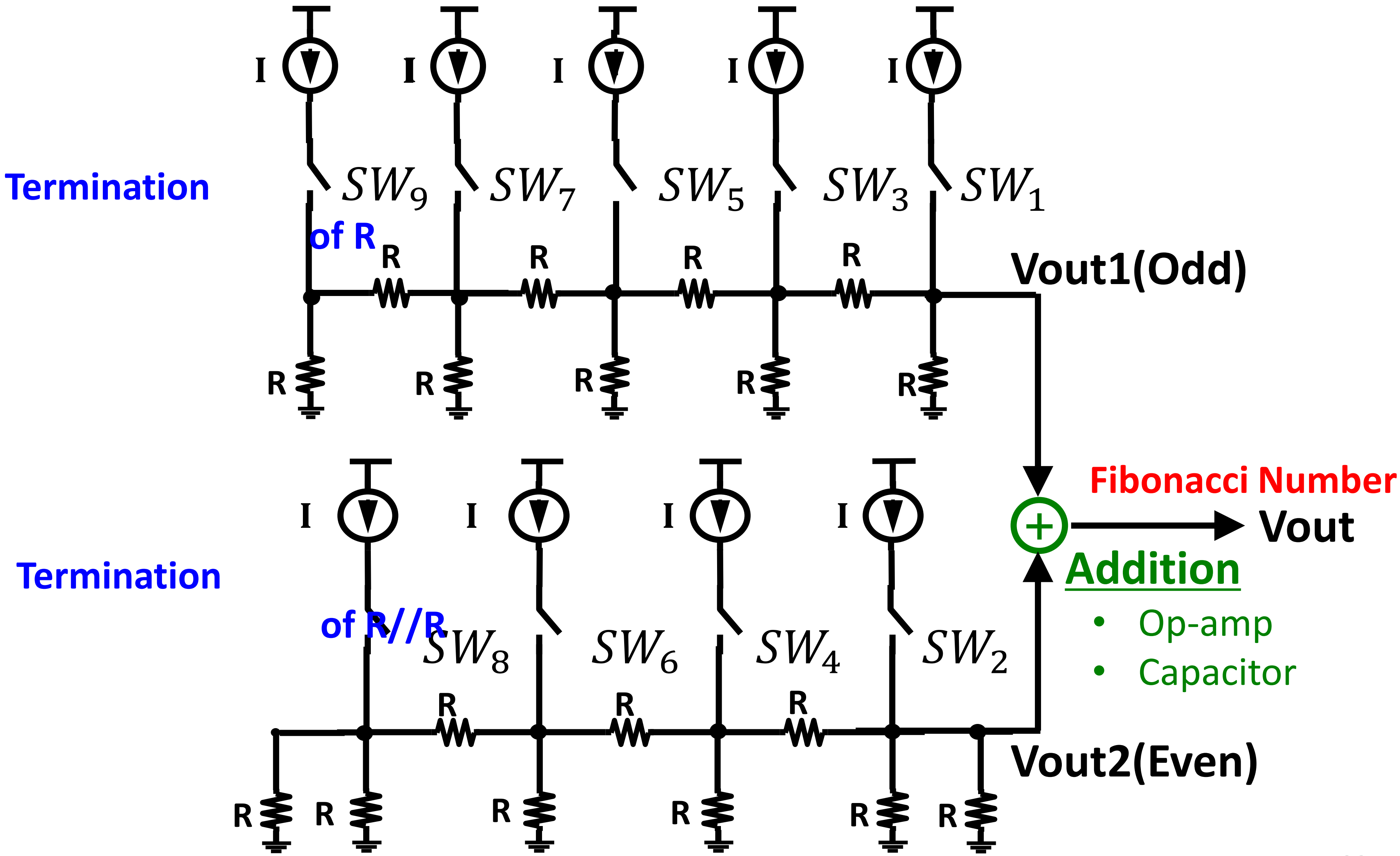
N: the number of nodes

m: a connected node number from the left

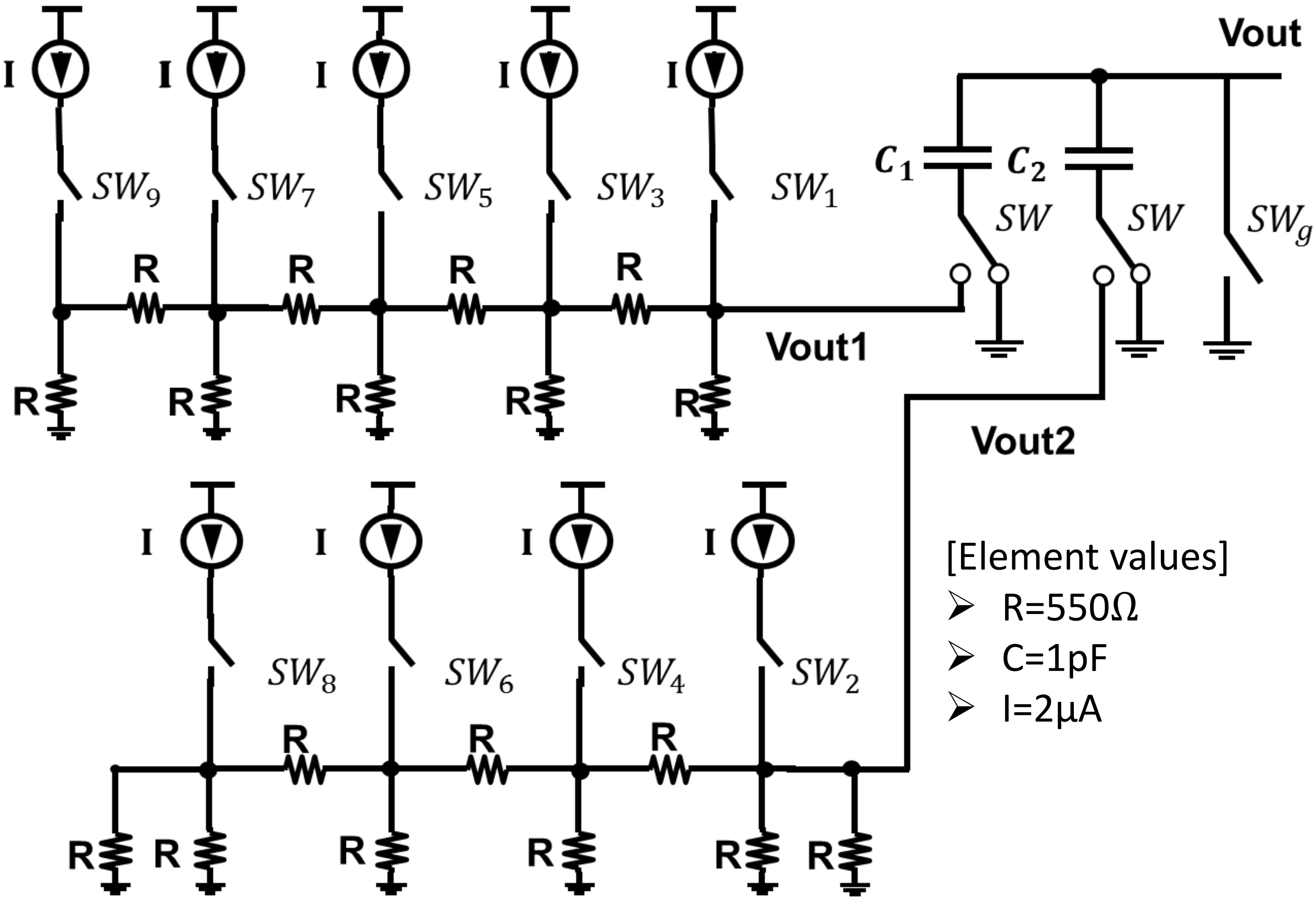
Even term of Fibonacci sequence

1, **1**, 2, **3**, 5, **8**,…

Fibonacci DAC



Fibonacci DAC Simulation



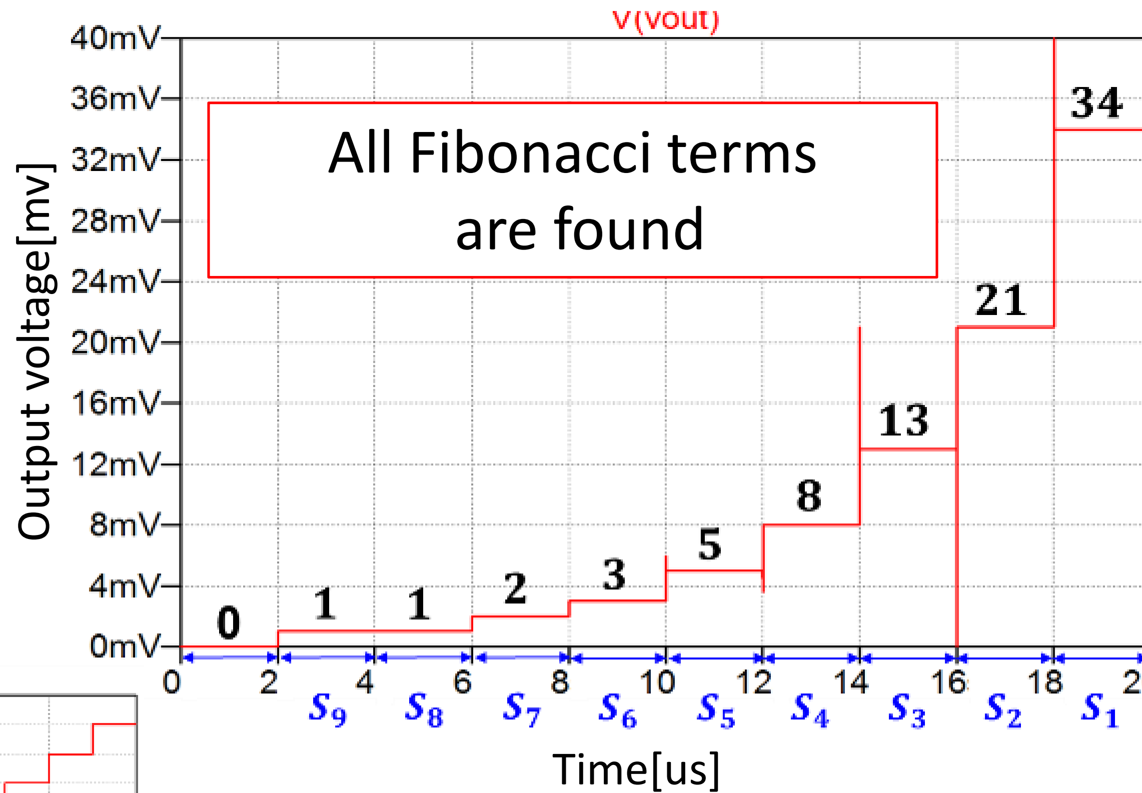
[Element values]

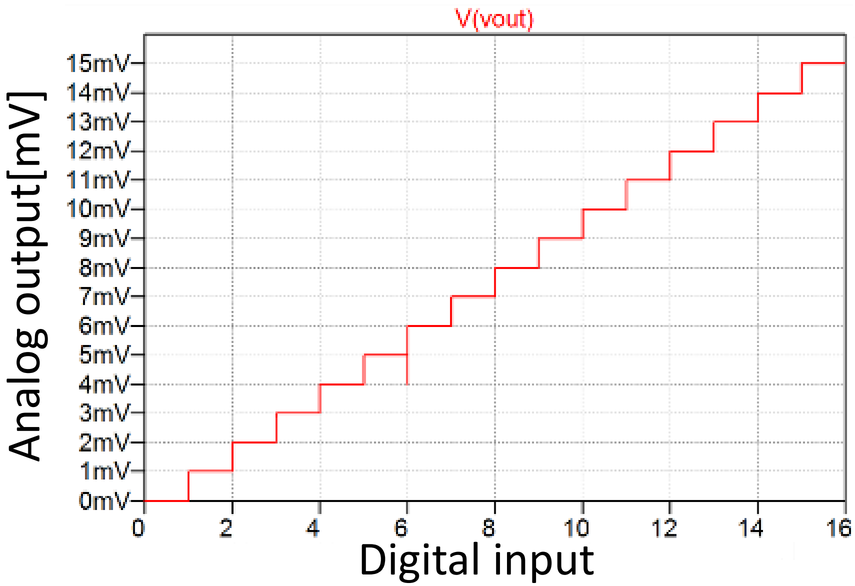
- R=550Ω
- C=1pF
- I=2μA

SPICE Simulation Verification

Operation simulation

Each switch corresponds to a Fibonacci term





A-D conversion simulation

Combination of current sources realizes DAC function

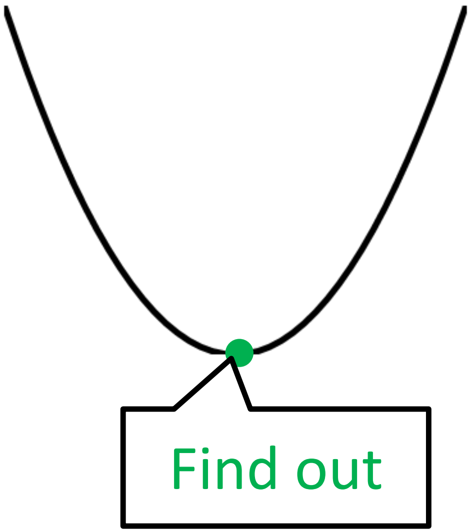
Fibonacci DAC is realized

Contents

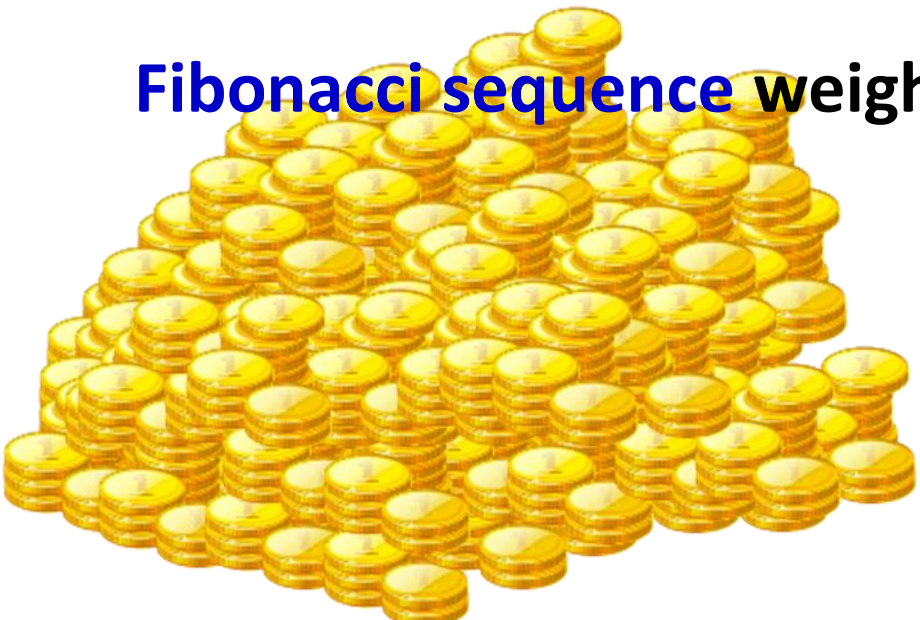
[6] H. Arai, H. Kobayashi, et. al., "Fibonacci Sequence Weighted SAR ADC as Golden Section Search", IEEE International Symposium on Intelligent Signal Processing and Communication Systems, Xiamen (Nov. 2017)

New Discovery

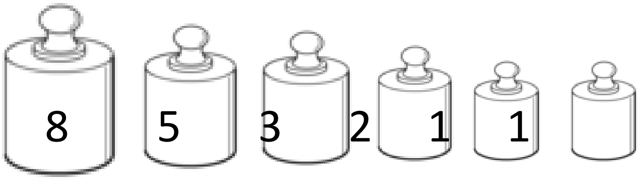
SAR ADC based on
golden section search
using unimodal function



equivalent



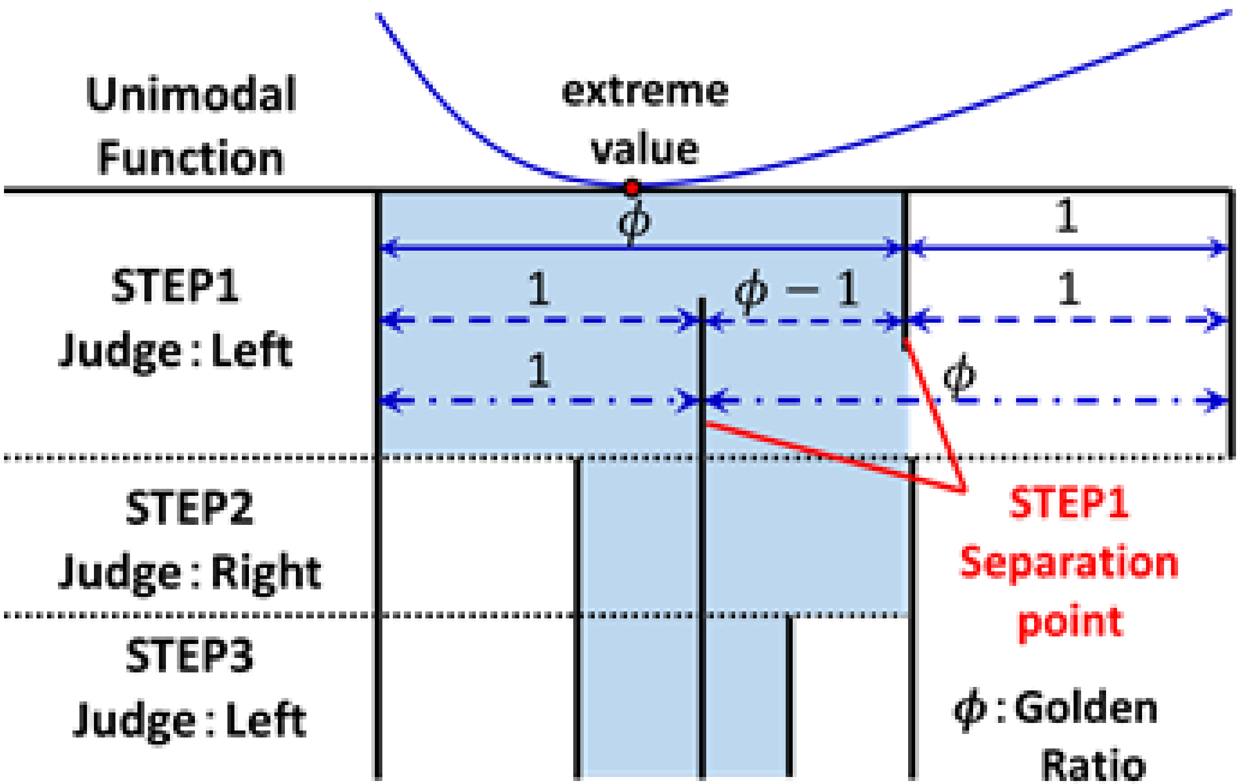
Fibonacci sequence weighted SAR ADC



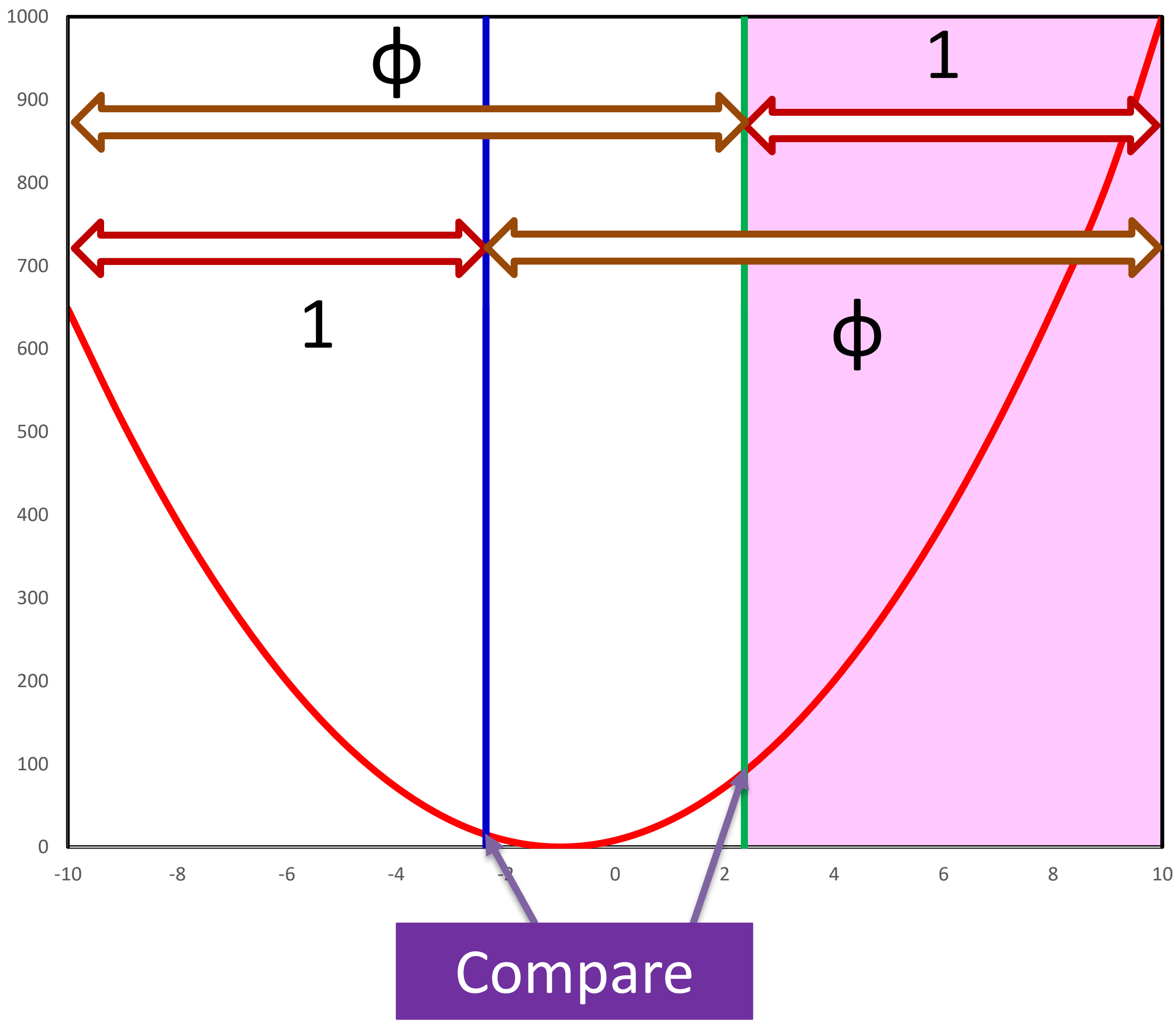
Golden Section Search

Finding of effectively extreme value of unimodal function

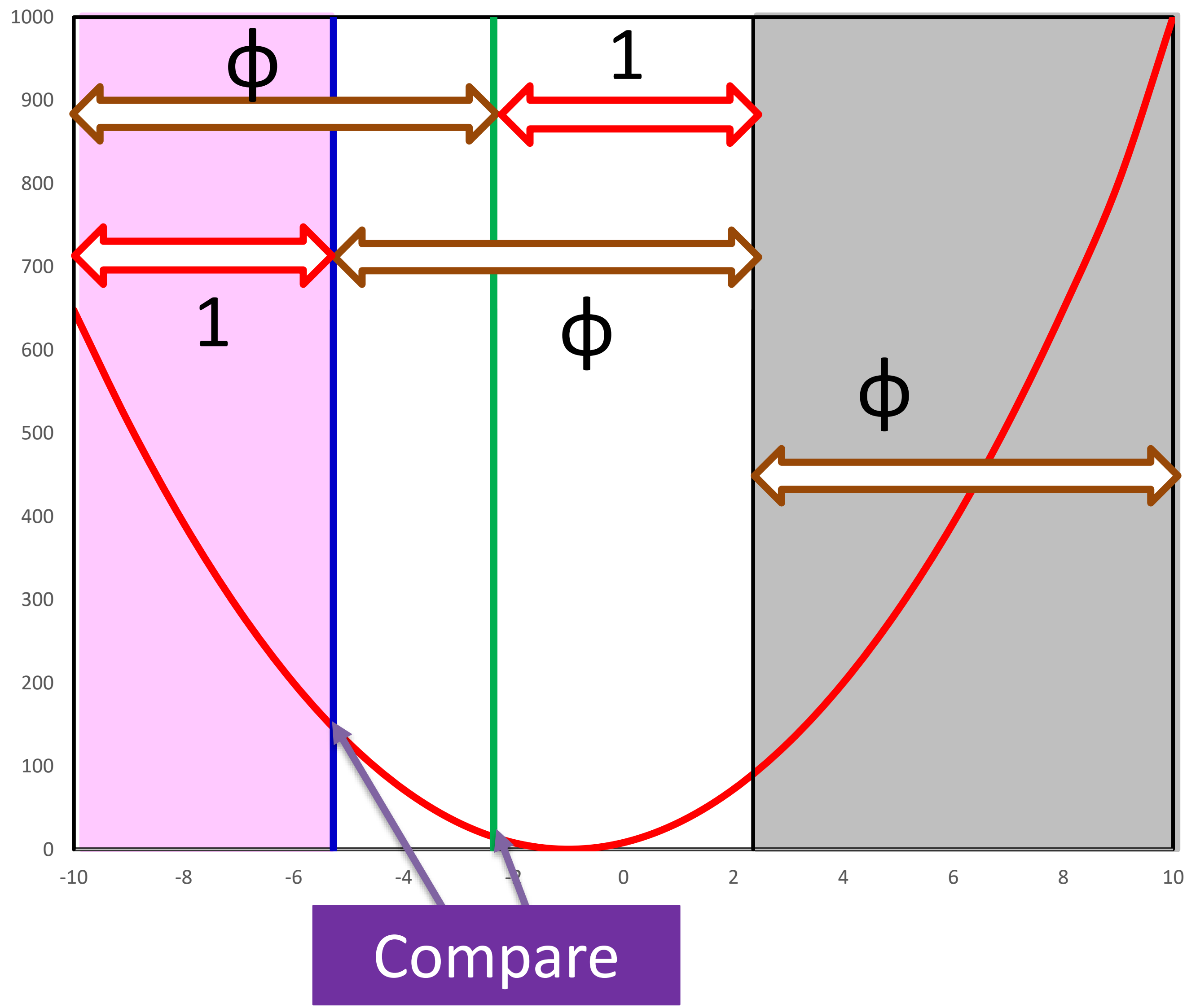
Division ratio = Golden ratio



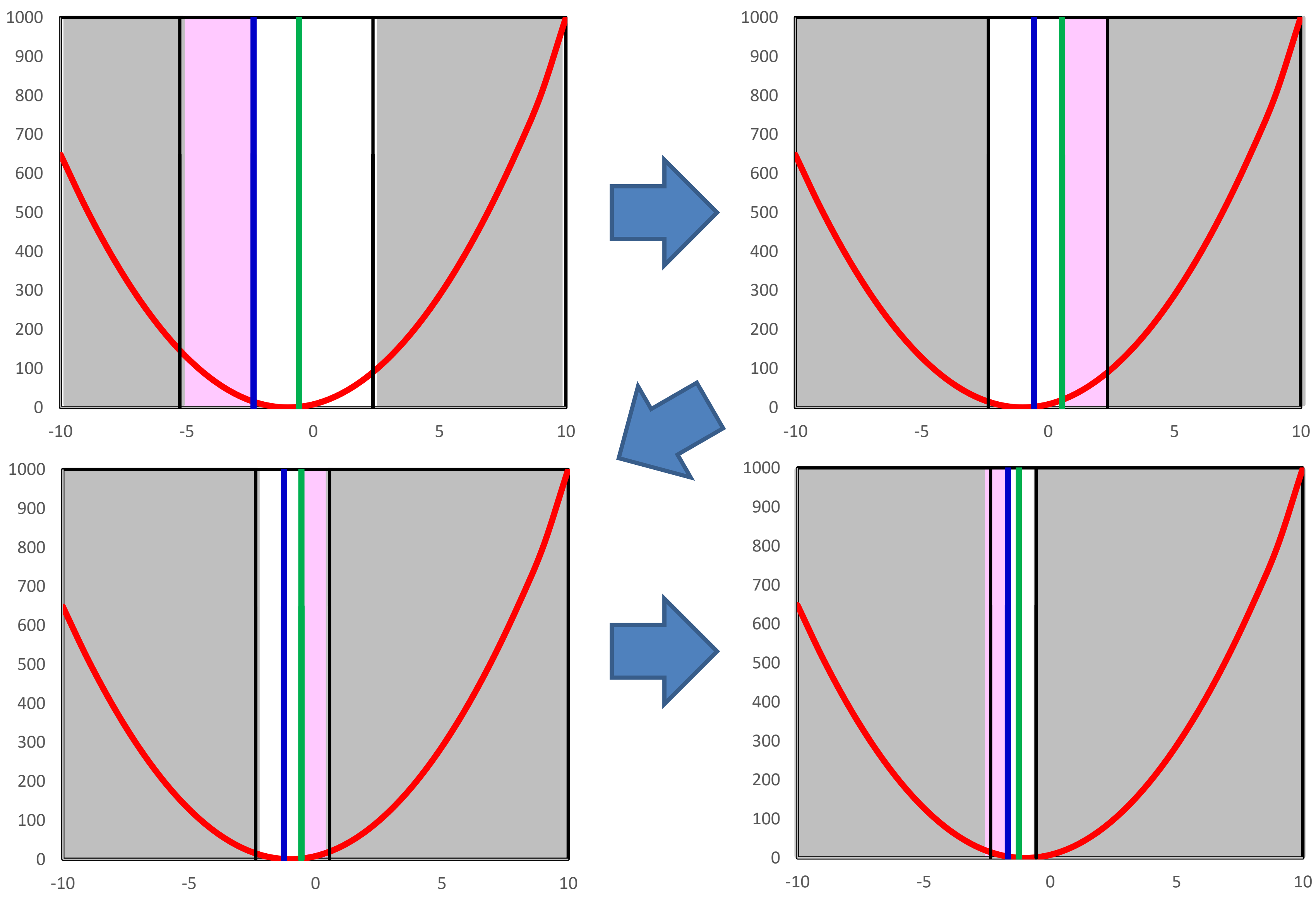
Golden Section Search : Operation (1)



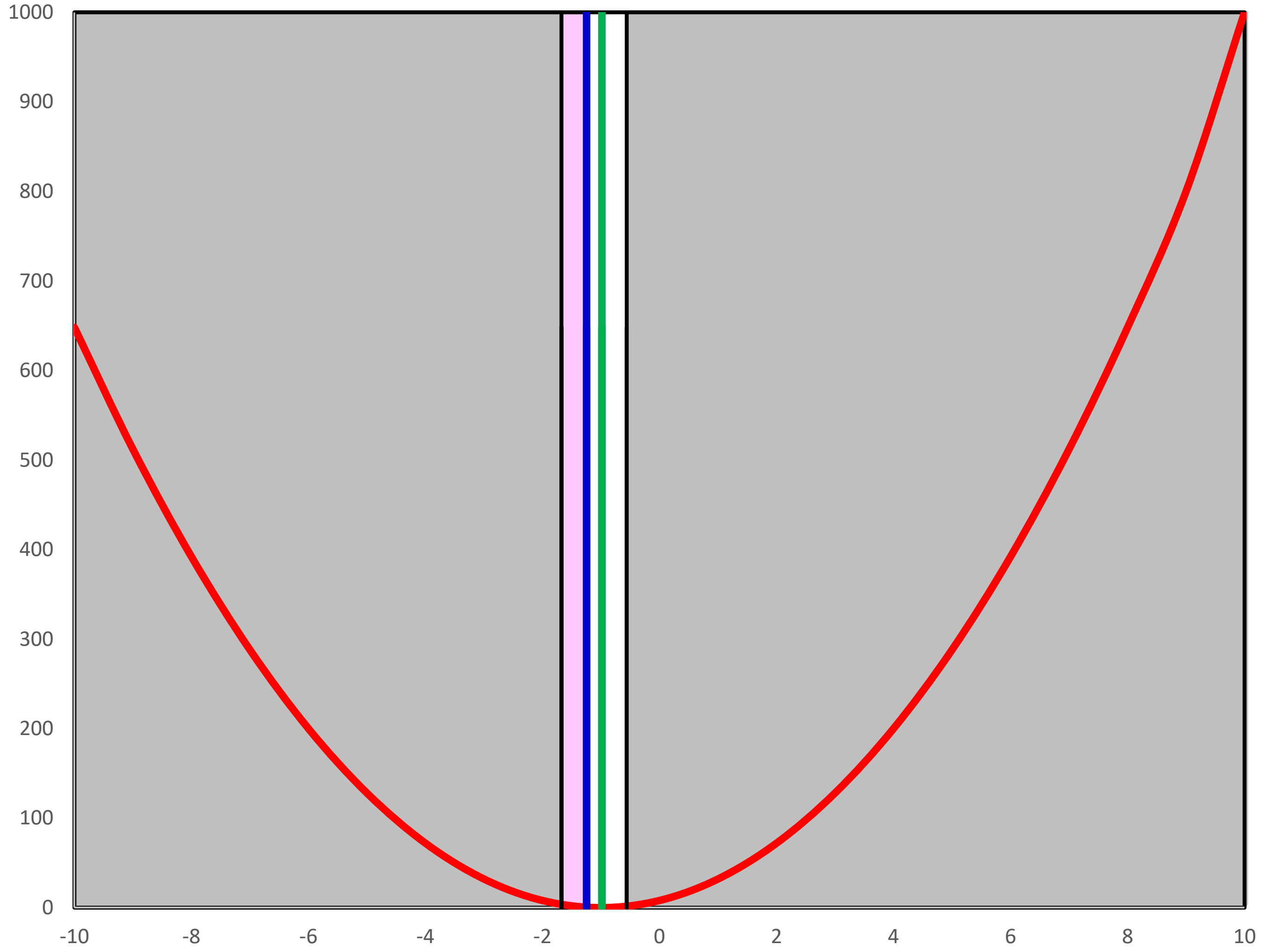
Golden Section Search : Operation (2)



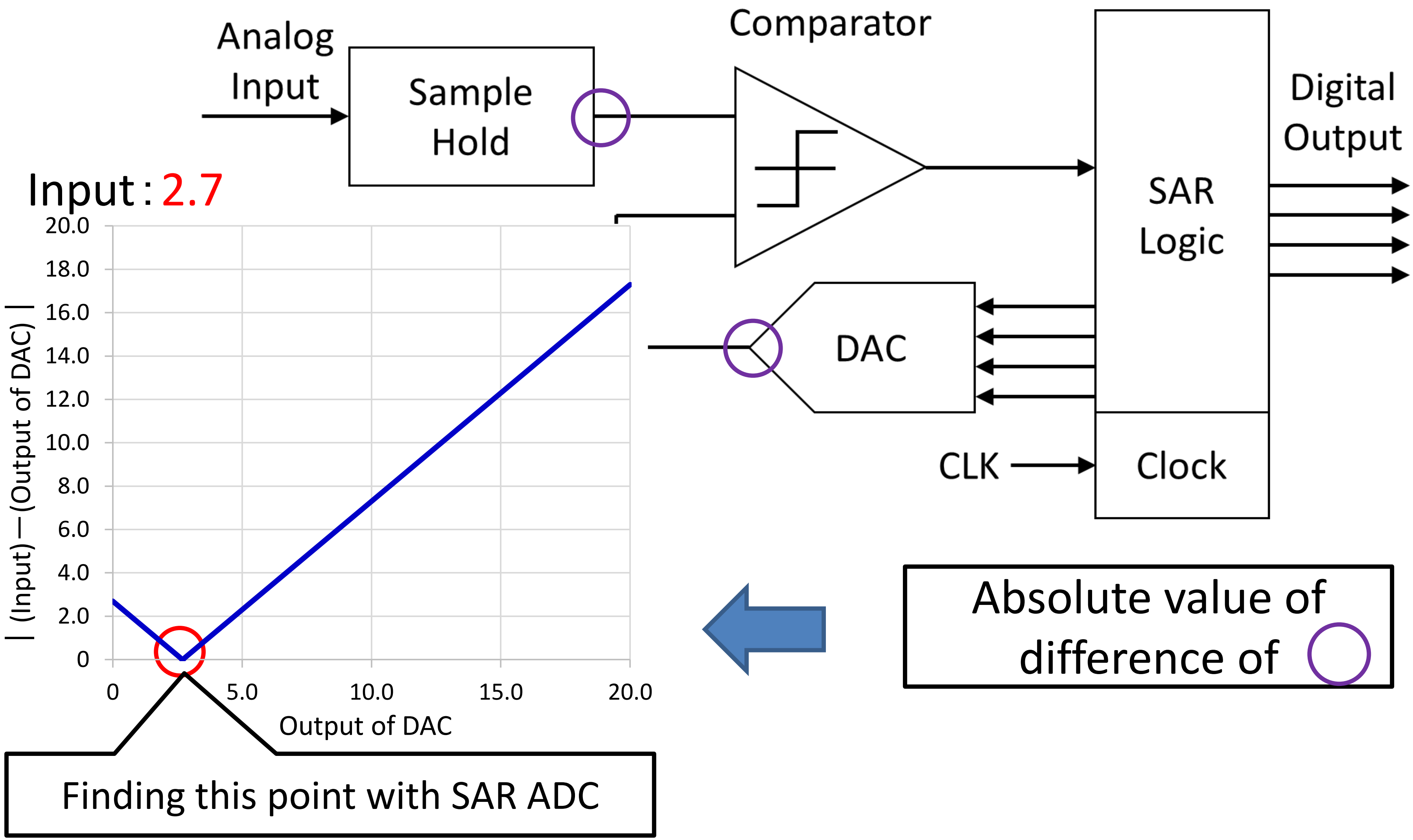
Golden Section Search : Operation (3)



Golden Section Search : Operation (4)

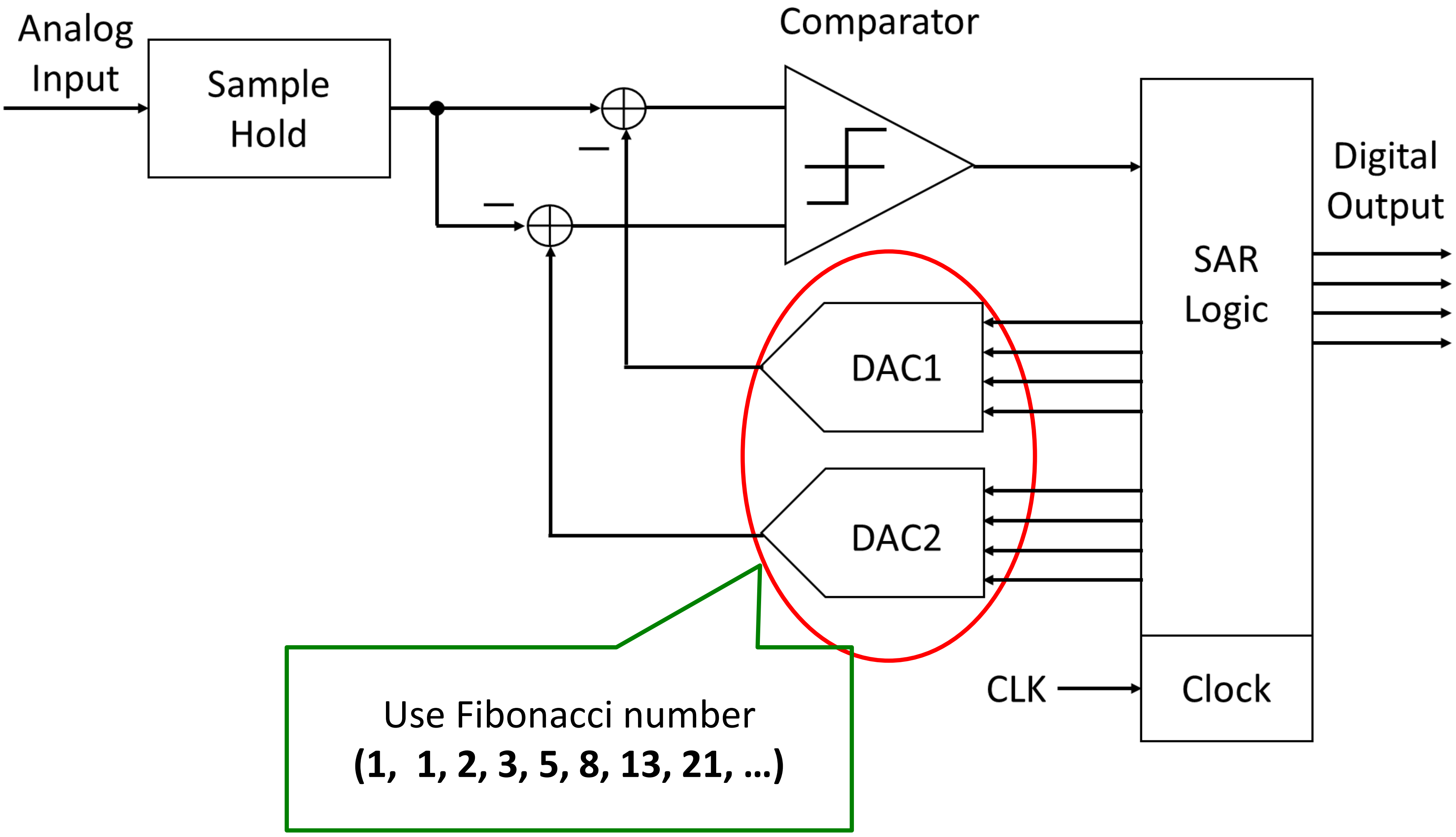


SAR ADC Based on Fibonacci Search

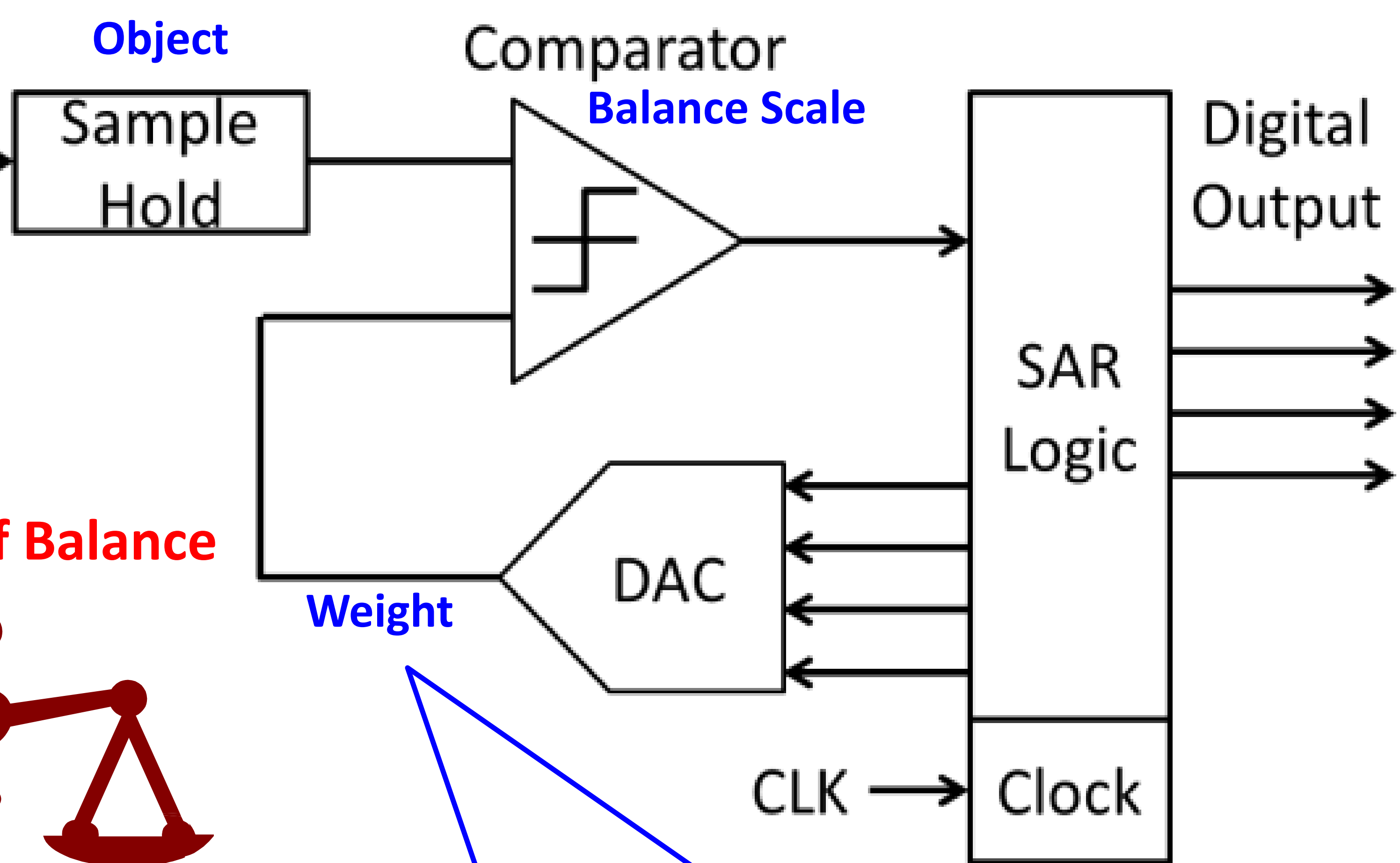


Unimodal function with local minimum → Use Fibonacci search

SAR ADC Based on Fibonacci Search



Golden Ratio SAR ADC



Based on
Principle of Balance

Golden ratio weight
(1 , 2 , 3 , 5, 8, 13, 21, 34, …)

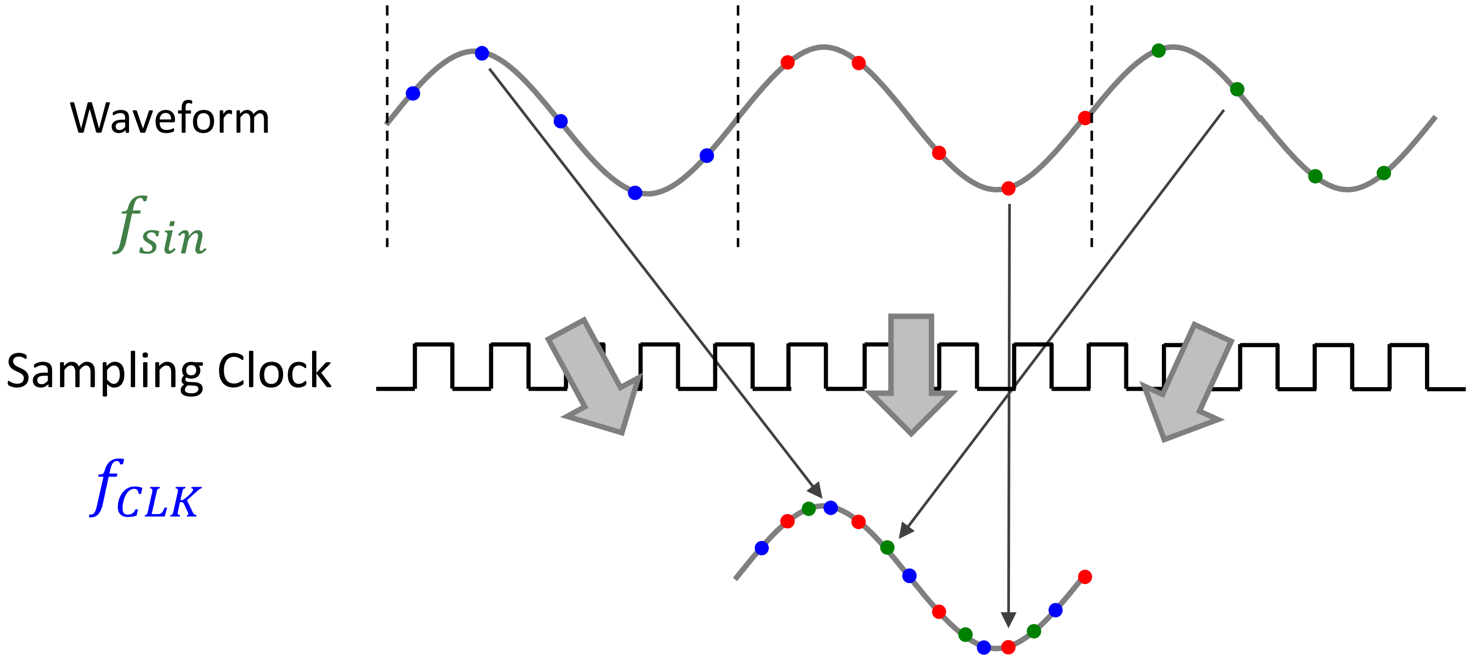
Contents

[7] Y. Sasaki, H. Kobayashi, "Integral-type Time-to-Digital Converter", IEEE International Conference on Solid-State and Integrated Circuit Technology, Qingdao (Nov. 2018)

[8] Y. Sasaki, Y. Zhao, A. Kuwana, H. Kobayashi, "Highly Efficient Waveform Acquisition Condition in Equivalent-Time Sampling System", IEEE Asian Test Symposium, Hefei, Anhui (Oct. 2018)

Equivalent-Time Sampling

Digital oscilloscope

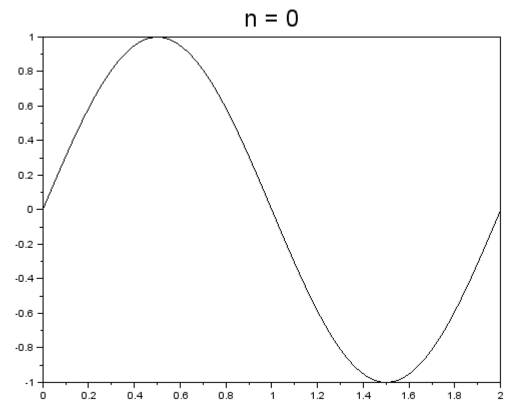


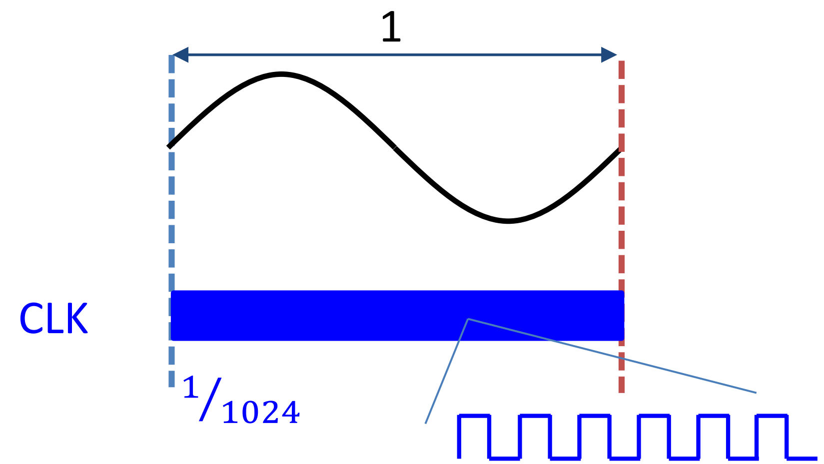
Waveform Missing : Case 1

Low frequency f_{sin} case

$$f_{CLK} \gg f_{sin}$$

Slow phase progress



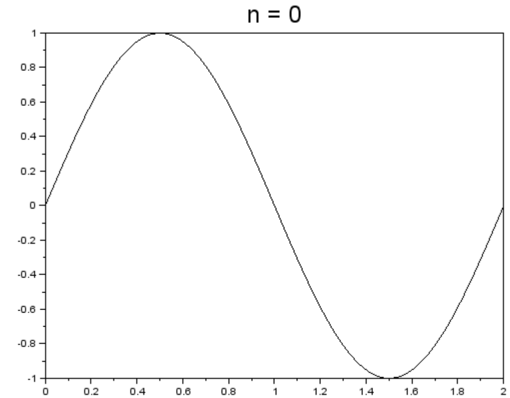


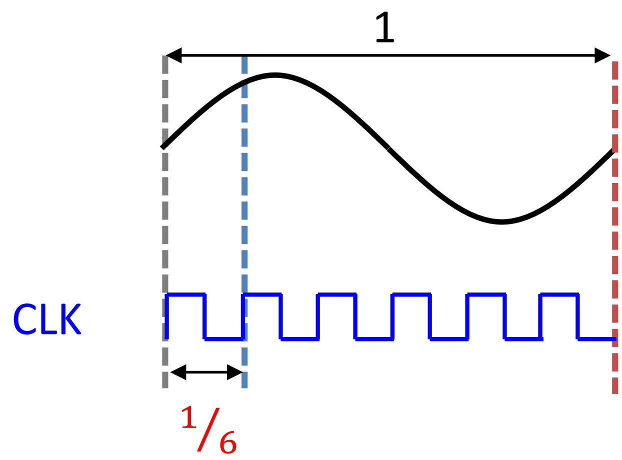
Waveform Missing : Case 2

Rational ratio f_{CLK}/f_{sin} case

$$f_{CLK} \approx \frac{1}{\alpha} f_{sin}$$

$$\left(\alpha = 1, \frac{1}{2}, \frac{1}{3}, \frac{2}{3}, \cdots, \frac{1}{6}, \cdots\right)$$

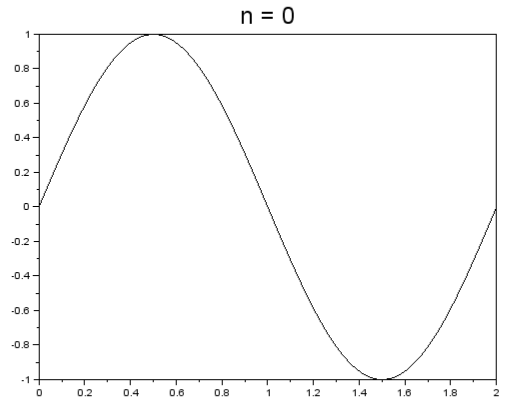


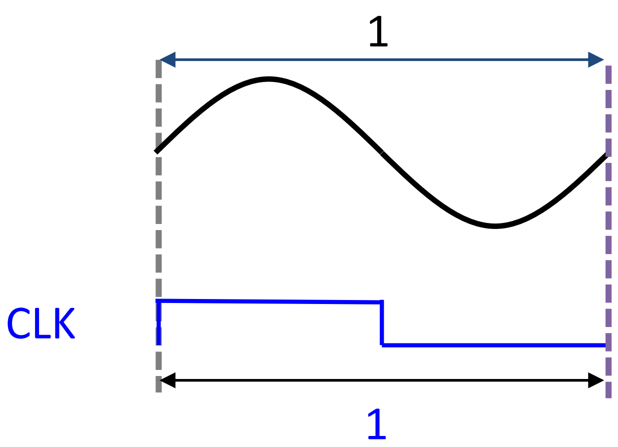


Waveform Missing : Case 3

Almost the same frequency case

$f_{CLK} \approx f_{sin}$

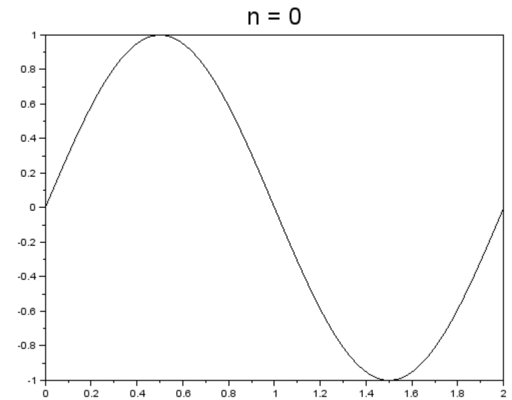


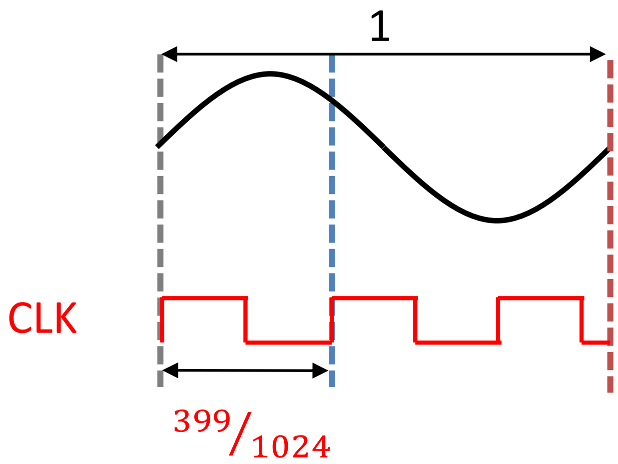


Efficient Waveform Acquisition

Proper relationship

f_{CLK} *and* f_{sin}

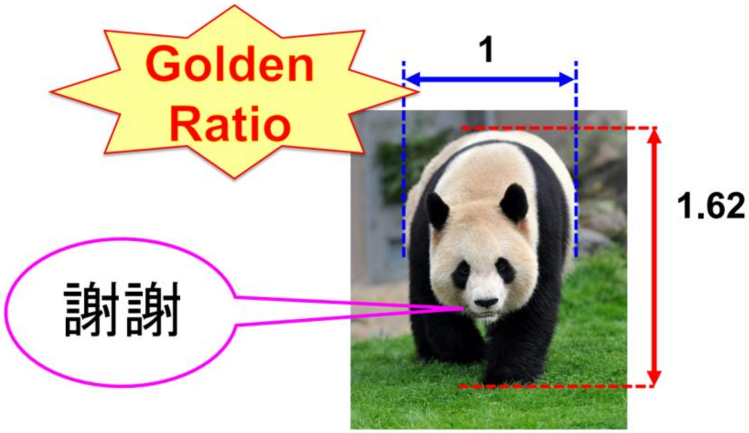




New Finding

In case f_{CLK} / f_{sin} = <u>1.6181..</u>

Golden ratio

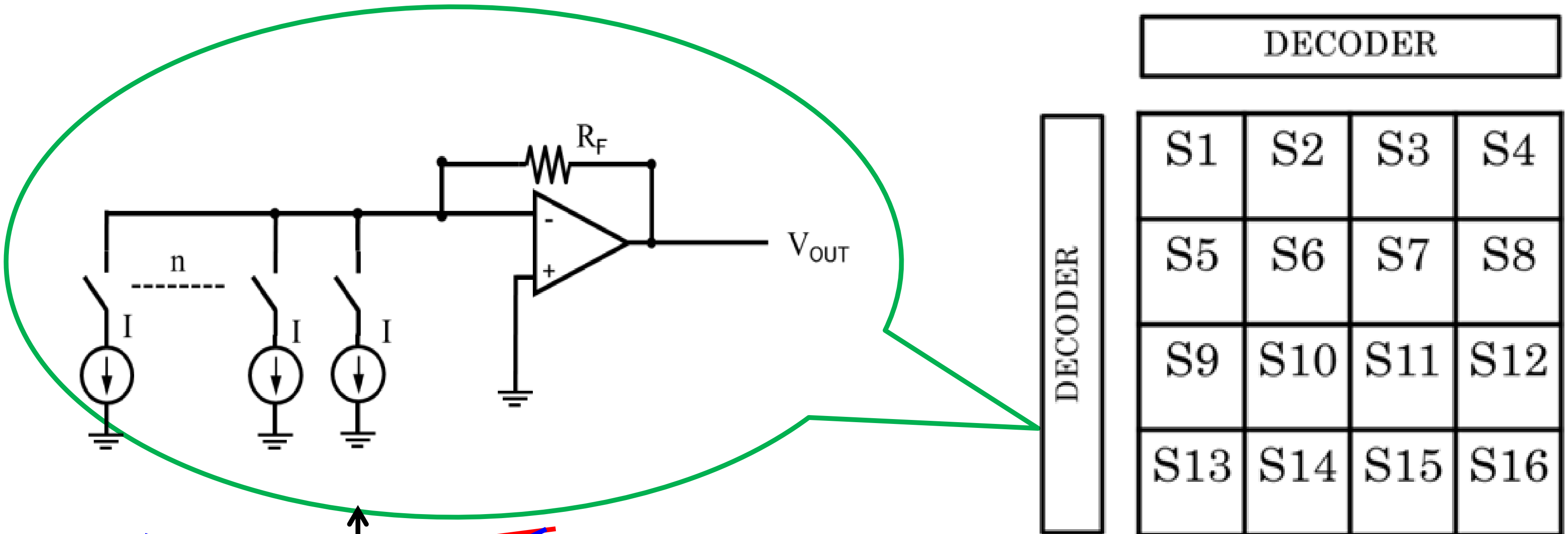


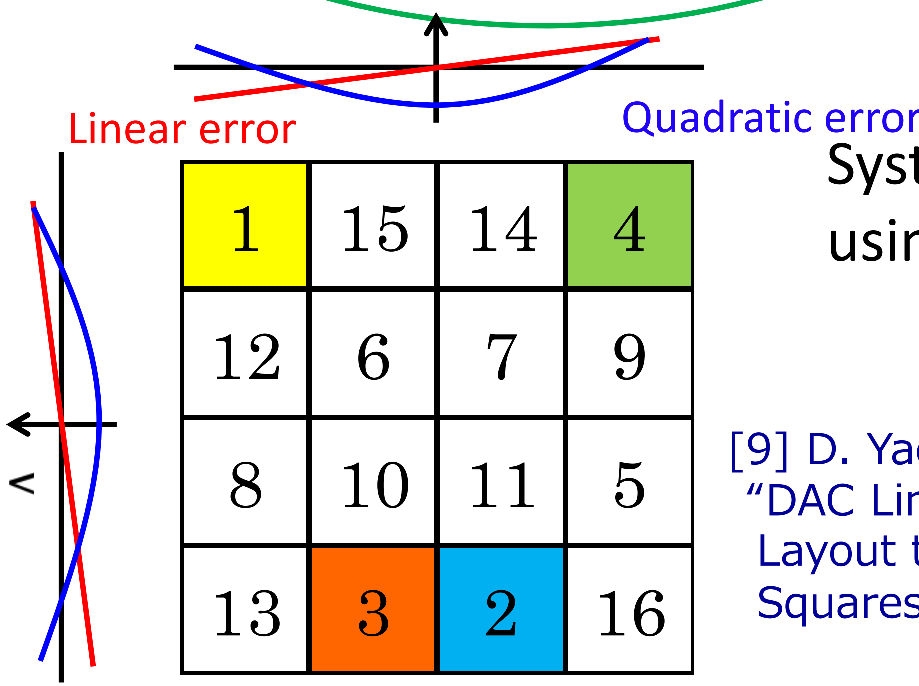
Based on extensive simulation
by my student (Mr. Yuto Sasaki)

The most efficient waveform acquisition can be achieved

Contents

Unary DAC Unit Cell Layout





Systematic mismatch cancellation using magic and Latin squares

[9] D. Yao, Y. Sun, M. Higashino, H. Kobayashi "DAC Linearity Improvement with Layout technique using Magic and Latin Squares", IEEE ISPACS, Xiamen (Nov. 2017)

A Lot of Frontiers

For obtaining prime numbers
素数

Sieve of Eratosthenes

	2	3	4	5	6	7	8	9	10
11	12	13	14	15	16	17	18	19	20
21	22	23	24	25	26	27	28	29	30
31	32	33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48	49	50
51	52	53	54	55	56	57	58	59	60
61	62	63	64	65	66	67	68	69	70
71	72	73	74	75	76	77	78	79	80
81	82	83	84	85	86	87	88	89	90
91	92	93	94	95	96	97	98	99	100
101	102	103	104	105	106	107	108	109	110
111	112	113	114	115	116	117	118	119	120

Primzahlen:

- Applications
  - Gears
  - ADC testing
  - Residue number TDC
  - Residue number sampling system

Under investigation in our lab

Contents

- Statement of This Paper
- SAR ADC Design with Golden Ratio Weight
- SAR ADC Design with Silver Ratio Weight
- DAC with Golden Ratio Weight
- Fibonacci Sequence Weighted SAR ADC as Golden Section Search
- Golden Ratio Sampling
- Other Examples
- Conclusion

Conclusion

- Traditionally, people believe that analog / mixed-signal circuit design is art and craft.

- Here we show that mathematics, especially number theory can contribute to the design as science.

↓

Both art and science are used for good analog / mixed-signal circuit design