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- 2010 年　マレーシア　クアラルンプール

IEEE Asia Pacific Conference on Circuits and Systems,

Kuala Lumpur, Malaysia (Dec. 2010).

[1] Takuya Yagi, Kunihiko Usui, Tatsuji Matsuura, Satoshi Uemori, Yohei Tan, Satoshi Ito, Haruo Kobayashi, "Background Calibration Algorithm for Pipelined ADC with Open-Loop Residue Amplifier using Split ADC Structure,"

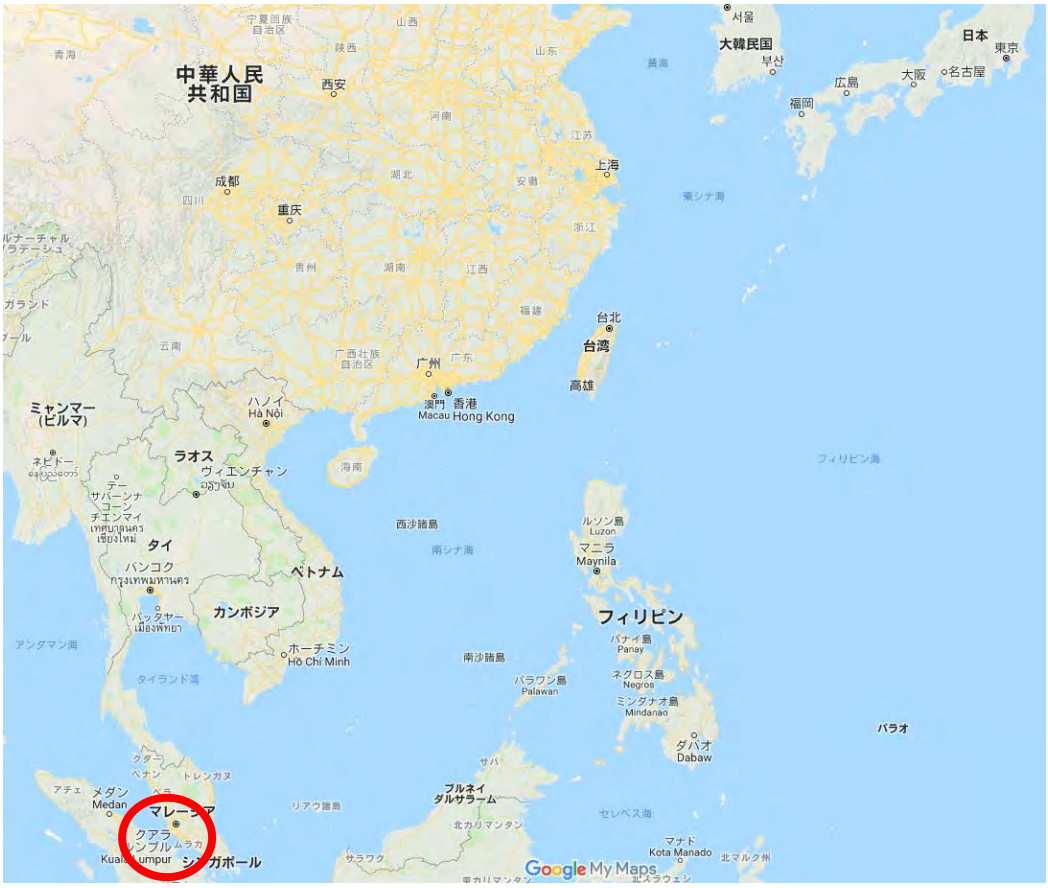
[2] Tomohiko Ogawa, Haruo Kobayashi, et. al., "Non-binary SAR ADC with Digital Error Correction for Low Power Applications,"

[3] Satoshi Ito, et. al., "Stochastic TDC Architecture with Self-Calibration,"

[4] Tomohiko Ogawa, Haruo Kobayashi, Youhei Tan, et. al., "SAR ADC That is Configurable to Optimize Yield,"

[5] Satoshi Uemori, et. al. "ADC Linearity Test Signal Generation Algorithm,"

[6] Kenji Takahashi, et. al. "Single Inductor DC-DC Converter with Bipolar Outputs using Charge Pump,"



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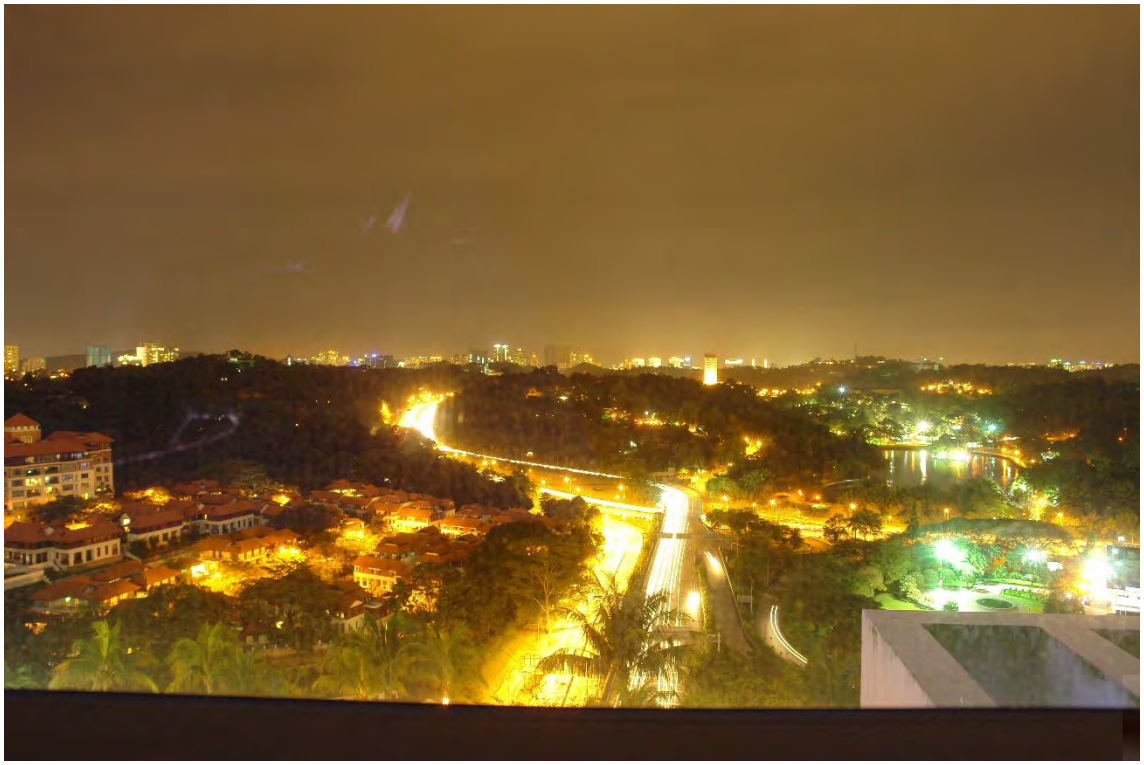

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● 2008 年 12 月　中国　澳門（まかお）

IEEE Asia Pacific Conference on Circuits and Systems, Macao, China, Dec. 2008.

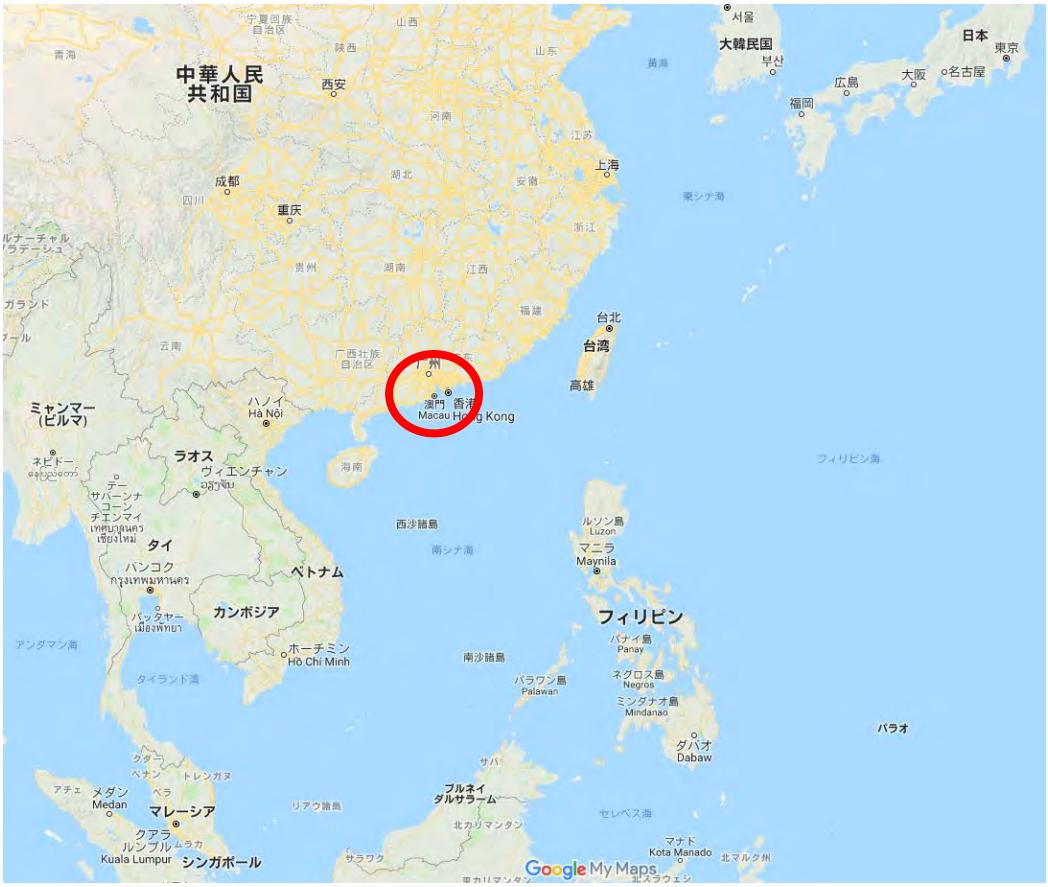
[1] Tomohiko Ogawa, et. al.,
"SAR ADC Algorithm with Redundancy", IEEE Xplore

[2] Akihiro KANB, et. al.,
"New Architecture of Envelope Tracking Power Amplifier for Base Station" IEEE Xplore

[3] Ibuki MORI, et. al.,
"High-Resolution DPWM Generator for Digitally Controlled DC-DC Converters",
IEEE Xplore

[4] Hajime Konagaya, et. al.,
"Delta-Sigma AD Modulator for Low Power Application", IEEE Xplore

[5] Santhos Ario Wibowo, et. al.,
"Analysis of Coupled Inductors for Low-Ripple Fast- Response Buck Converter",
IEEE Xplore



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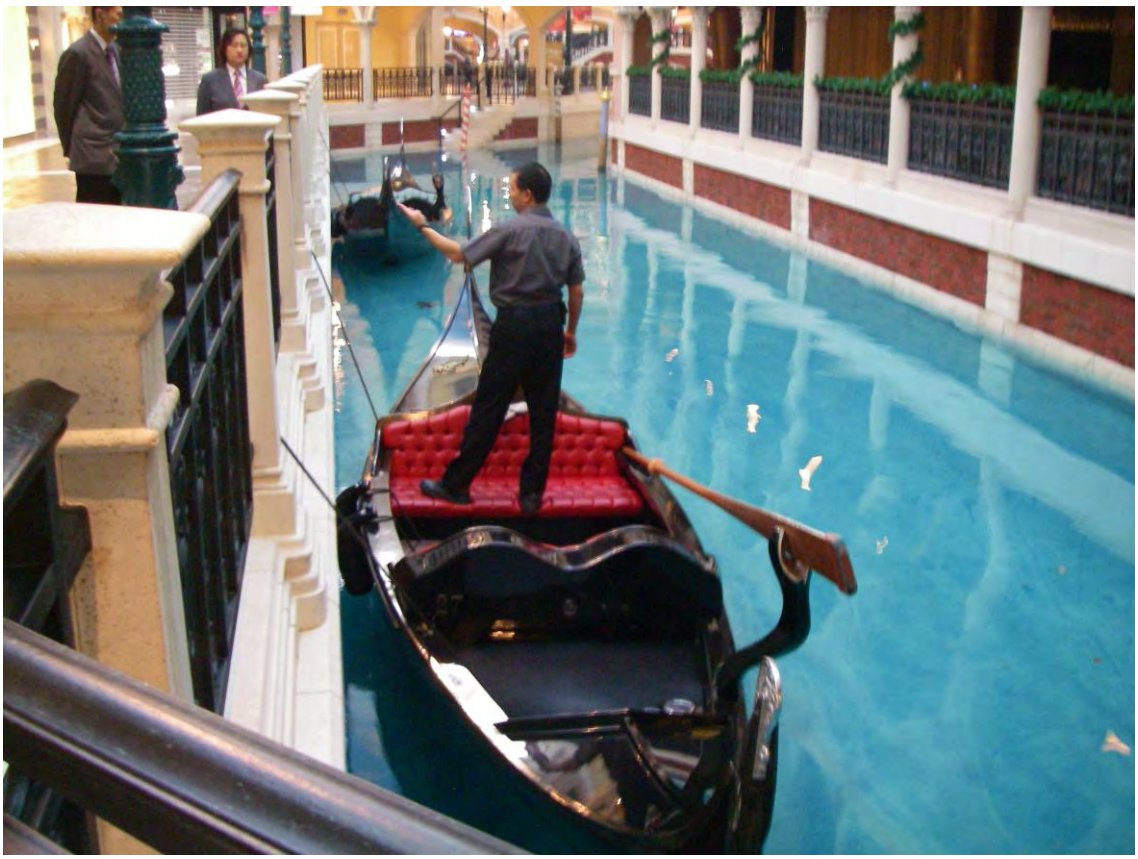

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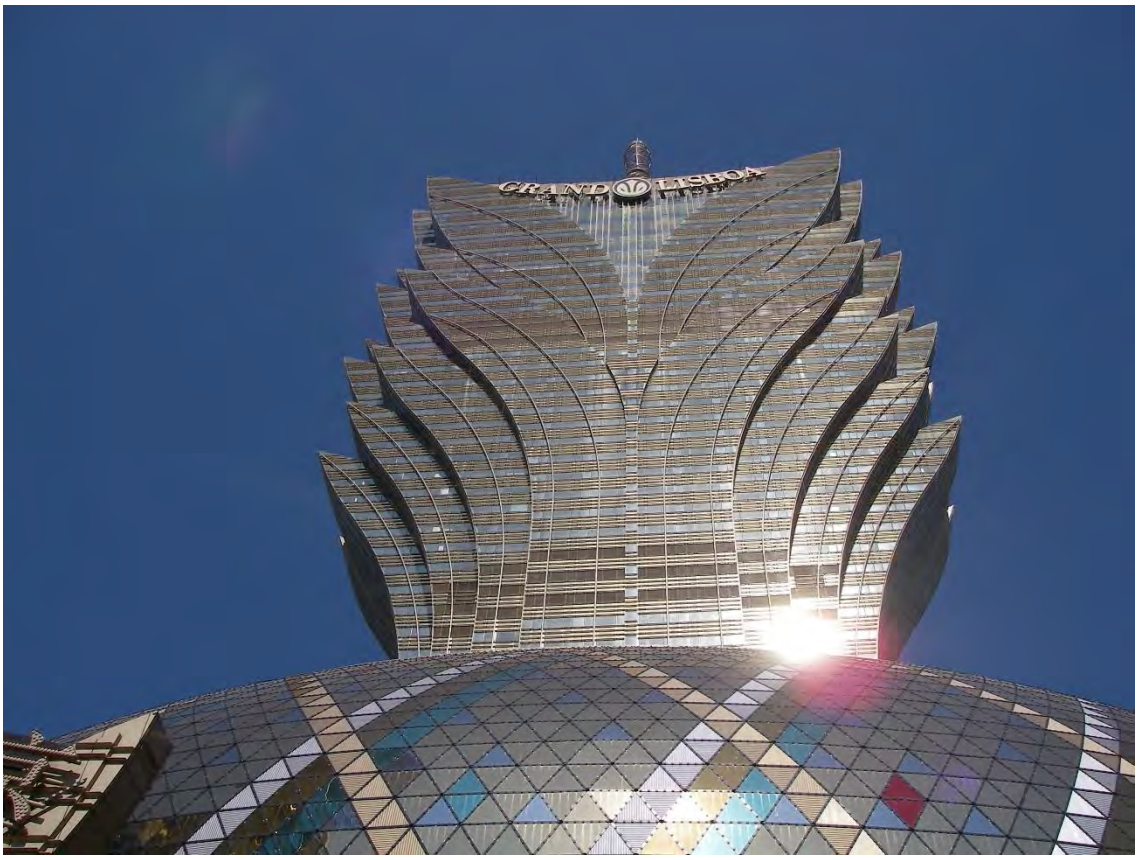

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● 2013 年 11 月　ベトナム　ホーチミン市

4th IEICE International Conference on Integrated Circuits Design and Verification,
Ho Chi Minh City, Vietnam (Nov. 15-16, 2013).

[1] Shu Wu, et. al.,　"Design of a Simple Feed-Forward Controller for DC-DC Buck Converter,"

[2] Zachary Nosker, et. al. "A Single Supply Bootsrapped Boost Regulator for Energy Harvesting Applications"

[3] Yukiko Arai, et. al., "Noise-Shaping Cyclic ADC Architecture"

[4] Satoru Kawauchi, et. al., "A Power-Efficient Noise Canceling Technique Using Signal-Suppression Feed-forward for Wideband LNAs"

[5] Yusuke Osawa, et. al., "Phase Noise Measurement and Testing with Delta-Sigma TDC"

[6] M. Murakami, et. al., "Study of Complex Multi-Bandpass ΔΣ Modulator for I-Q Signal Generation"

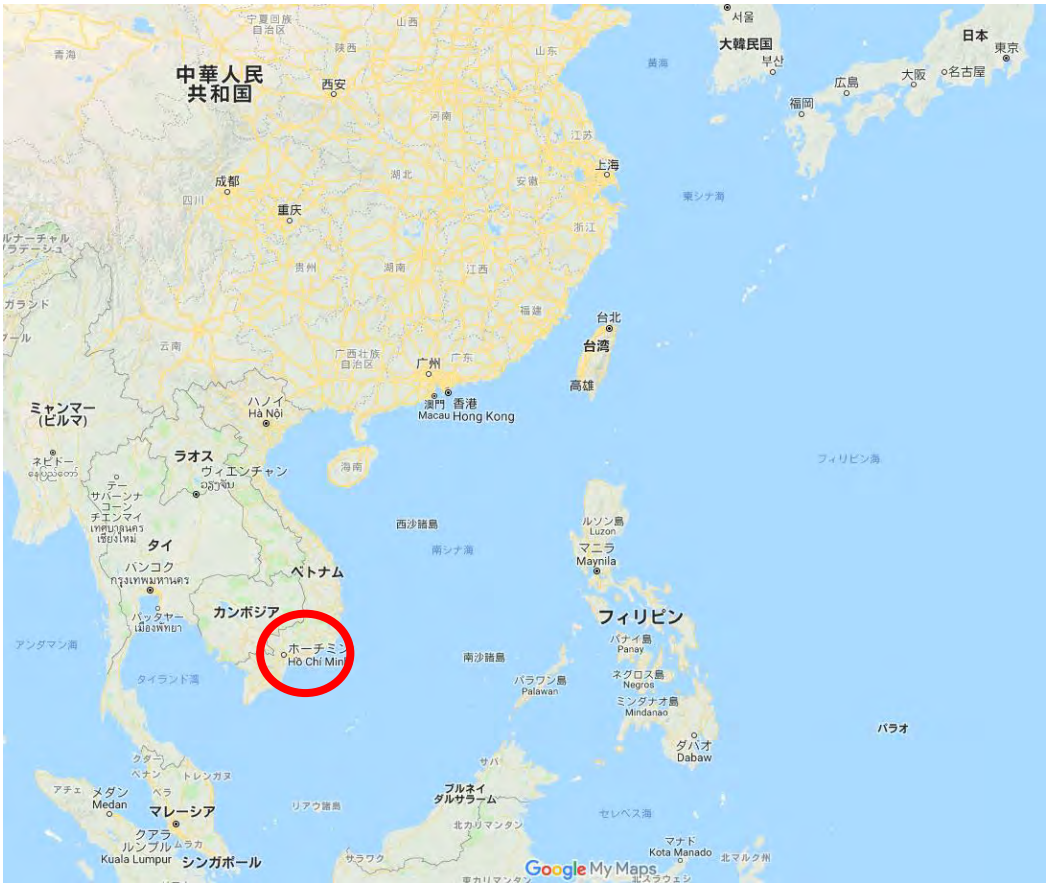
[7] Takayuki Negishi, et. al., "Automatic Synthesis of Comparator Circuit Using Genetic Algorithm"

[8] Ramin Khatami, et. al., "Delta-Sigma Digital-to-Time Converter and its Application to SSCG"

[9] S. Tanaka, et. al., "Single Inductor Multi Output DC-DC Converter Design with Hysteresis Control"

[10] Shaiful Nizam MOHYAR, et. al.,"SFDR Improvement Algorithms for Current-Steering DACs"

[11] Hitoshi Aoki, Haruo Kobayashi, "Typical n-MOSFET Modeling using A Skewing Method"



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● 2006 年 11 月　中国　杭州

[1] H. San,et. al., “A Multibit Complex Bandpass Delta Sigma AD Modulator with I, Q Dynamic Matching and DWA Algorithm”

IEEE Asian Solid-State Circuits Conference, Hangzhou, China (Nov. 2006)

[2] M. Hotta, et. al., “SAR ADC Architecture with Digital Error Correction",

IEEJ International Analog VLSI Workshop, Hangzhou, China (Nov.2006).

[3] Y. Kobori, et. al.,

“A New Control Method for Buck-Boost DC-DC Converters Using PWM and Delta-Sigma Modulation for Mobile Equipment,"

IEEJ International Analog VLSI Workshop, Hangzhou, China (Nov. 2006).

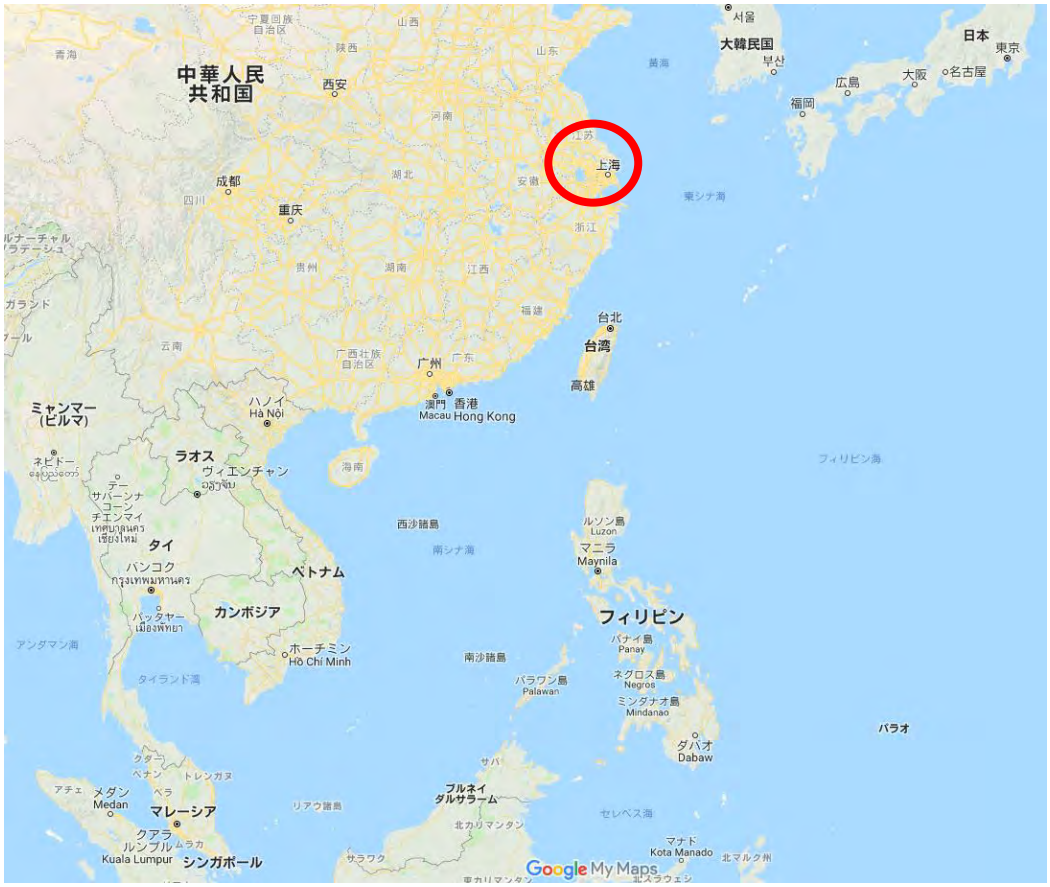
[4] M. Kono, et. al., “A High-Precision AC Wheatstone Bridge Strain Gauge",

IEEJ International Analog VLSI Workshop, Hangzhou, China (Nov. 2006).

[5] H. San, et. al.,

“DWA Algorithms for Multibit Complex Bandpass ΔΣAD Modulators of Arbitrary Signal Band,",

IEEJ International Analog VLSI Workshop, Hangzhou, China (Nov.2006).



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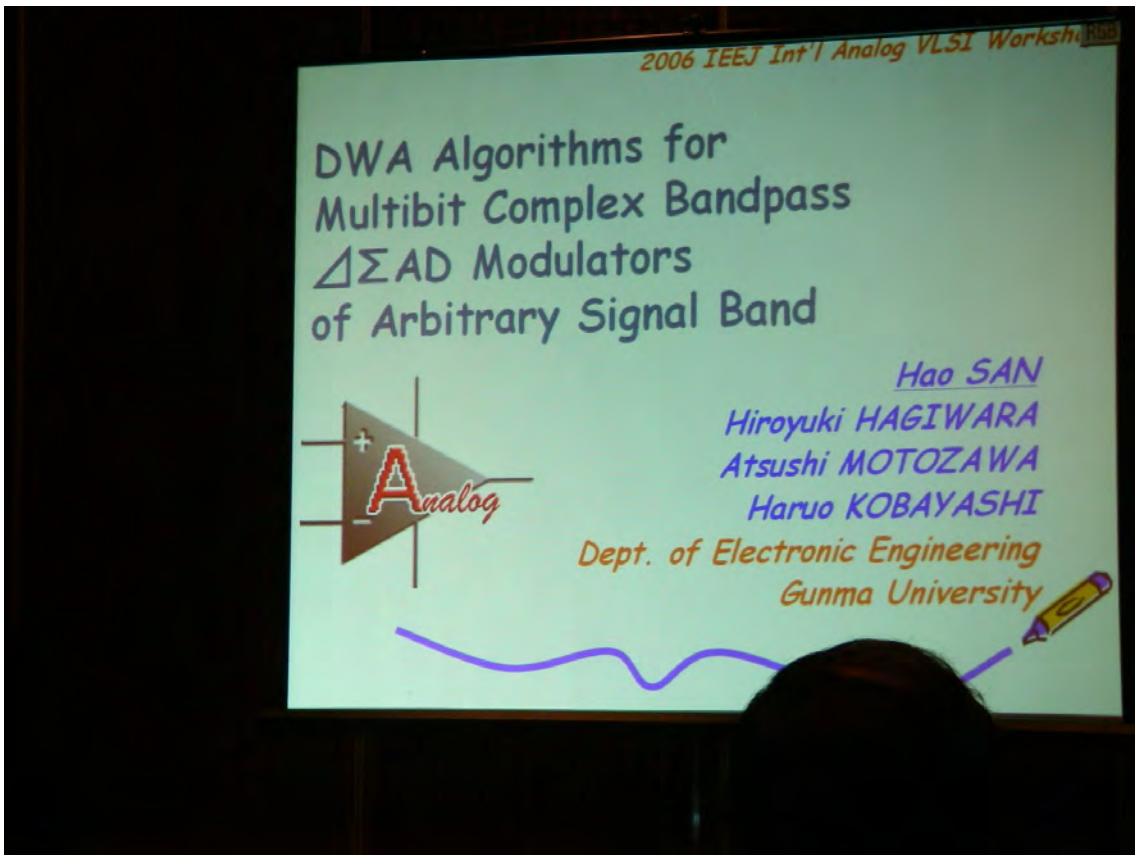

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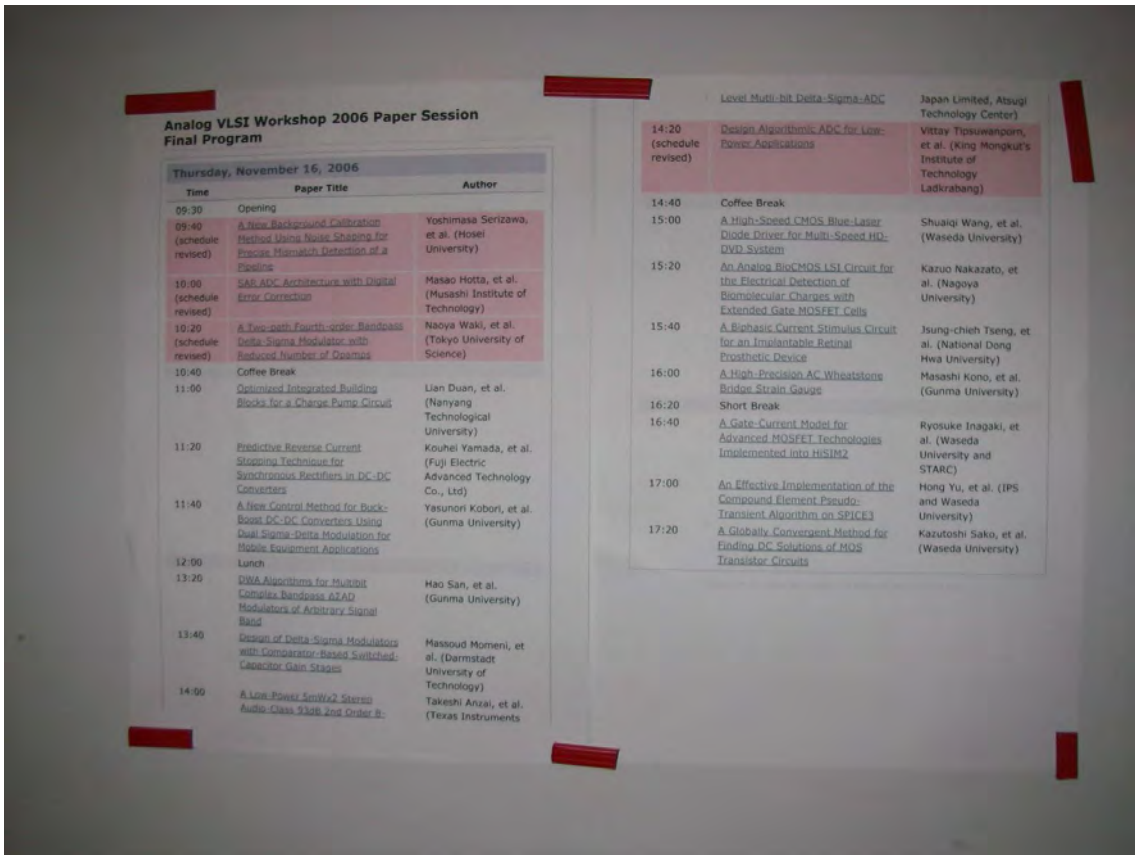

Analog VLSI Workshop 2006 Paper Session
Final Program

Thursday, November 16, 2006

Time	Paper Title	Author
09:30	Opening	
09:40 (schedule revised)	A New Background Calibration Method Using Noise Shaping for Precise Mismatch Detection of a Pipeline	Yoshimasa Serizawa, et al. (Hosei University)
10:00 (schedule revised)	SAR ADC Architecture with Digital Error Correction	Masao Hotta, et al. (Musashi Institute of Technology)
10:20 (schedule revised)	A Two-path Fourth-order Bandpass Delta-Sigma Modulator with Reduced Number of Opamps	Naoya Waki, et al. (Tokyo University of Science)
10:40	Coffee Break	
11:00	Optimized Integrated Building Blocks for a Charge Pump Circuit	Lian Duan, et al. (Nanyang Technological University)
11:20	Predictive Reverse Current Stopping Technique for Synchronous Rectifiers in DC-DC Converters	Kouhei Yamada, et al. (Fuji Electric Advanced Technology Co., Ltd)
11:40	A New Control Method for Buck-Boost DC-DC Converters Using Dual Sigma-Delta Modulation for Mobile Equipment Applications	Yasunori Kobori, et al. (Gunma University)
12:00	Lunch	
13:20	DWA Algorithms for Multibit Complex Bandpass AZAD Modulators of Arbitrary Signal Band	Hao San, et al. (Gunma University)
13:40	Design of Delta-Sigma Modulators with Comparator-Based Switched-Capacitor Gain Stages	Massoud Momeni, et al. (Darmstadt University of Technology)
14:00	A Low-Power 5mW×2 Stereo Audio Class 93dB 2nd Order ΔΣ-	Takeshi Anzai, et al. (Texas Instruments
	Level Multi-bit Delta-Sigma-ADC	Japan Limited, Atsugi Technology Center)
14:20 (schedule revised)	Design Algorithmic ADC for Low-Power Applications	Vittay Tipsuwanporn, et al. (King Mongkut's Institute of Technology Ladkrabang)
14:40	Coffee Break	
15:00	A High-Speed CMOS Blue-Laser Diode Driver for Multi-Speed HD-DVD System	Shuaiqi Wang, et al. (Waseda University)
15:20	An Analog BioCMOS LSI Circuit for the Electrical Detection of Biomolecular Charges with Extended Gate MOSFET Cells	Kazuo Nakazato, et al. (Nagoya University)
15:40	A Biphasic Current Stimulus Circuit for an Implantable Retinal Prosthetic Device	Jsung-chieh Tseng, et al. (National Dong Hwa University)
16:00	A High-Precision AC Wheatstone Bridge Strain Gauge	Masashi Kono, et al. (Gunma University)
16:20	Short Break	
16:40	A Gate-Current Model for Advanced MOSFET Technologies Implemented into HiSIM2	Ryosuke Inagaki, et al. (Waseda University and STARC)
17:00	An Effective Implementation of the Compound Element Pseudo-Transient Algorithm on SPICE3	Hong Yu, et al. (IPS and Waseda University)
17:20	A Globally Convergent Method for Finding DC Solutions of MOS Transistor Circuits	Kazutoshi Sako, et al. (Waseda University)

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- 2012 年 12 月　台湾　高雄

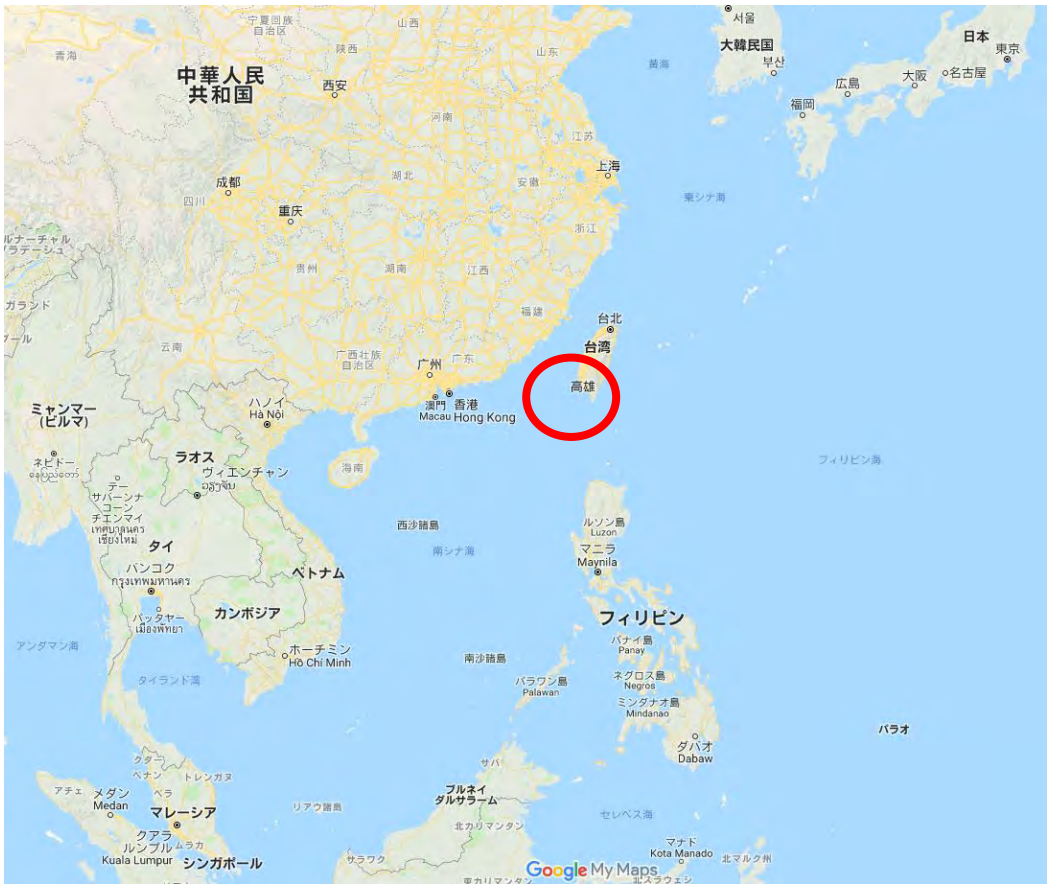
IEEE Asia Pacific Conference on Circuits and Systems, Kaohsiung, Taiwan (Dec. 2012).

[1] Guanglei Jin, et. al., "Digitally-Contolled Gm-C Bandpass Filter"

[2] Satoshi Uemori, Masamichi Ishii, Haruo Kobayashi, Yuta Doi, Osamu Kobayashi, Tatsuji Matsuura, Kiichi Niitsu,Yuta Arakawa, et. al.,
"Multi-bit Sigma-Delta TDC Architecture with Self-Calibration",

[3] Yasunori Kobori, Qiulin Zhu, Murong Li,et. al.,
"Single Inductor Dual Output DC-DC Converter Design with Exclusive Control",

[4] Hong Gao, Lin Xing, Yasunori Kobori, Zhao Feng, et. al.,
"DC-DC Converter with Continuous-Time Feed-Forward Sigma-Delta Modulator Control"



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● 2011 年 11 月　韓国　済州島

[7] Kiichi Niitsu,　et. al.,
"An On-Chip Timing Jitter Measurement Circuit Using a Self-Referenced Clock and A Cascaded Time Difference Amplifier with Duty-Cycle Compensation "
IEEE Asian Solid-State Circuits Conference (A-SSCC 2011), Jeju, Korea (Nov. 2011).

[8] Masato Sakurai, Kiichi Niitsu, et. al.,
"Analysis of Jitter Accumulation in Interleaved Phase Frequency Detectors for High-Accuracy On-Chip Jitter Measurements," International SoC Design Conference（Nov. 2011).

[9]　Masato Sakurai, Kiichi Niitsu, et. al.,
"A Reference-Clock-Free On-Chip Timing Jitter Measurement Circuit Using a Cascaded Time Difference Amplifier with Duty-Cycle Compensation in 65nm CMOS,"
International SoC Design Conference, Chip Design Contest, Jeju Korea (Nov. 2011)

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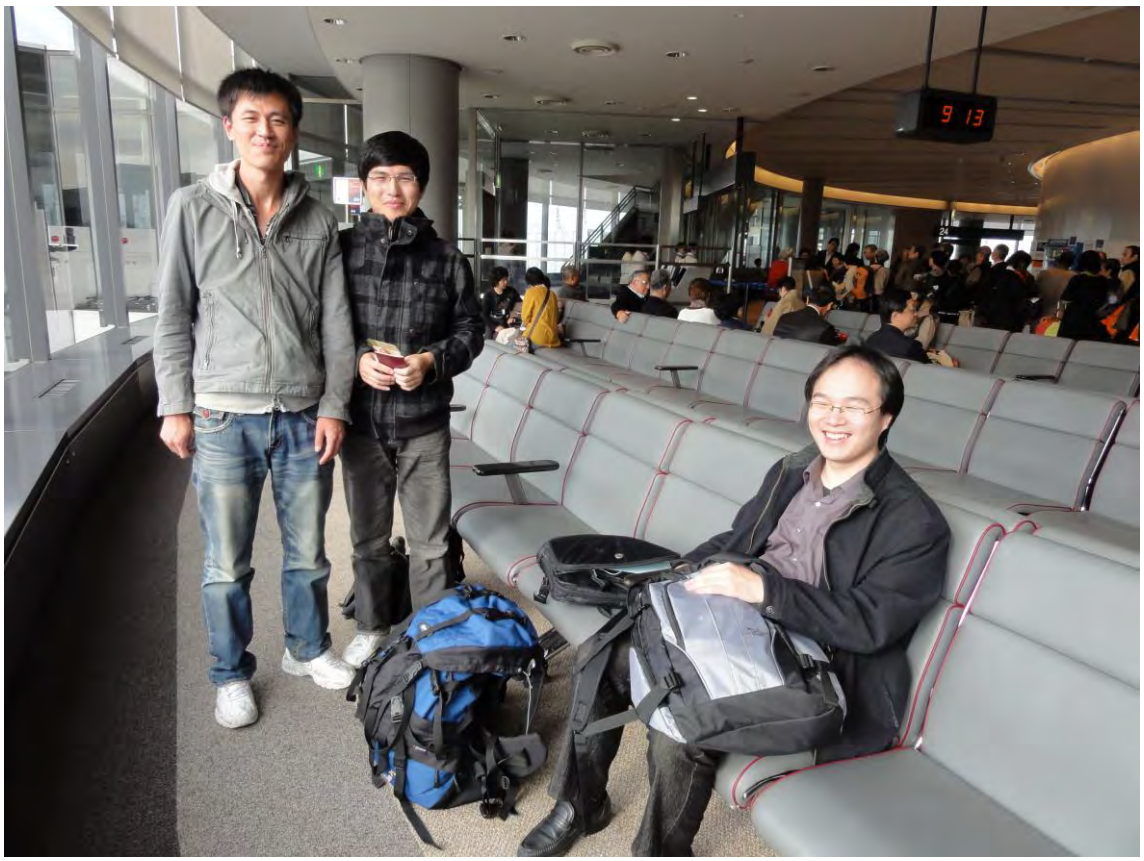

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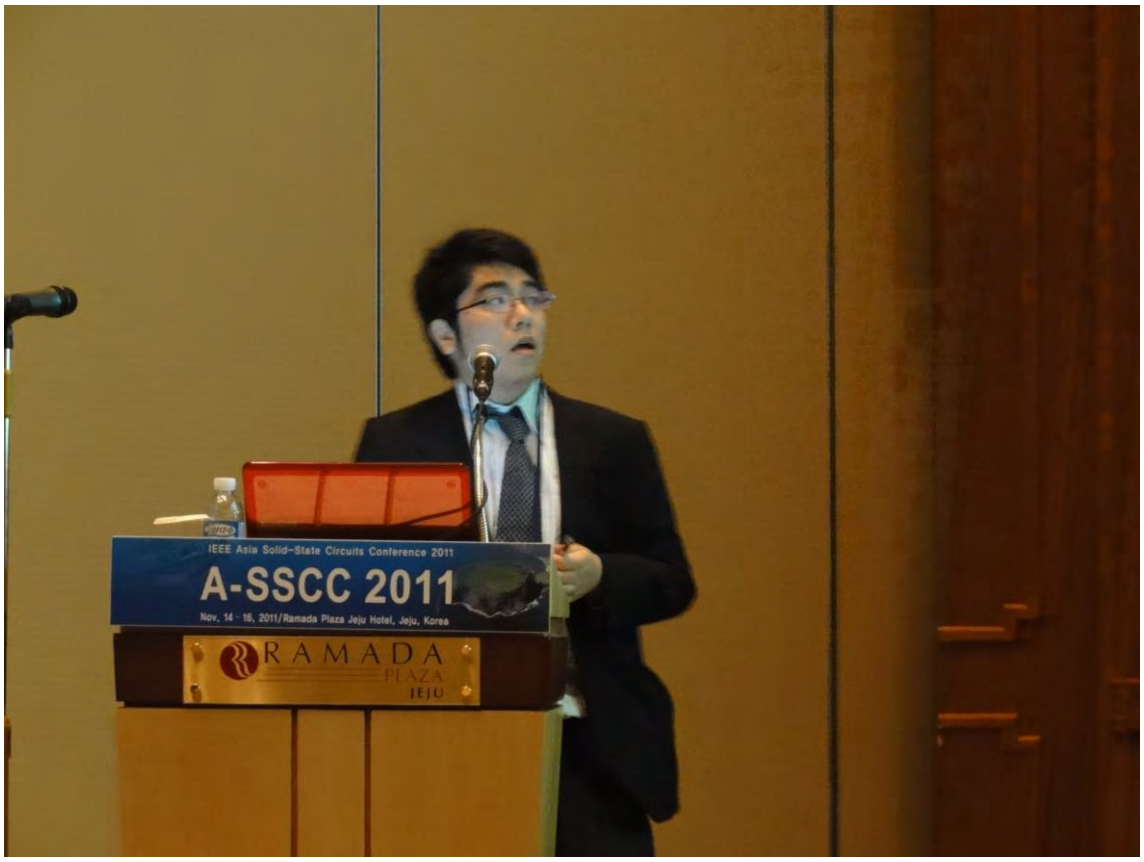

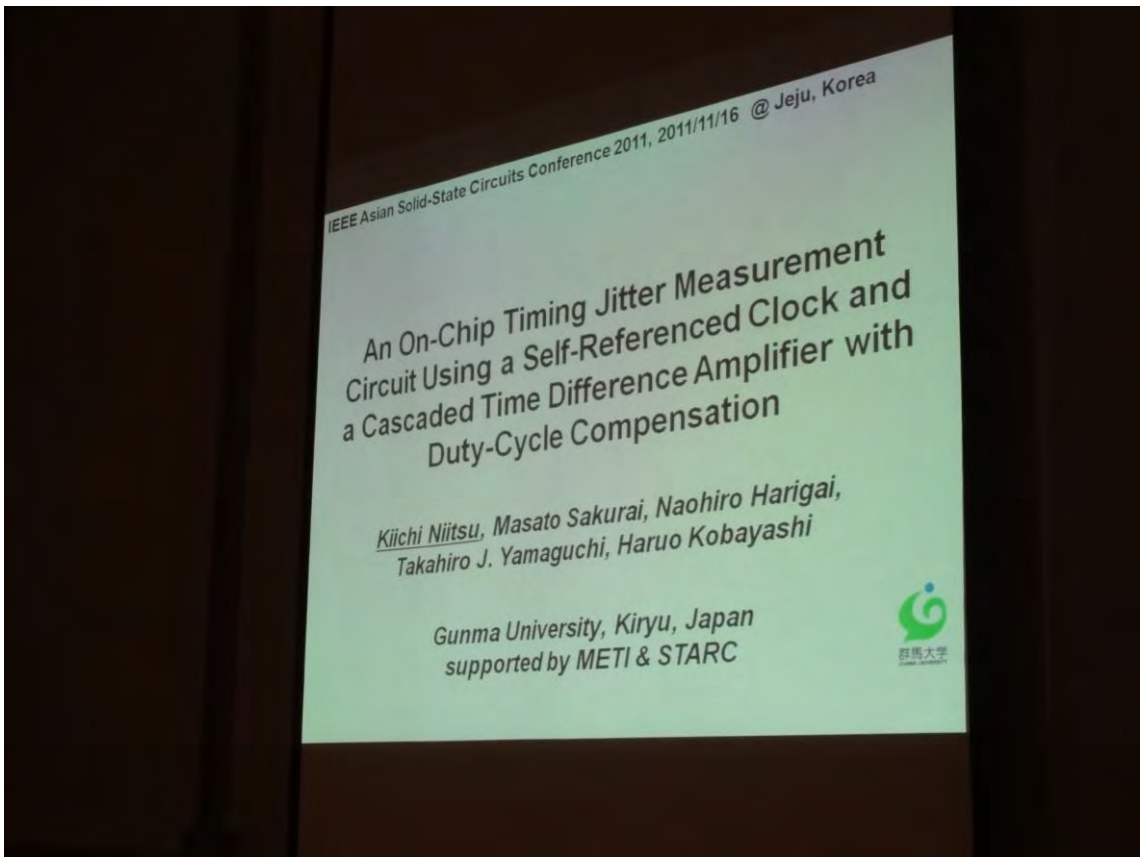

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Photos by Nobuyoshi Ishikawa, Gunma University