Research on a successive approximation register TDC architecture for one shot timing measurement

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Research target

High-speed I/O interface signal timing testing

- Small circuit
- Full digital
- High linearity
- High resolution

Enable to test at low cost

SAR TDC

SAR: Successive Approximation Register
TDC: Time to Digital Converter
Application

Multi channels

Large circuit $\times$ Large amounts
High test cost

Small circuit $\times$ Large amounts
Low test cost

ATE : Automated Test Equipment
Innovation

✓ **Ring Oscillator**

One-shot timing measurement &
Good for high & low frequency repetitive timing
Outline

- Research Objective
- TDC Application to LSI Testing Technology
- SAR TDC Architecture & Operation
- SAR TDC Employing Ring Oscillator
- Summary
Research objective

To develop time-to-digital circuit with small size, low power, fine time resolution & one-shot timing signal measurement capability
Approach

Flash TDC

Huge (Costly) 😞 Circuit Scale

One Shot 😊 Timing Signal

Enable to measure one shot timing with SAR TDC

SAR TDC

Small 😊

Repetitive 😞

One Shot 😊
Problem of SAR-TDC & remedy

Usual

- Voltage can be held
- Time difference cannot be held

Suggestion

- Time difference can be held!
Suggestion

SAR TDC + Ring Oscillator

- Measure one-shot timing
- Full digital circuit

Full digital FPGA implementation
Outline

● Research Objective
● TDC Application to LSI Testing Technology
● SAR TDC Architecture & Operation
● SAR TDC Employing Ring Oscillator (Digital)
● Summary
“Timing” is very important in ATE systems.

Many high-performance TDCs are used there.

Such as for clock timing, jitter measurements.

Analog/mixed-signal BIST, BOST

- TDC can be used for BIST, BOST
- BIST, DFT
  - Chip design time become longer
  - Chip become larger
  - Difficult to assure its reliability
  - Long time to market
  - Costly
  - Should be simple
- BOST
  - Design / implementation after tape out attractive

BIST : Built In Self Test
BOST : Built Out Self Test
Outline

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- Summary
D-FFs can be greatly reduced by using MUX

Circuit operation loop can be made with successive approximation

SAR : Successive Approximation Register
SAR-ADC Vs. SAR-TDC

SAR ADC:
- Comparator
- DAC

SAR TDC:
- D-FF
- Delay line, MUX
SAR TDC operation

STEP1

\[ \Delta T = 4.3 \tau \]

Example

\[ \Delta T = 4.3 \tau \]
SAR TDC operation

STEP2

Example

$\Delta T = 4.3 \tau$

CLK1

CLK2

STEP2

$\Delta T = 4.3 \tau$

6$\tau$

MUX

SAR Logic

select 110

3

0

DQ

$D_{out}$

18
SAR TDC operation

STEP 3

Example

\[ \Delta T = 4.3 \tau \]
SAR TDC operation

STEP4 (Stable)

Example

$\Delta T = 4.3 \tau$

Digital output: 4
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SAR-TDC employing 2-ring oscillators
Ring oscillator timing chart

$$T_{RO} = 2(n\tau + \tau_i)$$

$$0 < \Delta T < \frac{T_{RO}}{2}$$
Low frequency clock measurement

Low frequency

High frequency (Ring Oscillator)

Short testing time for low frequency repetitive timing
Simulated circuit

Software: spice
Resolution: 3bit
Full scale: 0 – 8.0ns
One shot input timing signal

$\Delta T = 5.2\text{ns}$
Simulated ring oscillator waveforms

\[ \Delta T = 5.2\text{ns} \]
D-FF output signal at each steps

\[ \Delta T = 5.2\,\text{ns} \]

\[ 5.0\,\text{ns} \leq \Delta T < 6.0\,\text{ns} \]
Input output linearity

SAR TDC employing 2 ring oscillators input & output have linear relationship
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- SAR TDC Employing Ring Oscillator
- Summary
Summary

- One shot timing can be measured with SAR TDC
- Ring oscillator can generate repetitive clock timing
- Full digital implementation employing ring oscillators. Suitable for high & low frequency repetitive clock timing

- Small circuit
- One shot timing
- Full digital
- High linearity
- High resolution

Timing testing at low cost
Future works

- FPGA implementation
- Experiment using signal generator
- Calibrate oscillation frequency mismatch of ring oscillator
Thank you for your attention
Appendix
Q&A(1)

Q1 実際の回路の要求仕様的には満たしているのか

A1 従来のカウンタタイプのTDCは計測対象の時間の間に何回カウンタが回るかという方法で時間を測定していた。このTDCは1クロック未満でも計測出来るのが利点。FPGAのボードの性能やカスタムICの性能にもよるがnsオーダーの時間計測であればカウンタでは数十GHzに相当する時間計測が可能。
Q2 アナログ回路を使わなくても良い利点とは

A2 アナログ回路はキャパシタなどの素子（チップ面積大）を使わなくてはならず、高コスト。またアナログ回路の設計者も限られており、設計の容易化という面でも不利。デジタルであればハードウェア言語でプログラミングすることで自動合成できるので設計容易でアナログ回路と比較するとコストでメリットが大きい。
Q&A(3)

Q3 単発信号のアプリケーションとは

A3 クロックタイミング試験は基本的には繰り返し信号。しかし他のTOFや距離計測、科学実験など、単発信号しか入力出来ないアプリケーションも存在する。そのようなアプリケーションでも使える可能性があるというという期待もある。
Flash TDC vs. SAR TDC

Flash TDC

10-bit : 1023

One Shot

Timing Signal

SAR TDC

# of D-FFs

10-bit : 23

Repetitive
High & low frequency clock measurement

High Frequency

CLK1 (CLK2)
Ready
START (STOP)
Ring Oscillator I (Ring Oscillator II)

2GHz
Ring Oscillator
10ns × 10 = 100ns

Low Frequency

CLK1 (CLK2)
Ready
START (STOP)
Ring Oscillator I (Ring Oscillator II)

0.01Hz
Ring Oscillator
10ns × 10 = 100ns

Short testing time for low frequency repetitive timing