平成30年度　第9回電気学会栃木･群馬支所合同研究発表会　March 4, 2019

Research on a successive approximation register TDC architecture for one shot timing measurement

Division of Electronics and Informatics
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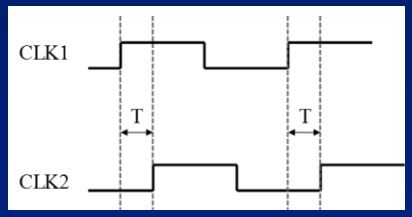
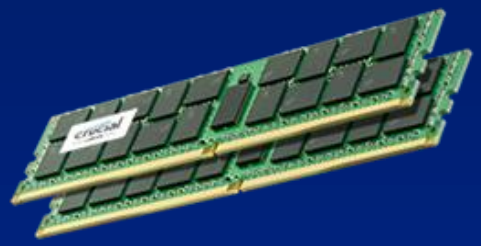
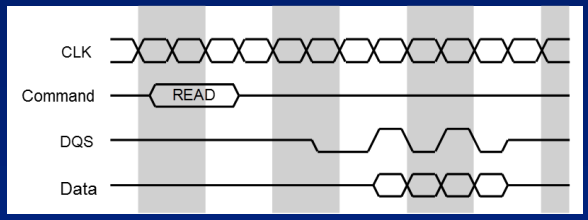
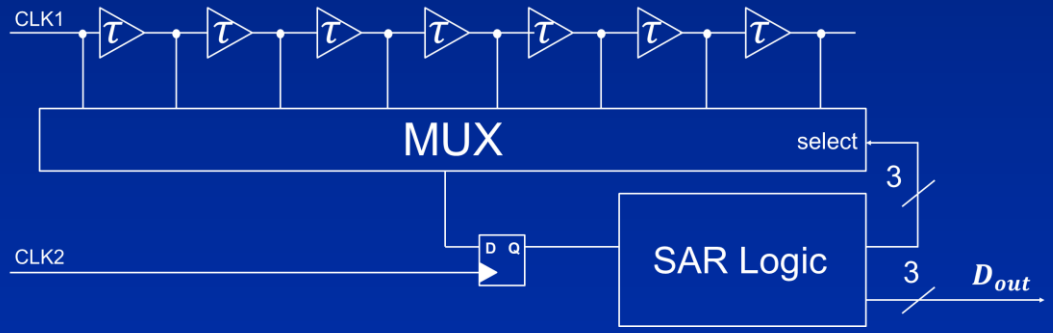
Research target







High-speed I/O interface signal timing testing



SAR TDC

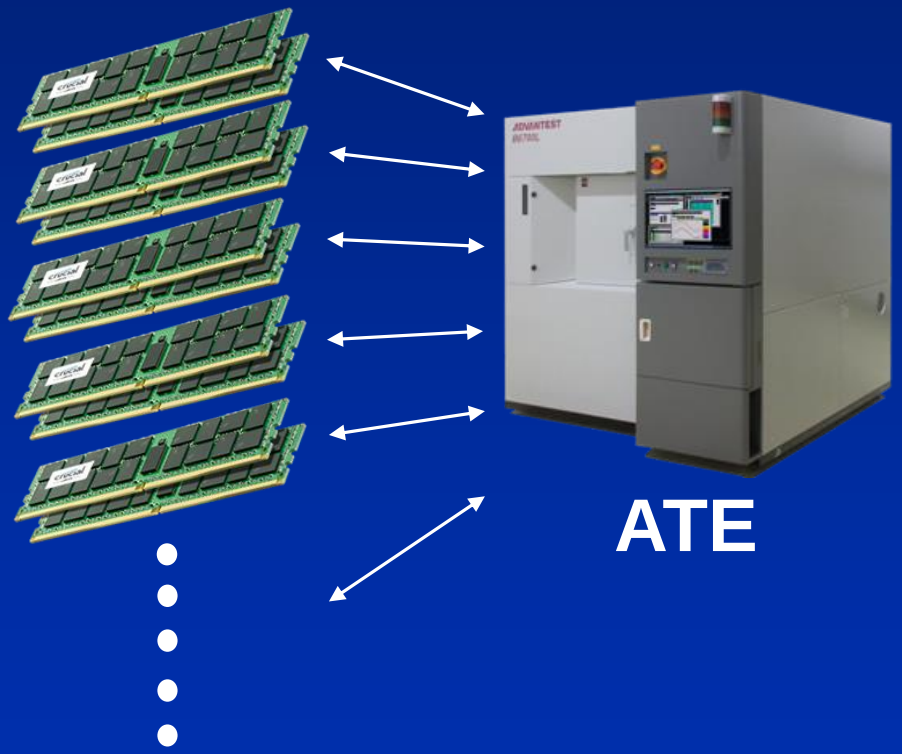
- ✓ **Small circuit**
- ✓ **Full digital**
- ✓ **High linearity**
- ✓ **High resolution**

Enable to test at low cost

SAR : Successive Approximation Register
TDC: Time to Digital Converter

Application

Multi channels



ATE

Large circuit × Large amounts

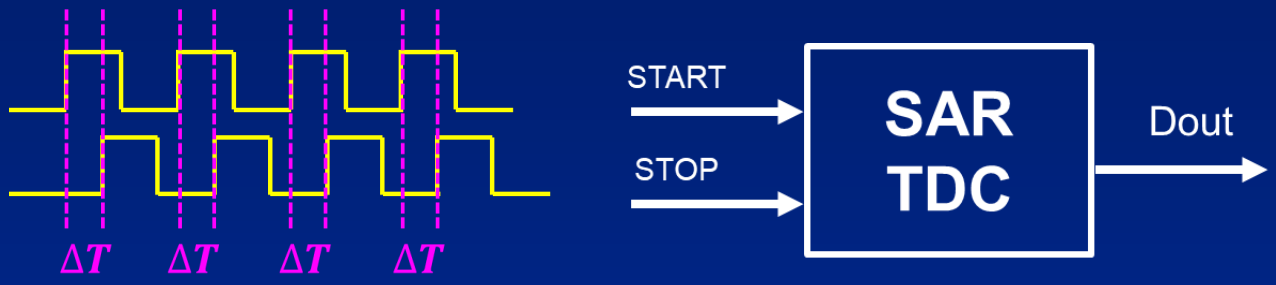
High test cost

Small circuit × Large amounts

Low test cost

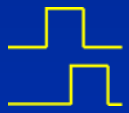
ATE : Automated Test Equipment

Innovation



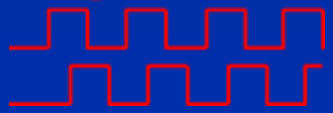
- ✓ **Ring Oscillator**

One-shot timing measurement



&

Good for high & low frequency repetitive timing



Outline

- Research Objective
- TDC Application to LSI Testing Technology
- SAR TDC Architecture & Operation
- SAR TDC Employing Ring Oscillator
- Summary

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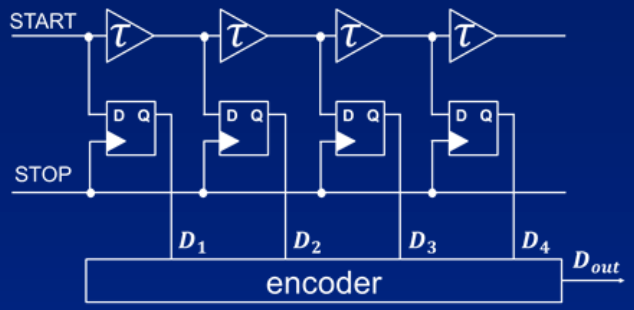
Research objective

To develop time-to-digital circuit with small size,

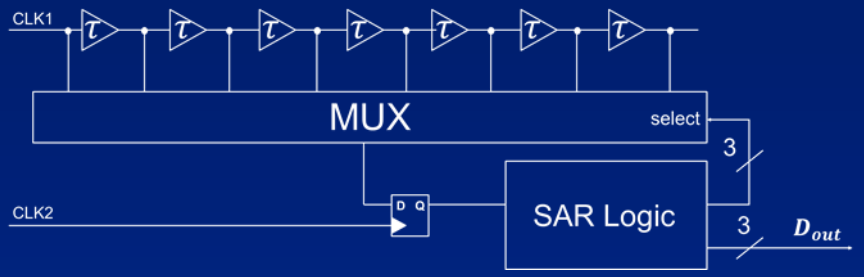
low power, fine time resolution

& one-shot timing signal measurement capability

Approach



Flash TDC



SAR TDC

Huge (Costly)

Circuit Scale

Small

One Shot

Timing Signal

Repetitive

One Shot

Enable to measure one shot timing with SAR TDC

Problem of SAR-TDC & remedy

Usual

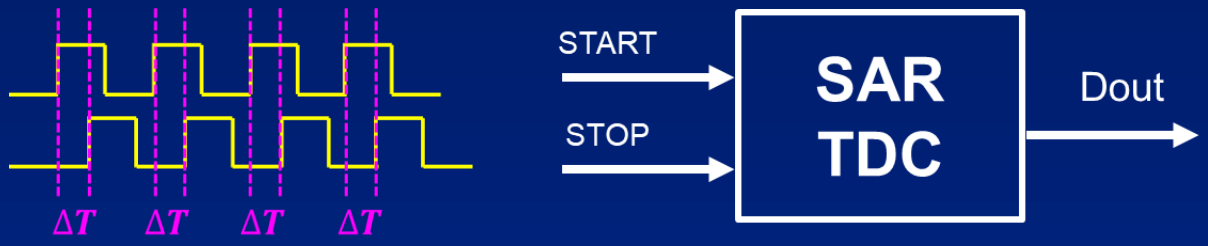
Voltage can be held

Time difference cannot be held

Suggestion

Time difference can be held !

Suggestion



SAR TDC + Ring Oscillator

- Measure one-shot timing
- Full digital circuit

Full digital FPGA implementation

Outline

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- SAR TDC Employing Ring Oscillator (Digital)
- Summary

ATE system & TDC

- **“Timing” is very important in ATE systems**
- **Many high-performance TDCs are used there.**

Such as

for clock timing, jitter measurements

[1] K. Yamamoto,at. el. (Advantest Corp.), “Multi Strobe Circuit for 2.133 GHz Memory Test System,” IEEE International Test Conference, Paper 6.1 (2006).

Analog/mixed-signal BIST, BOST

- **TDC can be used for BIST, BOST**
- **BIST, DFT**

Chip design time become longer — **Long time to market**

Chip become larger — **Costly**

Difficult to assure its reliability — **Should be simple**

- **BOST**

Design / implementation after tape out attractive

BIST : Built In Self Test

BOST : Built Out Self Test

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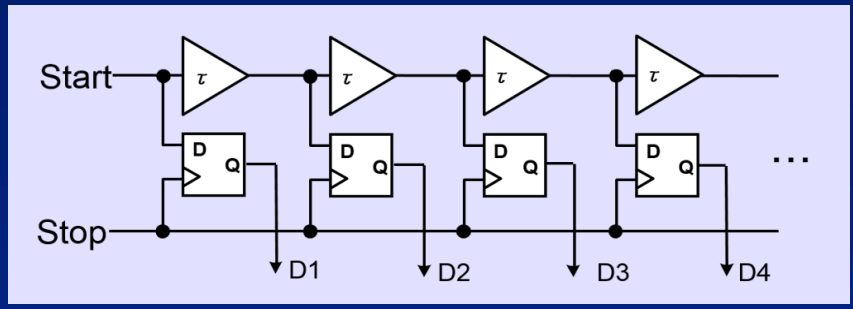
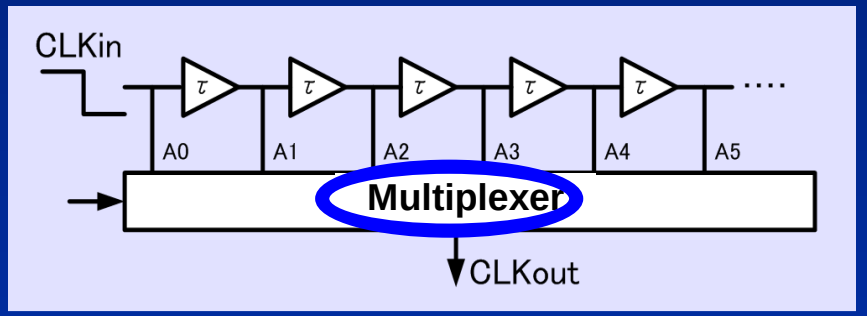
SAR TDC architecture

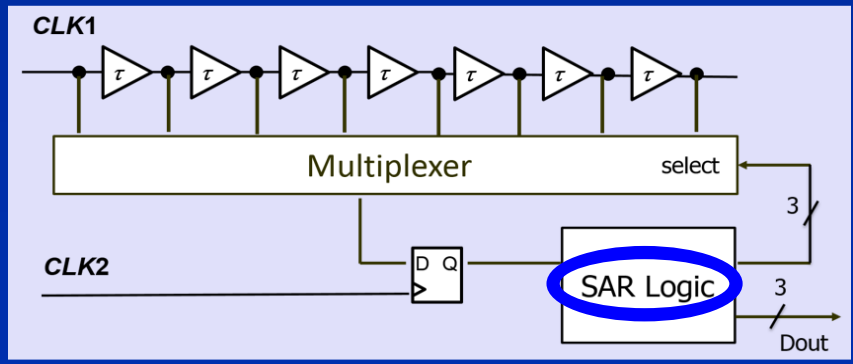
D-FFs can be greatly reduced by using MUX

Circuit operation loop can be made with successive approximation



Flash TDC





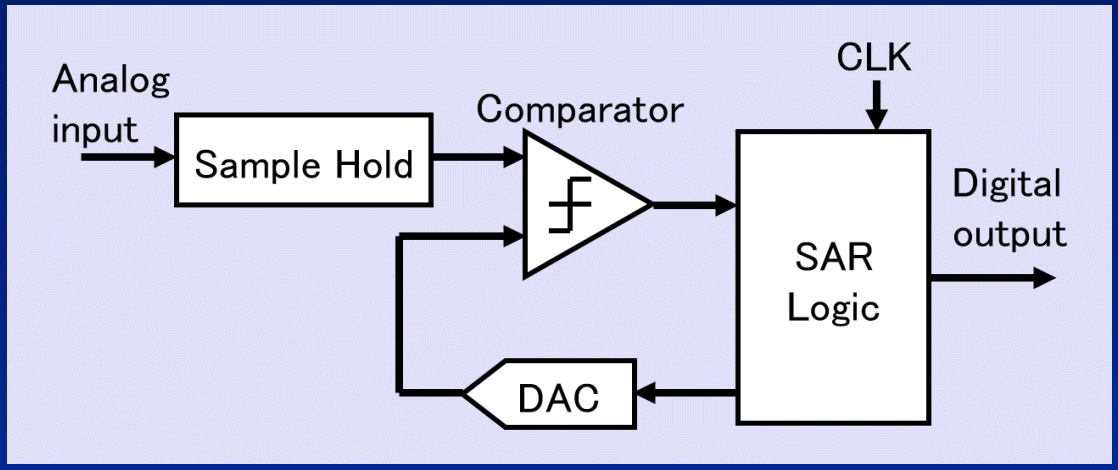
SAR TDC

SAR : Successive Approximation Register

SAR-ADC Vs. SAR-TDC

SAR ADC :

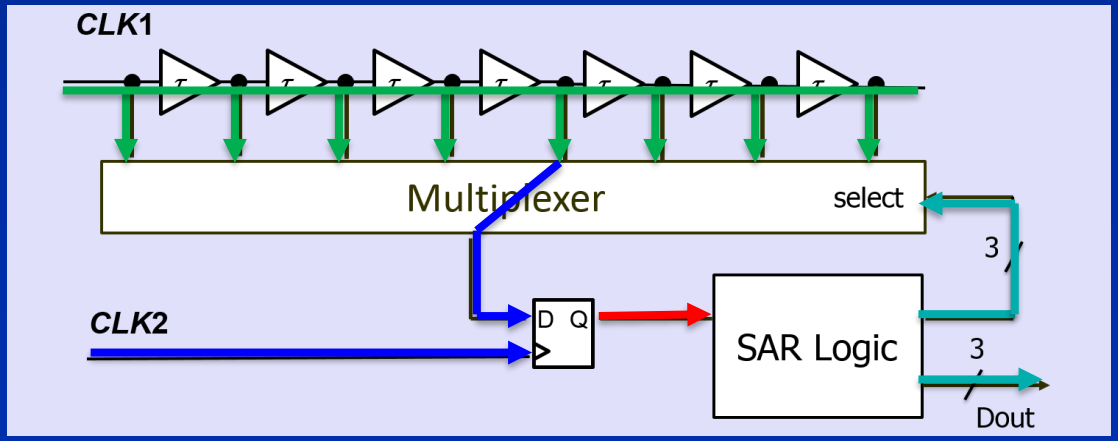
- **Comparator**
- **DAC**



SAR-ADC

SAR TDC :

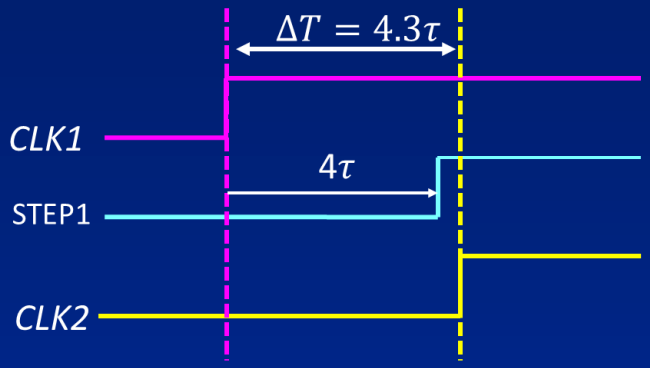
- **D-FF**
- **Delay line,MUX**

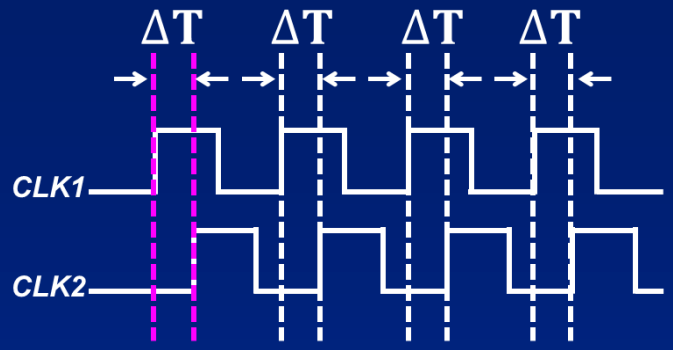


SAR-TDC

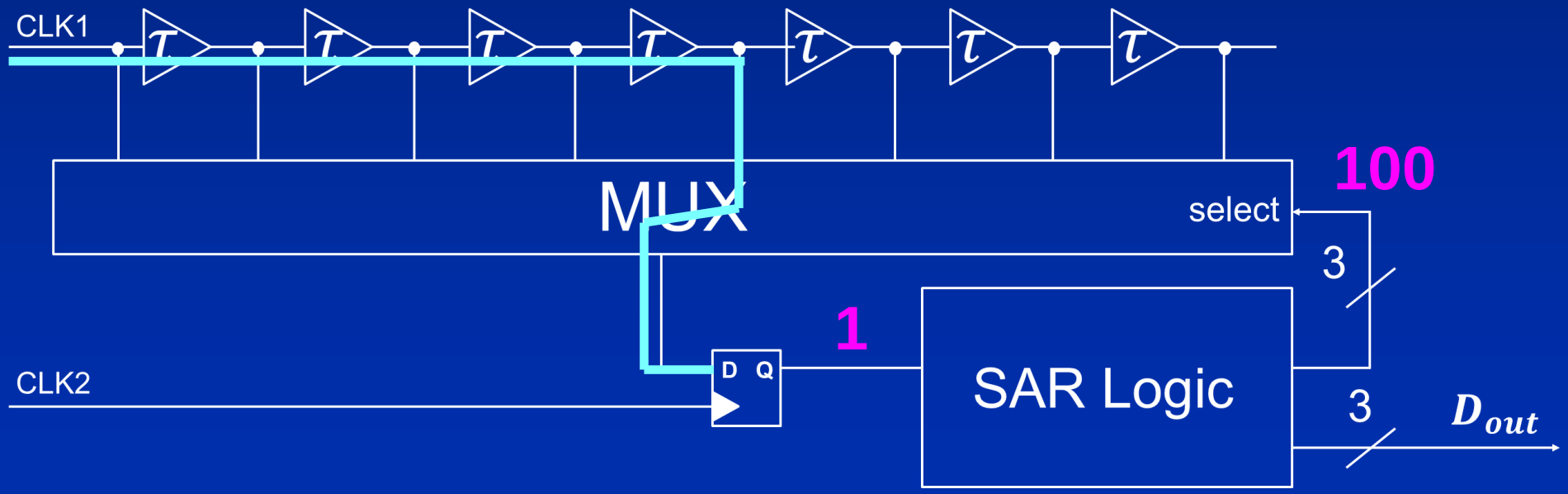
SAR TDC operation

STEP1



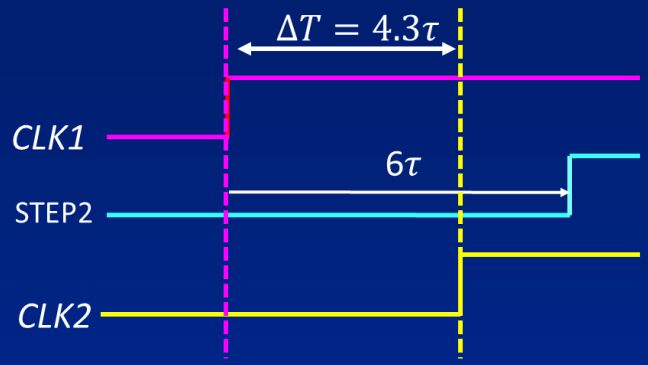


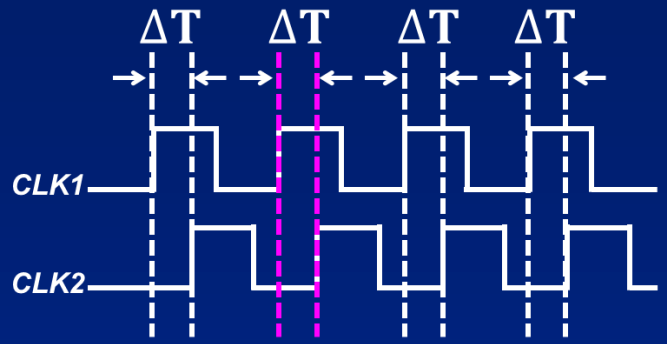
Example $\Delta T = 4.3\ \tau$



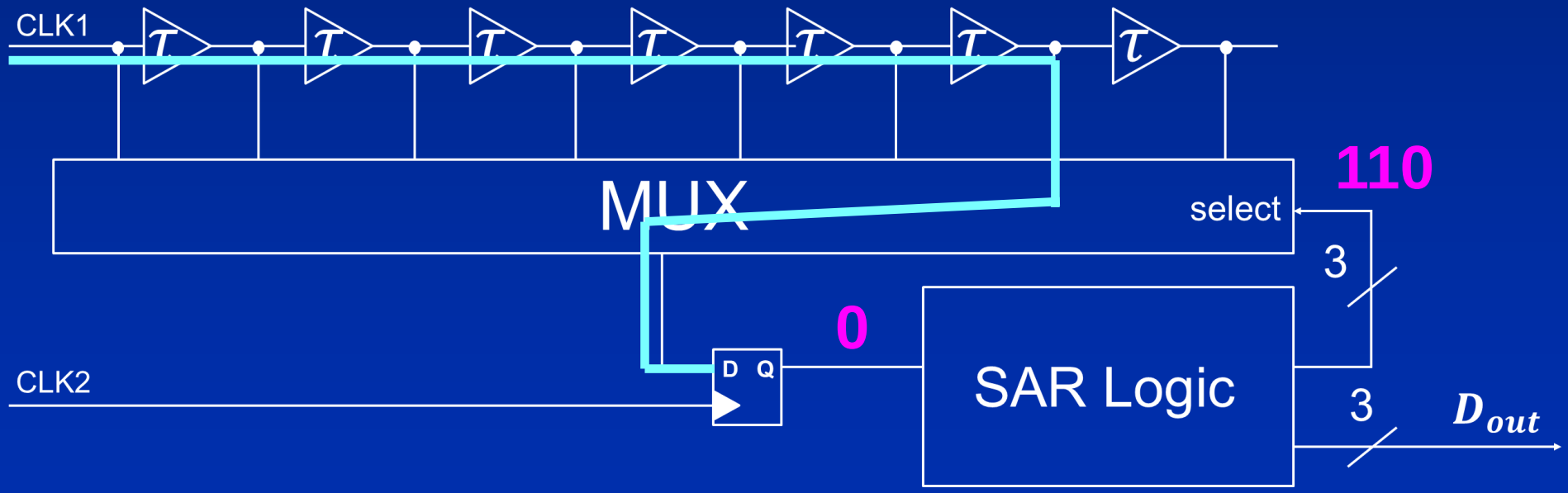
SAR TDC operation

STEP2



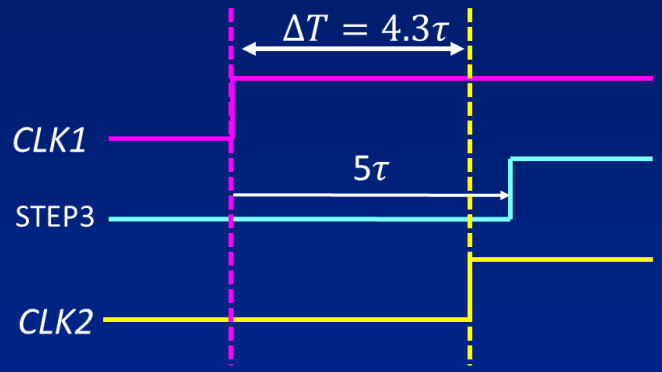


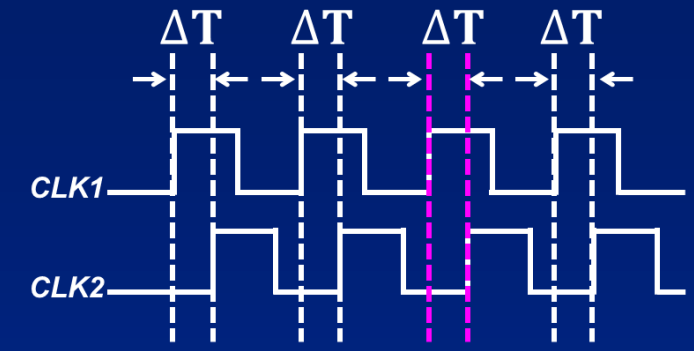
Example $\Delta T = 4.3\ \tau$



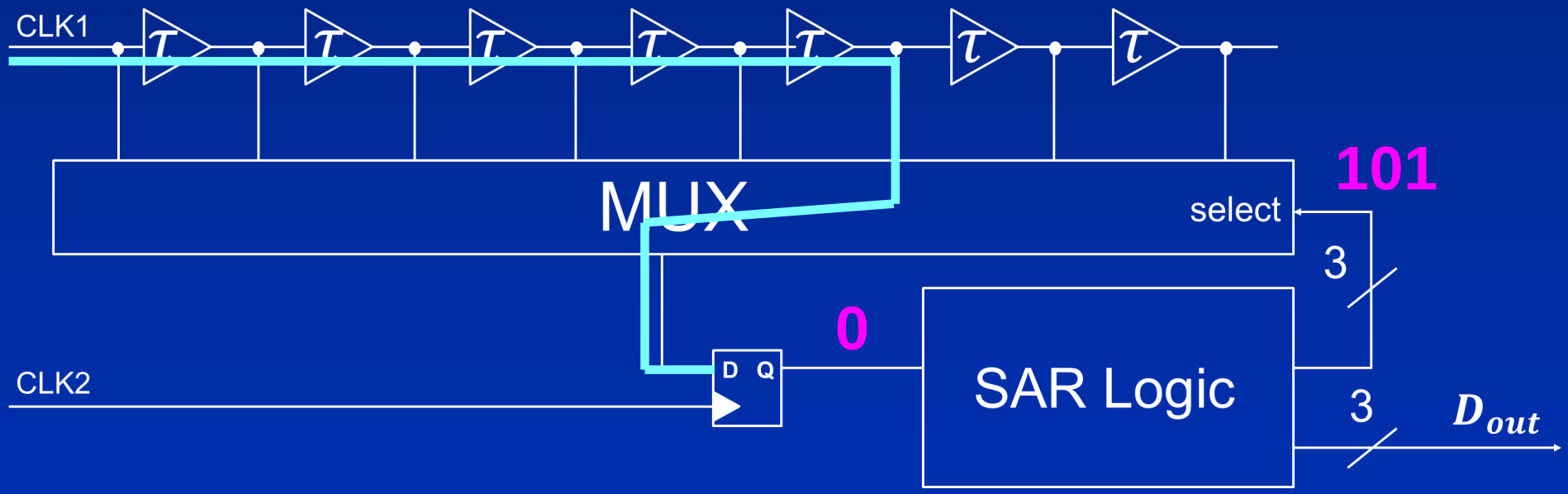
SAR TDC operation

STEP3



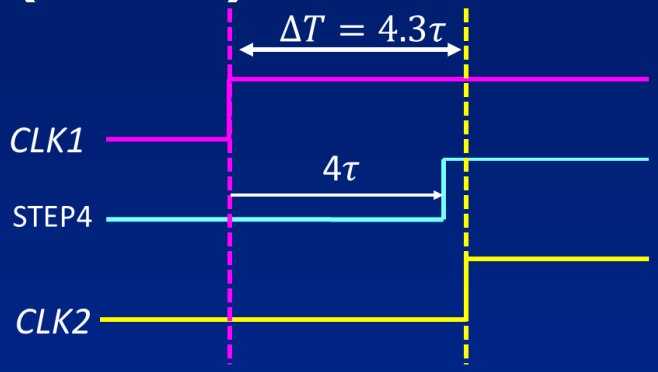


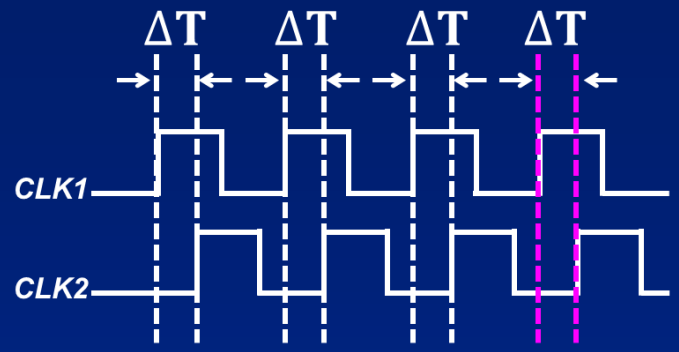
Example $\Delta T = 4.3\ \tau$



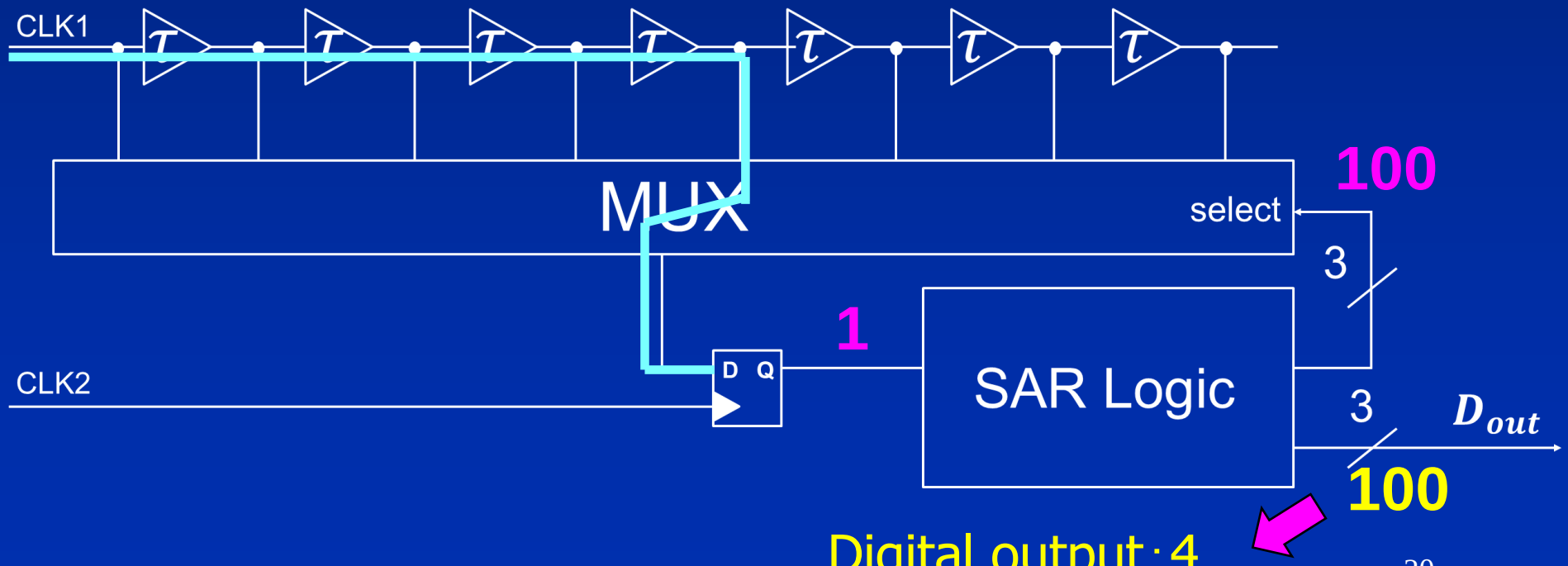
SAR TDC operation

STEP4 (Stable)





Example $\Delta T = 4.3\ \tau$



Digital output : 4

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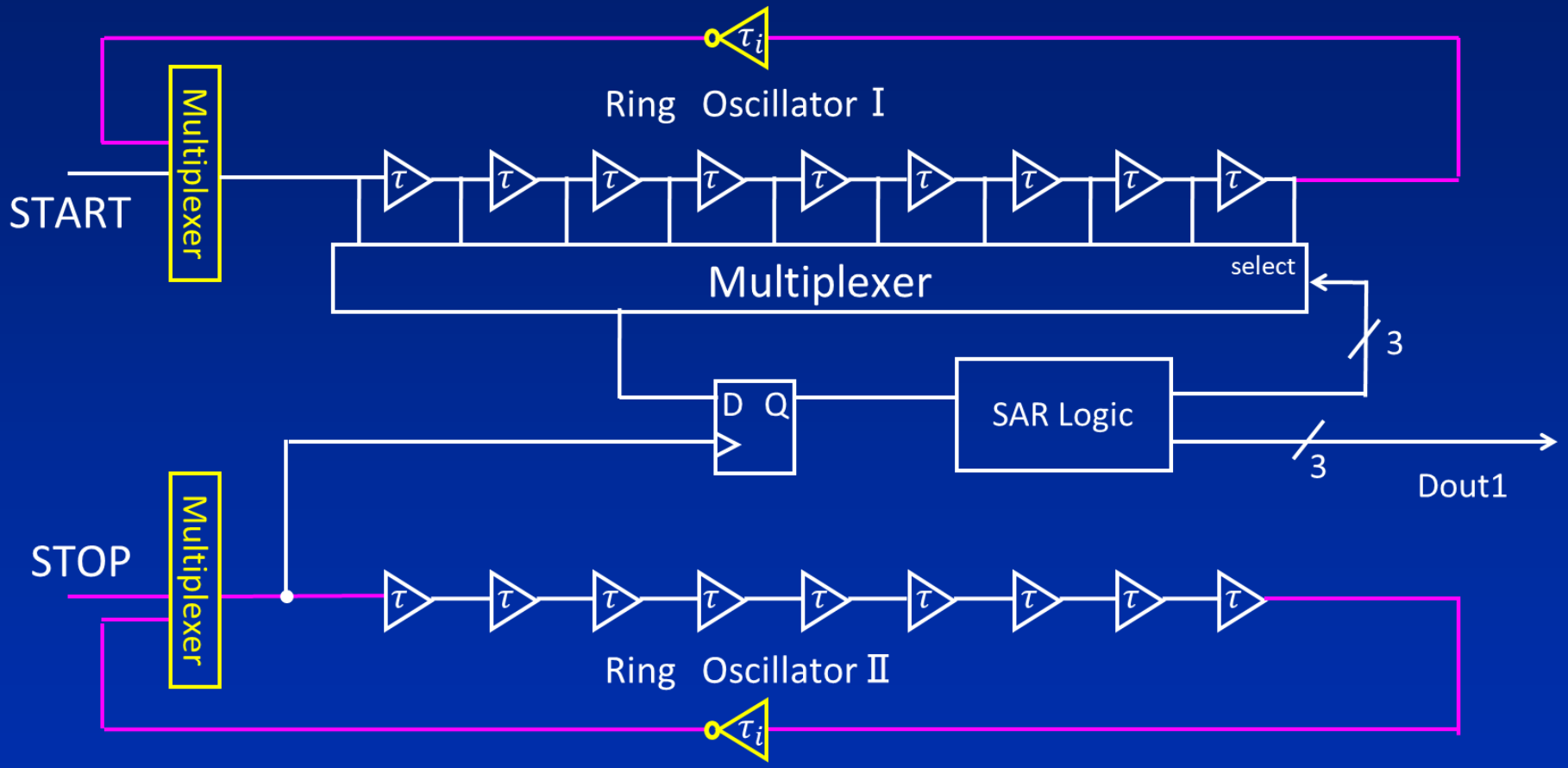
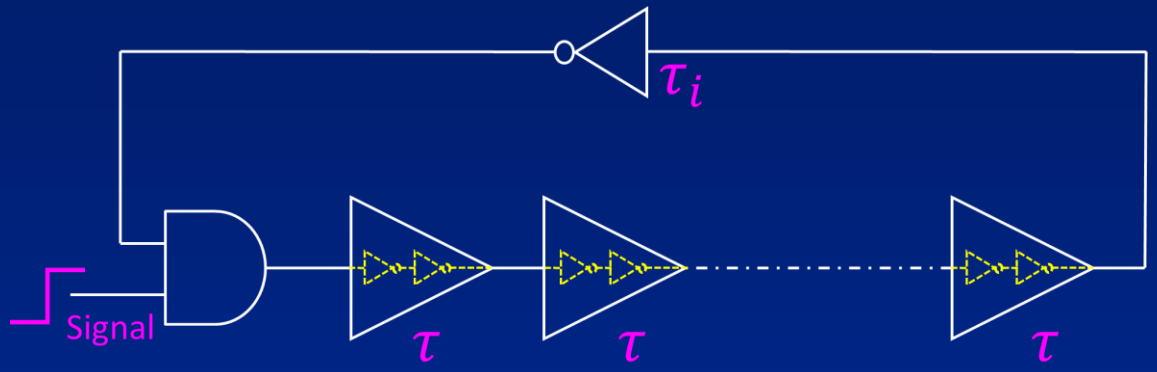
SAR-TDC employing 2-ring oscillators

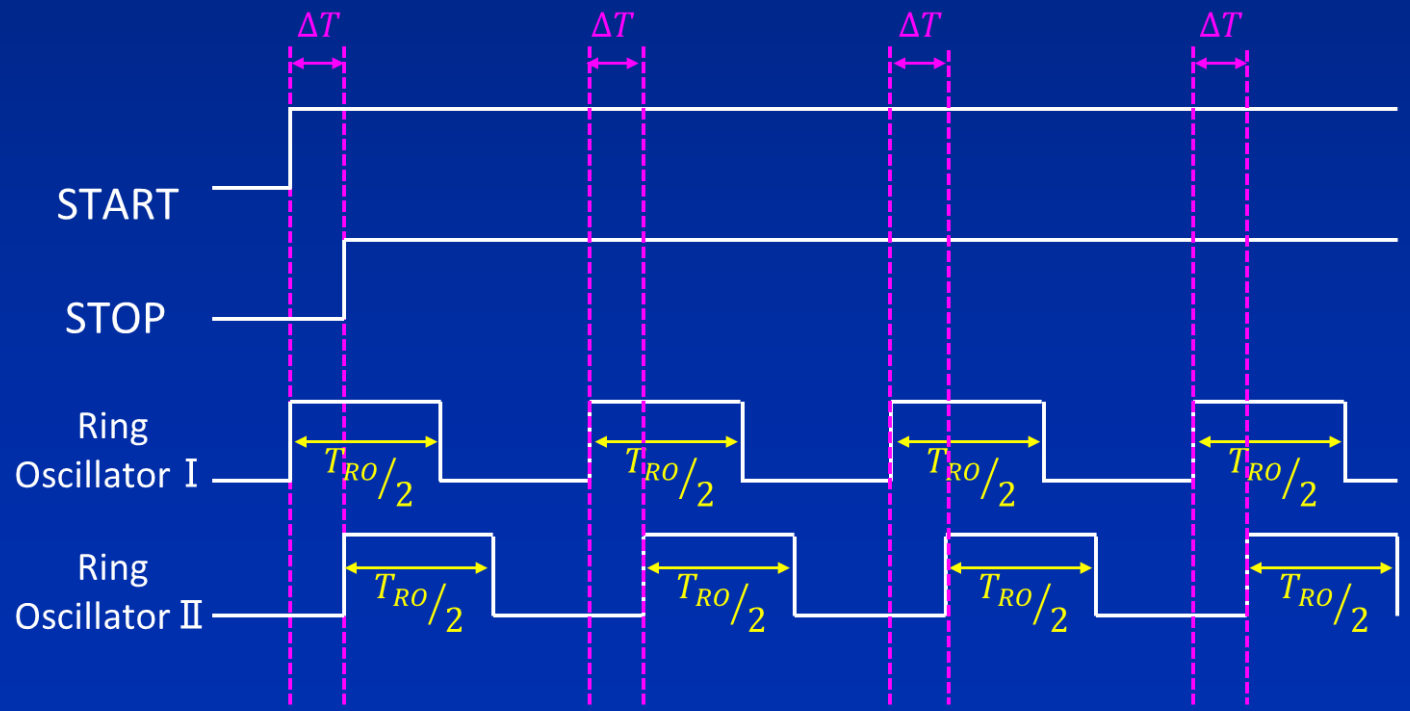


Ring oscillator timing chart

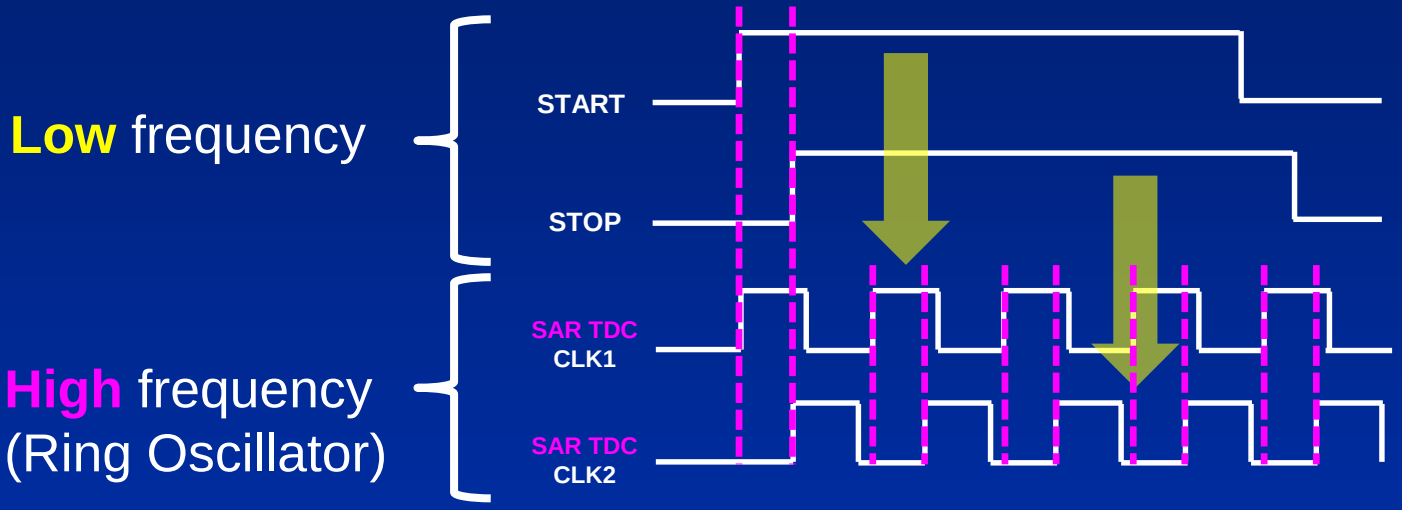


$$T_{RO} = 2(n\tau + \tau_i)$$

$$\mathbf{0} < \Delta T < {}^{T_{RO}}/_{2}$$

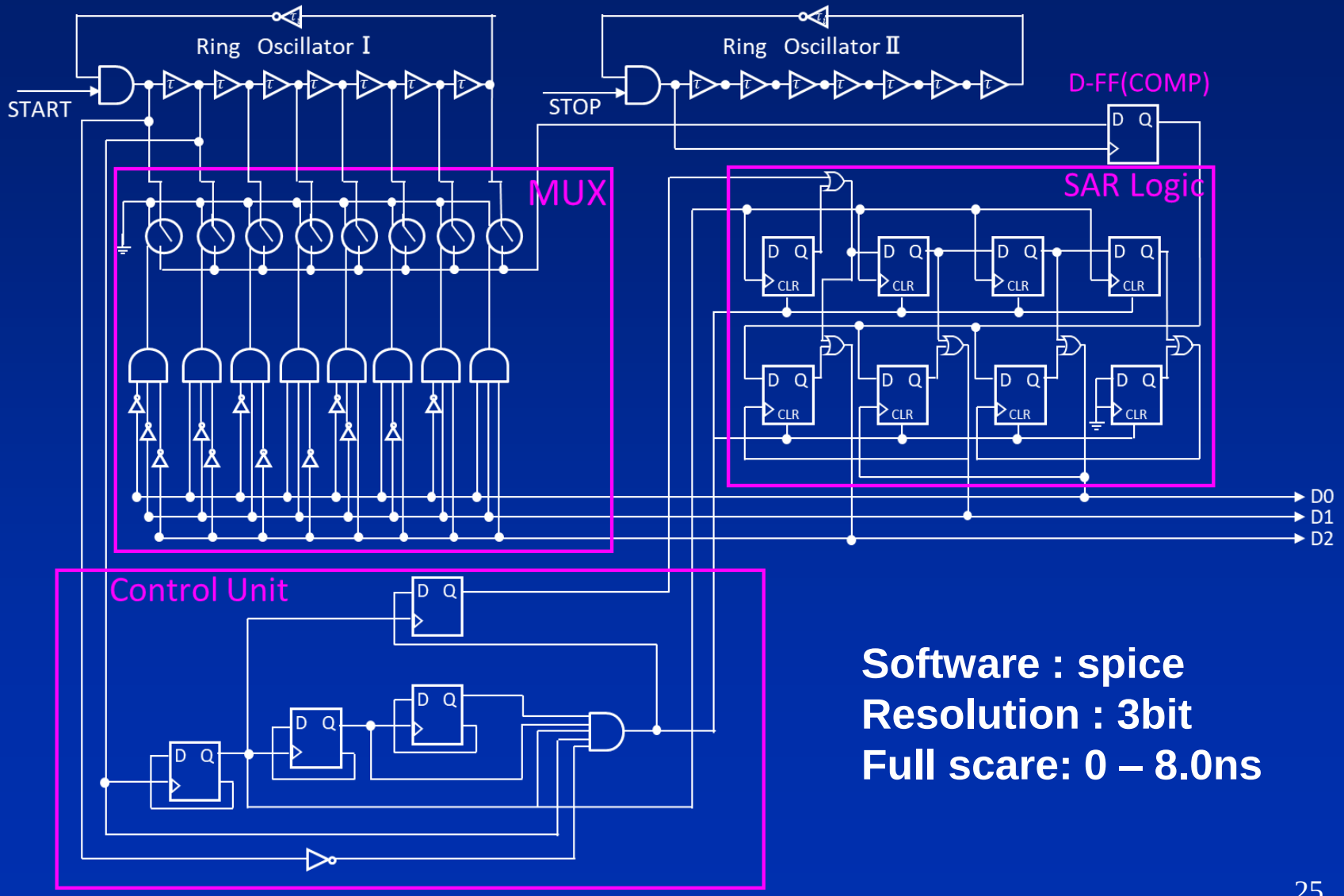


Low frequency clock measurement



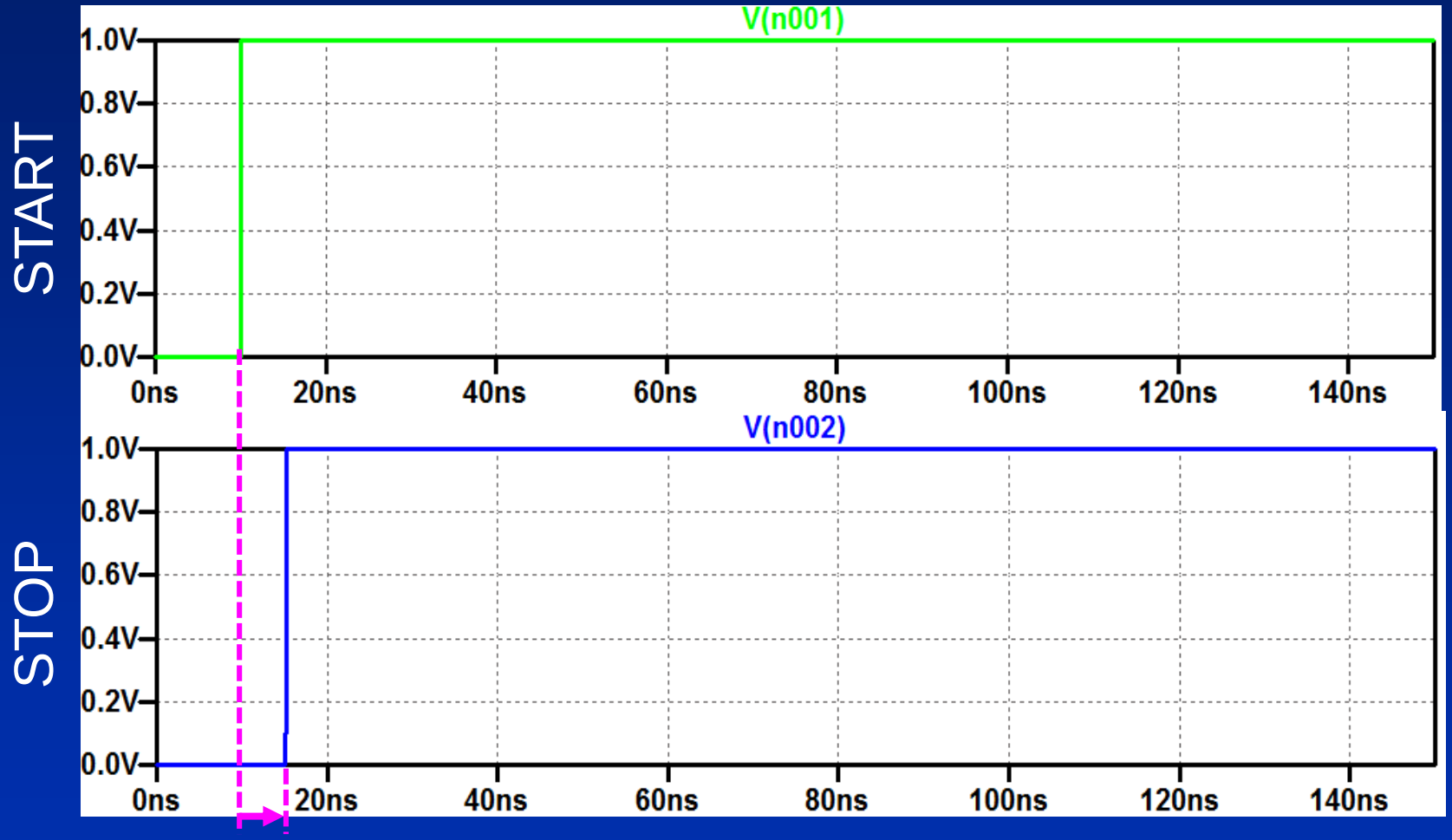
Short testing time for low frequency repetitive timing

Simulated circuit



Software : spice
Resolution : 3bit
Full scare: 0 – 8.0ns

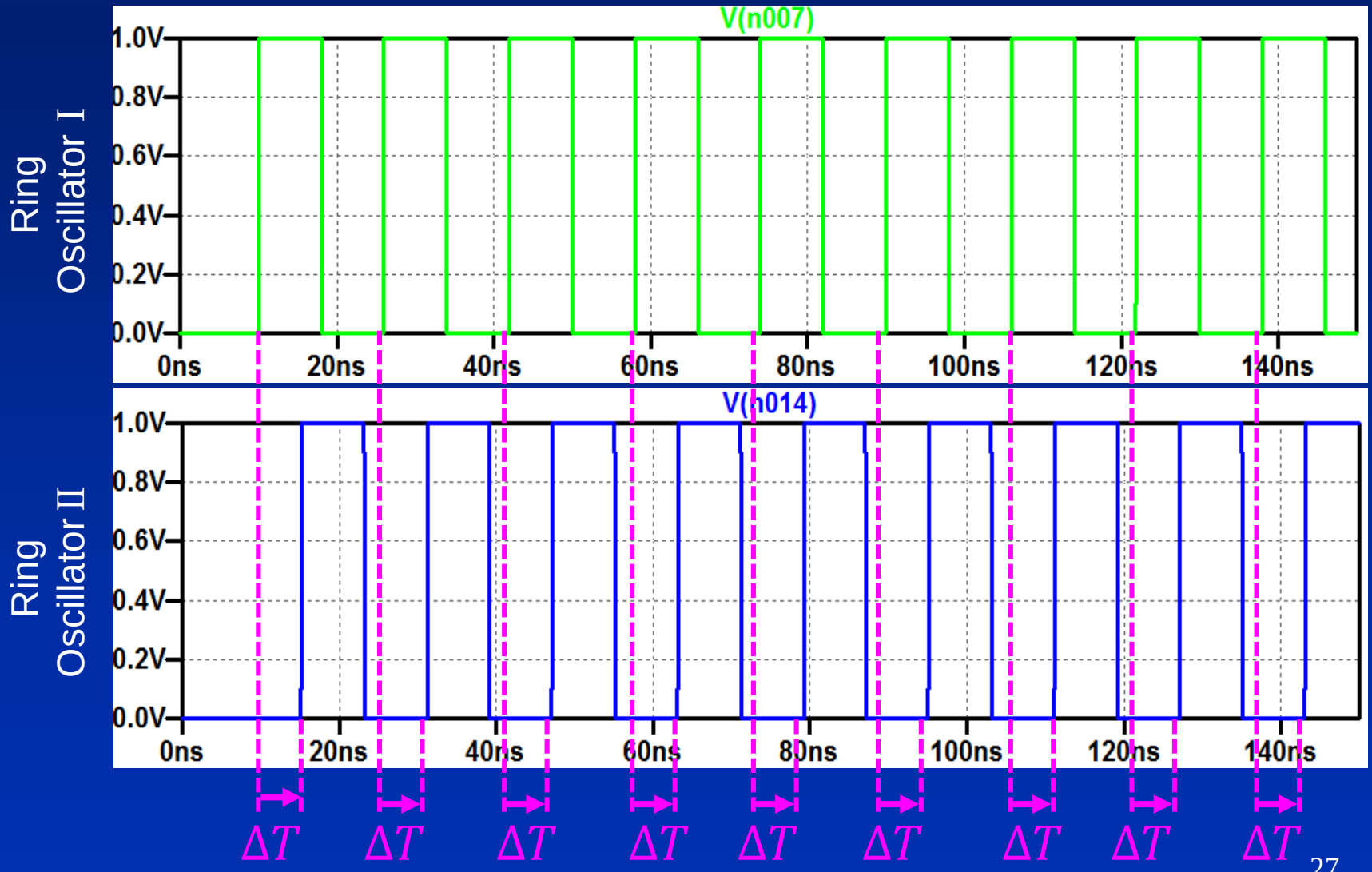
One shot input timing signal



$\Delta T = 5.2ns$

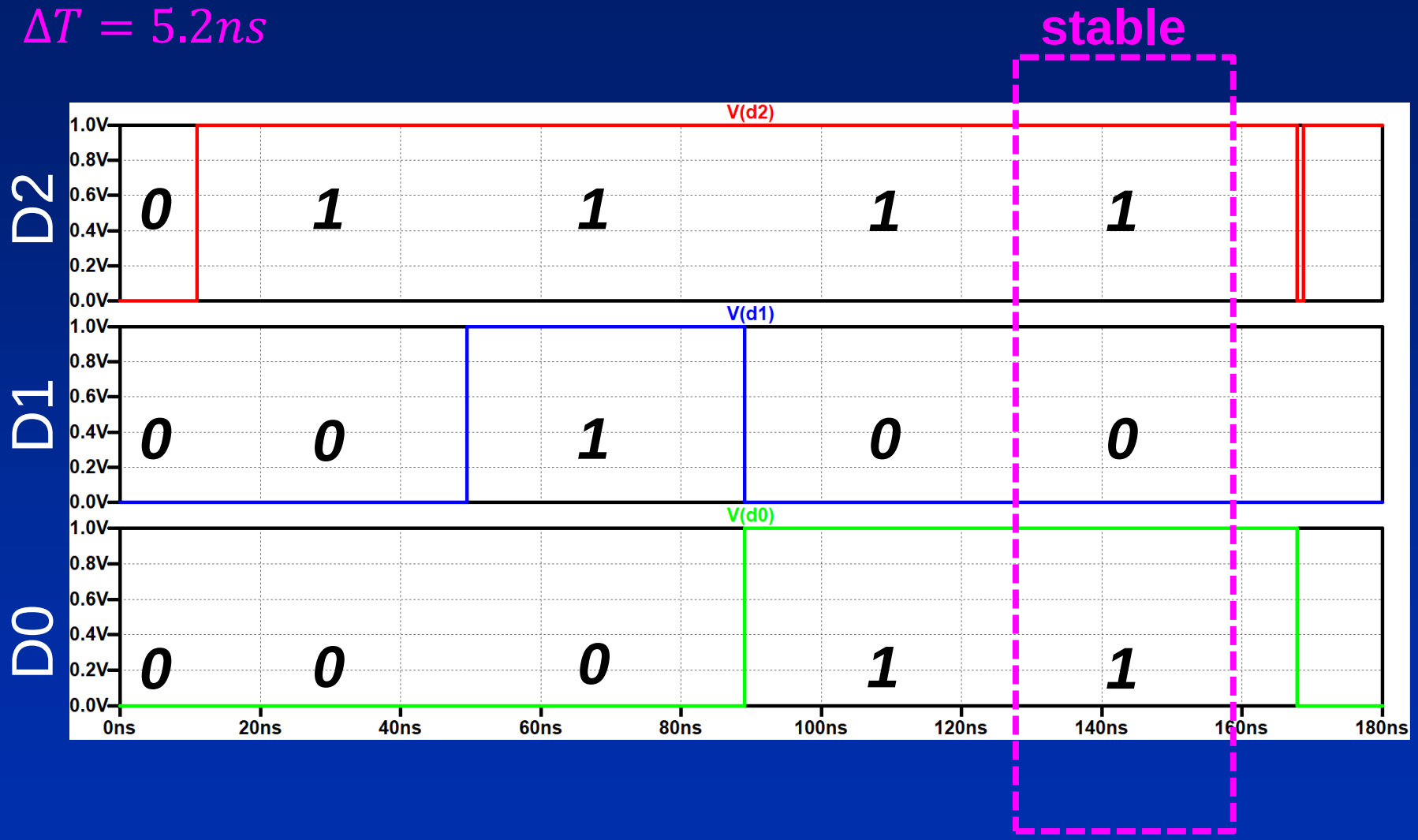
Simulated ring oscillator waveforms

$\Delta T = 5.2ns$



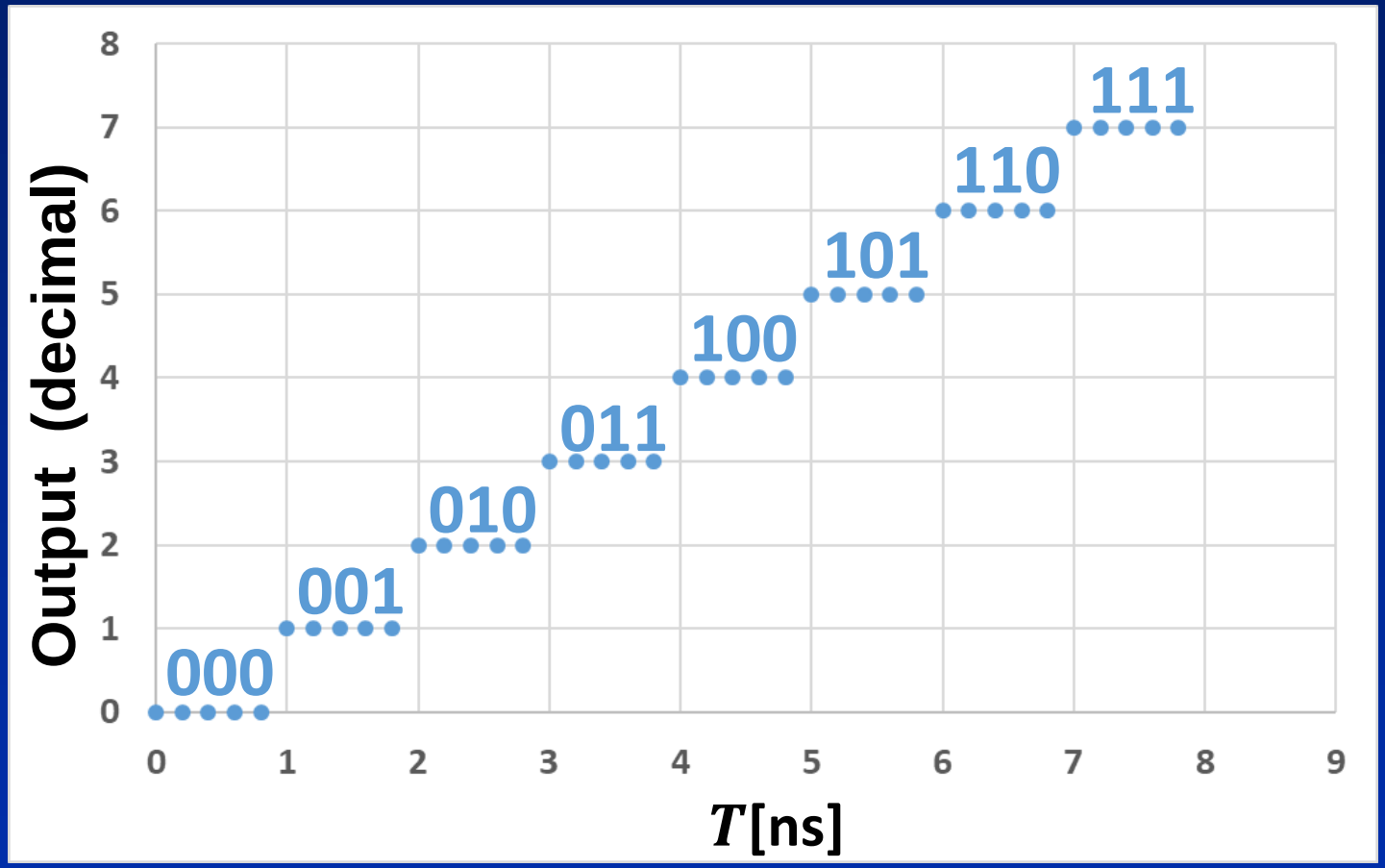
D-FF output signal at each steps

$\Delta T = 5.2ns$



101 ➡ $5.0ns \leq \Delta T < 6.0ns$

Input output linearity



SAR TDC employing ***2 ring oscillators*** input & output have linear relationship

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Summary

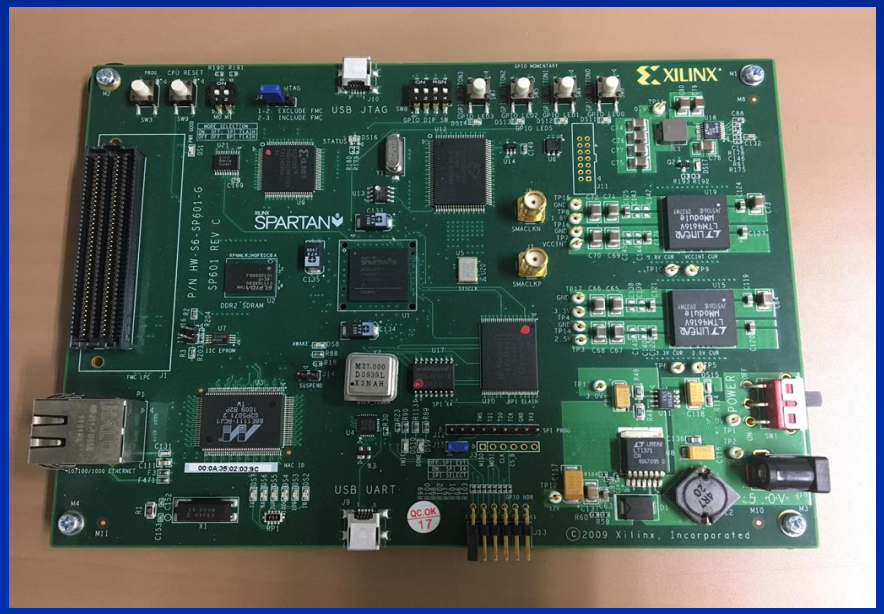
- One shot timing can be measured with SAR TDC
- Ring oscillator can generate repetitive clock timing
- Full digital implementation employing ring oscillators. Suitable for high & low frequency repetitive clock timing

✓Small circuit
✓One shot timing
✓Full digital
✓High linearity
✓High resolution

Timing testing at low cost

Future works

- FPGA implementation
- Experiment using signal generator
- Calibrate oscillation frequency mismatch of ring oscillator



Thank you for your attention

Appendix

Q&A(1)

Q1 実際の回路の要求仕様的には満たしているのか

A1 従来のカウンタタイプのTDCは計測対象の時間の間に何回カウンタが回るかという方法で時間を測定していた。このTDCは1クロック未満でも計測出来るのが利点。FPGAのボードの性能やカスタムICの性能にもよるがnsオーダーの時間計測であればカウンタでは数十GHzに相当する時間計測が可能。

Q&A(2)

Q2　アナログ回路を使わなくても良い利点とは

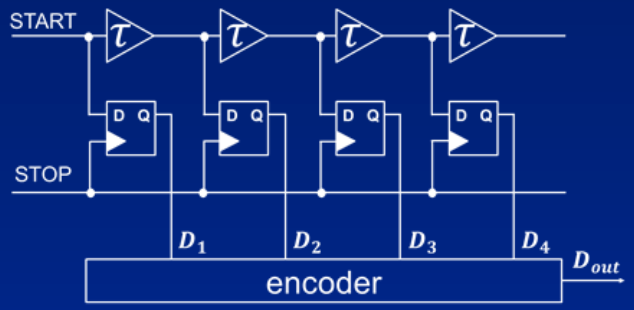
A2　アナログ回路はキャパシタなどの素子（チップ面積大）を使わなくてはならず、高コスト。またアナログ回路の設計者も限られており、設計の容易化という面でも不利。デジタルであればハードウェア言語でプログラミングすることで自動合成できるので設計容易でアナログ回路と比較するとコストでメリットが大きい。

Q&A(3)

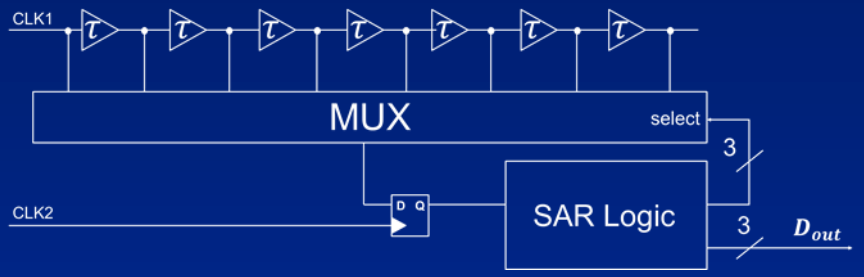
Q3 単発信号のアプリケーションとは

A3 クロックタイミング試験は基本的には繰り返し信号。しかし他のTOFや距離計測、科学実験など、単発信号しか入力出来ないアプリケーションも存在する。そのようなアプリケーションでも使える可能性があるというという期待もある。

Flash TDC vs. SAR TDC



Flash TDC



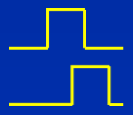
SAR TDC

10-bit :1023

# of D-FFs

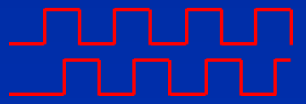
10-bit : 23

One Shot



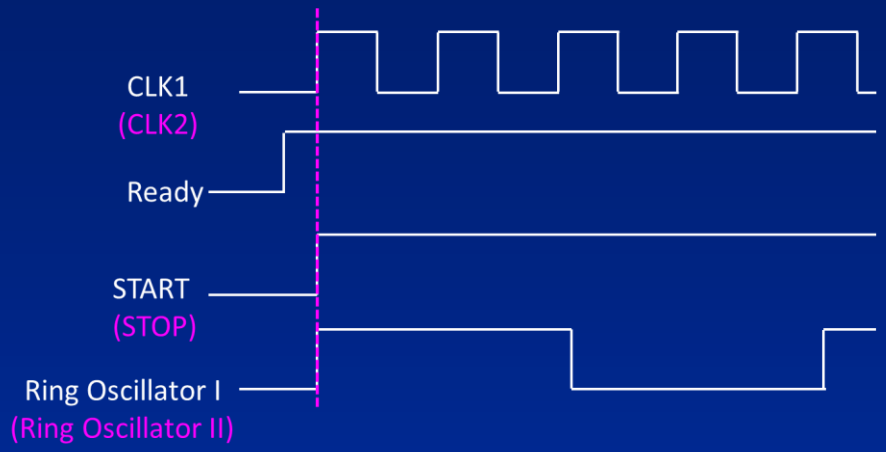
Timing Signal

Repetitive



High & low frequency clock measurement

High Frequency

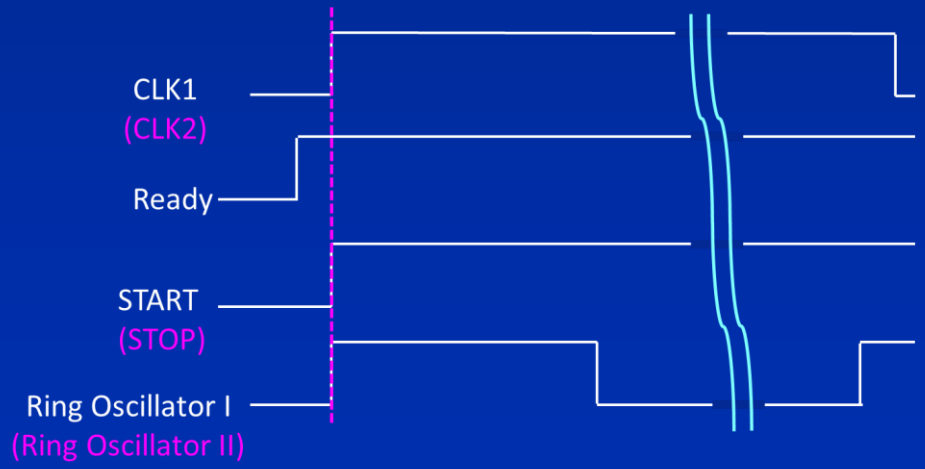


2GHz

Ring Oscillator

$10ns \times 10 = 100ns$

Low Frequency



0.01Hz

Ring Oscillator

$10ns \times 10 = 100ns$

Short testing time for low frequency repetitive timing