High-Resolution Low-Sampling-Rate ΔΣ ADC
Linearity Short-Time Test Algorithm


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ROHM Semiconductor
OUTLINE

• Research background and objective
• Proposed linearity test method
• Simulation configuration and results
• Conclusion
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IOT (Internet of things)

- Testing and evaluation of IOT devices are becoming important.

- Mass production shipment of IOT devices requires high quality and low cost testing.
Research Objective

High resolution, low speed $\Delta \Sigma$ ADC

- Sensor interface key components
- Mass production test

- Linearity test takes a long time.
- In most cases, it is omitted.

High reliability requirements

- Perform its linearity test in a short time
- Develop its algorithm
ΔΣ ADC Testing Challenge

Sensor + amplifier + ΔΣADC + microcomputer

4 difficulties for its mass production shipping test.

① Low speed sampling
② High resolution
③ High linearity analog input signal
④ Complex ADC output signal processing

1 US dollar chip

Test time should be less than 1 second
ADC Role in Digital Era

Analog signal: continuous signal

Digital signal: discrete numerical signal

- Natural signal (sound, light)
- Analog clock
- Binary number
- Digital clock

Sampling Clock
ΔΣ ADC

- Measurement
- Audio system
- Satellite communication
Linearity of ΔΣ ADC

Ideal characteristic (linear)

Actual (nonlinear)

Circuit imperfection, variation

Nonlinear

Linearity:

- Important performance item
- Need its accurate test in a short time.
Integral Non-Linearity: INL

If INL is large:

- Missing codes occur
- Lack of monotonicity

Deviation between the ideal input threshold value and the measured threshold level of a certain output code.
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Problem of Direct Linearity Test

ΔΣ ADC

Analog input

ΔΣ AD modulator

1 bit output

32ksps

Digital Filter

Data decimation

Digital output

Stepwise signal

24

7sps 24bit

Seven 24-bit data output per second

Linearity test time
Assuming 4 point per code
(1/7) x 2^{24} x 4 seconds = 104 day!

Totally unrealistic
Digital Filter Test

ΔΣ ADC

ΔΣ AD modulator → 1bit output 32ksps → Digital Filter

Data decimation → Digital output

Analog input → 7sps 24bit

Digital filter does NOT affect the linearity.
Only pass or fail.

Test with scan path method
ΔΣ AD Modulator Test

Proposed: Cosine Input & FFT Analysis

ΔΣ ADmodulator

1-bit output
32ksps

Digital Filter

Data decimation

Pin test output data

FFT analysis

Analog input

A cos(ωt)

32000 1-bit data output per second

7sps 24bit

Digital output

Seven 24-bit data output per second

24

Seven 24-bit data output per second

Seven 24-bit data output per second

32ksps

1-bit output

2019/11/8
Modeling by polynomial approximation

Assumption: I/O characteristics are continuous in the AD modulator.

$$y = a_0 + a_1 x + a_2 x^2 + \cdots + a_n x^n$$

3rd order model for simplicity:

$$y(t) = a_1 x(t) + a_3 x(t)^3$$
Polynomial Coefficient Estimation

Analog cosine input:
\[ x(t) = A \cos(\omega t) \]

Modulator 1-bit output stream

FFT

Measure fundamental & 3\textsuperscript{rd} harmonic power

Estimate \(a_1, a_3\):
\[ y(t) = a_1 x(t) + a_3 x(t)^3 \]
Fundamental / 3rd Harmonic Power and Polynomial Coefficients

Cosine input:

\[ x(t) = A \cos \omega t \]

Output characteristic model:

\[ y(t) = a_1 x(t) + a_3 x(t)^3 \]

\[ y(t) = a_1 A \cos \omega t + a_3 (A \cos \omega t)^3 \]

\[ (a_1 A + \frac{3}{4} a_3 A^3) \cos \omega t + \frac{1}{4} a_3 A^3 \cos 3\omega t \]

Fundamental:

\[ a_1 A + \frac{3}{4} a_3 A^3 \]

3rd harmonic:

\[ \frac{1}{4} a_3 A^3 \]
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Proposed ΔΣ ADC linearity test method

● Highly accurate estimation of polynomial coefficients from FFT values

● Modulator 1 bit data output of $2^{20}$

$$2^{20} / (32 \times 1000) = 32 \text{ seconds}$$

● Test time drastically reduced

● 32 pieces are tested in parallel simultaneously, equivalent testing time per unit is 1 second.
$V_m = E - k \times E^3 (k>0)$

1st-order Modulator, 3rd-order Nonlinearity Model

3rd-order nonlinearity model

1st-order modulator
DC Input Simulation

- Number of data: \( N = 2^{20} \)
- \( V_{in} : DC = -1.0 \sim +1.0 \)
- \( k = 0.0001, 0.0005, 0.001, 0.005, 0.01 \)

\[
V_m = E - k \cdot E^3 \quad (k > 0)
\]

\[V_{in} + E \rightarrow M \rightarrow V_m \rightarrow \sum \rightarrow V_0 \rightarrow \Delta \rightarrow D_{out}
\]

Control by the number of 1’s

Modulator 1-bit output

«0» or «1»

1\textsuperscript{st} -order modulator
DC Input Simulation Result

Number of modulator output: \( N=2^{20} \)

Number of output 1's

\[
y = a_3 x^3 + a_1 x
\]

<table>
<thead>
<tr>
<th>( k )</th>
<th>( a_3 )</th>
<th>( a_1 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0001</td>
<td>104.84</td>
<td>524180</td>
</tr>
<tr>
<td>0.0005</td>
<td>524.48</td>
<td>523760</td>
</tr>
<tr>
<td>0.0010</td>
<td>1050.5</td>
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<tr>
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<td>10643.0</td>
<td>513610</td>
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Cosine Input Simulation Configuration

\[ V_m = E - k \times E^3 (k > 0) \]

Control by the number of 1’s

\[ V_m = E - k \times E^3 (k > 0) \]

Modulator 1-Bit output
「0」 or 「1」

1st-order modulator

- Number of data: \( N = 2^{20} \)
- \( V_{in} : A \cos(\omega t) (A = 0.1 \sim 1) \)
- \( k = 0.0001, 0.0005, 0.001, \)
  0.005, 0.01

Power [dB] vs. frequency (Hz)

fundamental - P1

3rd harmonic - P3
Cosine Input Simulation Result

**Number of modulator output:**

\[ N = 2^{20} \]

**FFT result**

\[
\text{Power} = 20 \log(\text{FFT}_{value}) - 6.02 \text{ [dB]}
\]
Find Spectrum Power from DC Characteristics

- 1st-order modulator
- Number of 1-bit output data: \( N=2^{20} \)

By nonlinearity

**Fundamental**: \( a_1A + \frac{3}{4}a_3A^3 \)

**3rd harmonic**: \( \frac{1}{4}a_3A^3 \)

**A**: amplitude

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Comparison Between Estimated and FFT Values

Fundamental values

Amplitude

Estimation error of fundamental

Estimation error of $3^{rd}$ harmonic

$P_1$: fundamental obtained by FFT
$Q_1$: estimated fundamental

$P_3$: $3^{rd}$ harmonic obtained by FFT
$Q_3$: estimated $3^{rd}$ harmonic

Error = \frac{Q_{values} - P_{values}}{Q_{values}}

$P_1 = 0.0001$
$Q_1 = 0.0001$
$P_3 = 0.0001$
$Q_3 = 0.0001$

$P_1 = 0.0005$
$Q_1 = 0.0005$
$P_3 = 0.0005$
$Q_3 = 0.0005$

$P_1 = 0.001$
$Q_1 = 0.001$
$P_3 = 0.001$
$Q_3 = 0.001$

$P_1 = 0.005$
$Q_1 = 0.005$
$P_3 = 0.005$
$Q_3 = 0.005$

$P_1 = 0.01$
$Q_1 = 0.01$
$P_3 = 0.01$
$Q_3 = 0.01$
Accurate Estimation Condition for 3rd Harmonic

1st-order modulator

Good condition
3rd harmonic

Amplitude = 0.9
Error = 0.0123%
(k = 0.0005)
Comparison of 1\textsuperscript{st} and 2\textsuperscript{nd} -order Modulators

1\textsuperscript{st} -order modulator

Estimation error of fundamental

Error is random

Amplitude

Estimation error (*100%)

k=0.0001, k=0.0005, k=0.001, k=0.005, k=0.01

Estimation error of 3\textsuperscript{rd} harmonic

A : 0.9
Error : 0.0123% (k : 0.0005)

2\textsuperscript{nd} -order modulator

Estimation error of fundamental

Error is stable

Amplitude

Estimation error (*100%)

k=0.0001, k=0.0005, k=0.001, k=0.005, k=0.01

Estimation error of 3\textsuperscript{rd} harmonic

A : 0.9
Error : 0.0103114% (k : 0.001)
DUT Measurement Result

- Measurements results from Rohm semiconductor company

- Signal from our developed AWG (AWG: Arbitrary Waveform Generator)

- Use of NI PXI system for experiment

- Obtained INL prediction with the proposed method

<table>
<thead>
<tr>
<th>Output</th>
<th>1kHz 44.1ksp</th>
<th>THD</th>
<th>122dB (~Fifth Harmonics)</th>
<th>SN</th>
<th>132dB(Filter:20kHzLPF)</th>
</tr>
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</table>

-120dB(1ppm limit)

-109[dBV]

-11[dBV]

-2.208[ppm]
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High resolution, low speed ΔΣ ADC linearity short time testing algorithm

- Polynomial modeling of modulator input / output characteristics
- FFT of modulator 1-bit output stream for cosine input
- Estimate polynomial coefficients from fundamental and harmonic powers

Verified by simulation and experiments that the proposed method is feasible.

Drastic testing time reduction:
104 days → 32 seconds
Future Work

Consideration of the followings:

● Higher-order distortions
  High-order polynomial modeling

● Application to high-order modulators

● Application to multi-bit modulators
No Science without Measurement

No Production without Testing

Lord Kelvin

Kelvin P.M.
Thanks for listening!
Appendix
First order modulator:
Input: DC = 1
Sampling: 16Bit

\[ V_{m} = V_{1} - k \cdot V_{1}^{3} \quad (k > 0) \]

\[ V_{1}(i) = V_{\text{in}}(i) - V_{3}(i) \]
\[ V_{m}(i) = V_{1}(i) - k \cdot V_{1}(i)^{3} \quad (K > 0) \]
\[ V_{2}(i) = V_{2}(i-1) + V_{m}(i) \]

V1, Vm, V2 Values ➡ Always 0

Nonlinearity Model

V3 value ➡ Always 1

If A=1
Estimation error become bigger

So, A=1.
⇒ It can’t be modulator.
Merits & Demerits of ΔΣ DAC

**Merit**
- Mostly digital circuit
- High linear & high resolution for low frequency signal generation

**Demerit**
- Limit cycle problem for small input

※ Due to modulator nonlinearity by quantizer
DC small signal input

Digital input

Small signal input

Analog output

Limit cycle

Estimation error of 3^{rd} harmonic

Power [dB]

Frequency [Hz]

Fs/2

Estimation error (*100%)

Amplitude
Limit cycle solution

< Features >

① NOT sacrifice input range

② NOT affect signal band, thanks to noise-shaping

③ Easily generate random signal.

I published at ICSICT in 2018
First-order modulator ($3^{rd}$ nonlinearity)

**fundamental**

Sampling: 18Bit  A : 0.9 ~ 1  amplitude increase step: 0.01

The fundamental estimation error of 18Bit

Sampling: 18Bit  A : 0.999 ~ 1  amplitude increase step: 0.0005

The fundamental estimation error of 18Bit
First-order modulator (3\textsuperscript{rd} nonlinearity)

- **3\textsuperscript{rd} harmonic**
- **Sampling: 18Bit**
  - A : 0.9 ~ 1 amplitude increase step : 0.01
  - The 3\textsuperscript{rd} harmonics estimation error of 18Bit

- **Sampling: 18Bit**
  - A : 0.999 ~ 1 amplitude increase step : 0.0005
  - The 3\textsuperscript{rd} harmonics estimation error of 18Bit

Good value
- A = 0.9995
First-order modulator

3rd harmonic

10 Bit

12 Bit

14 Bit

16 Bit

18 Bit

20 Bit

Amplitude

Power (dB)

Amplitude

Power (dB)

Amplitude

Power (dB)

Amplitude

Power (dB)