High-Resolution Low-Sampling-Rate ΔΣ ADC Linearity Short-Time Test Algorithm

Jiang-Lin Wei, N. Kushita, T. Arai, L. Sha,
A. Kuwana, H. Kobayashi , T. Nakatani, K. Hatayama
Gunma University

K. Sato, T. Ishida, T. Okamoto, T. Ichikawa
ROHM Semiconductor

群馬大学
GUNMA UNIVERSITY

OUTLINE

- Research background and objective
- Proposed linearity test method
- Simulation configuration and results
- Conclusion

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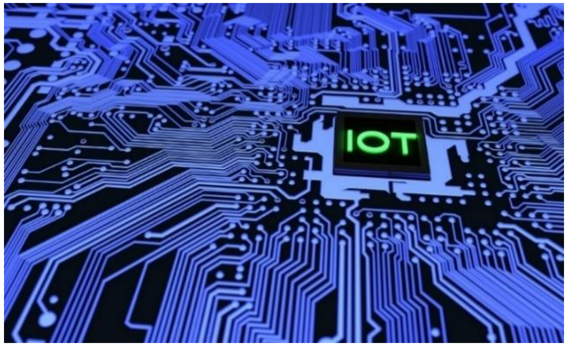
Research Background

IOT（Internet of things）

- Testing and evaluation of IOT devices are becoming important.



- Mass production shipment of IOT devices requires high quality and low cost testing.

Research Objective

High resolution, low speed ΔΣ ADC

- Sensor interface key components
- Mass production test
  - ✓ Linearity test takes a long time.
  - ✓ In most cases, it is omitted.

High reliability requirements

- ✓ Perform its linearity test in a short time
- ✓ Develop its algorithm

ΔΣ ADC Testing Challenge

Sensor ＋ amplifier ＋ ΔΣADC ＋ microcomputer

4 difficulties for its mass production shipping test.

① Low speed sampling
② High resolution

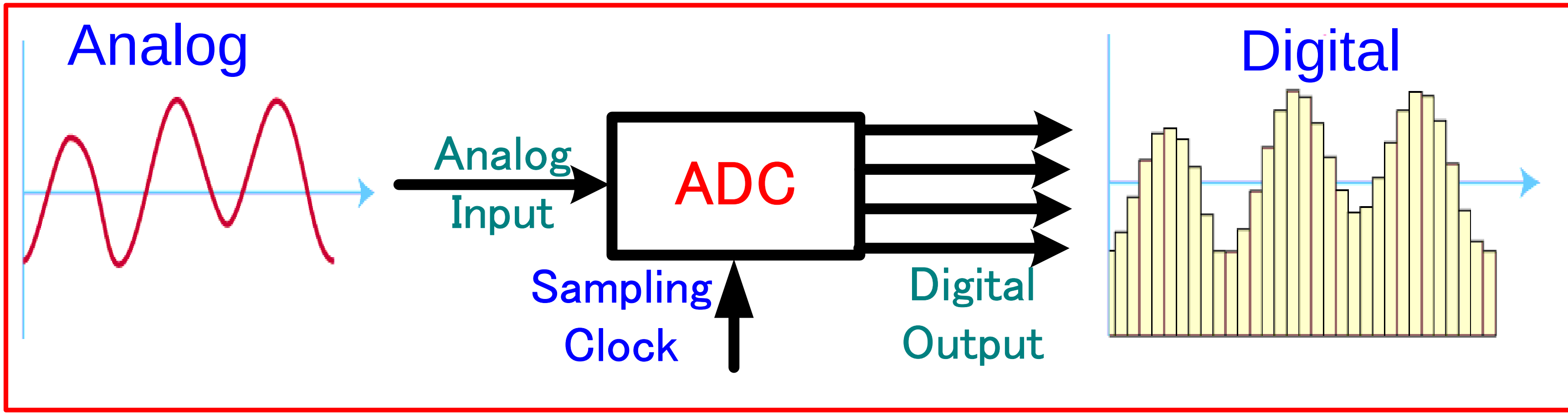
→ Long test time

③ High linearity analog input signal
④ Complex ADC output signal processing

1 US dollar chip

Test time should be less than 1 second

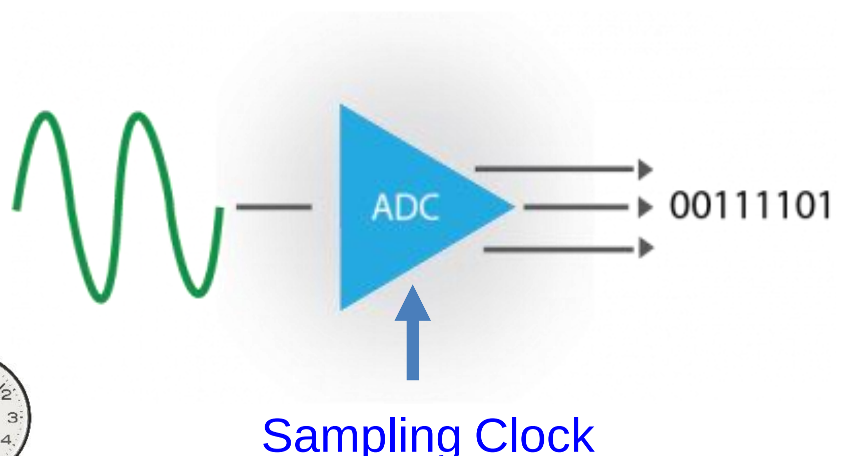
ADC Role in Digital Era



Analog signal :
continuous signal

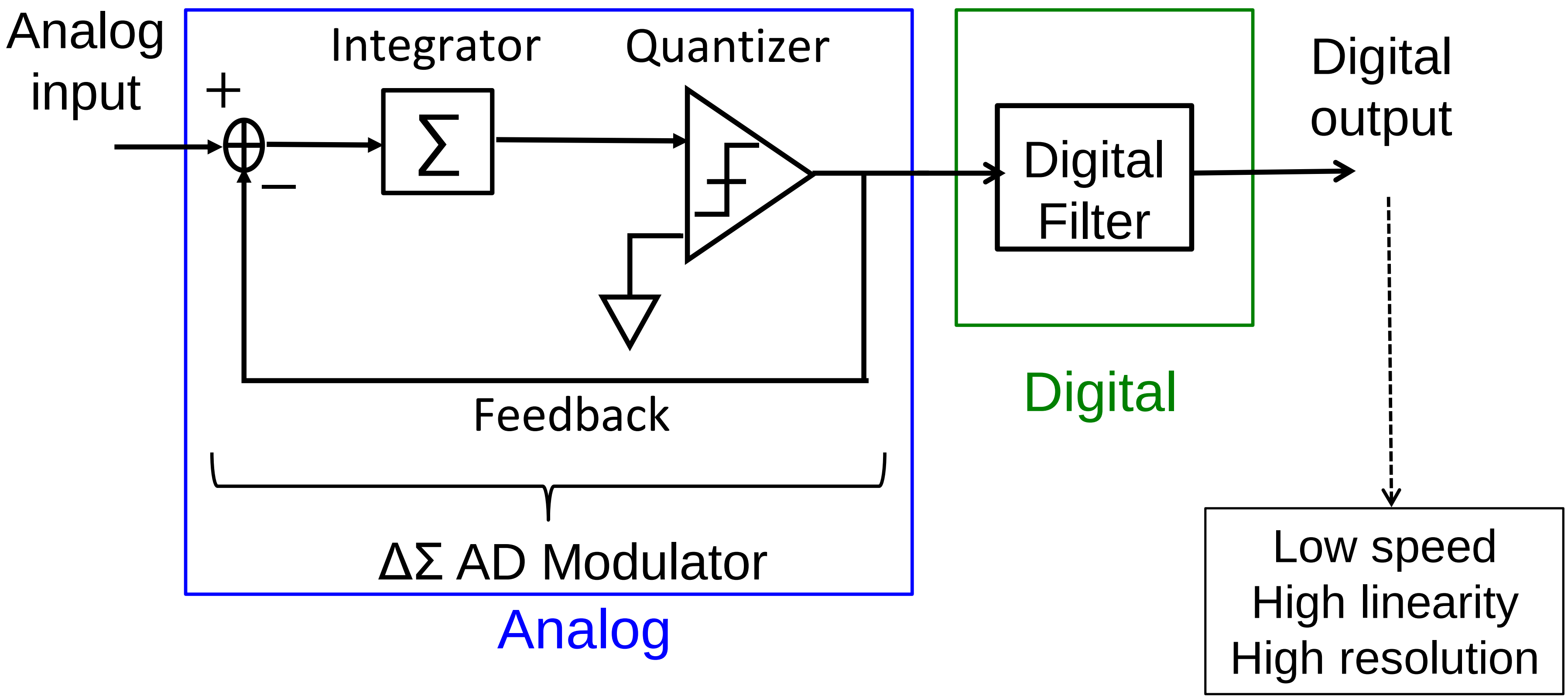
Digital signal :
discrete numerical signal

- Natural signal (sound, light)
- Analog clock



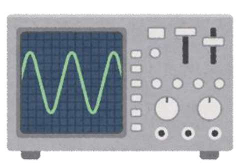
- Binary number
- Digital clock

ΔΣ ADC



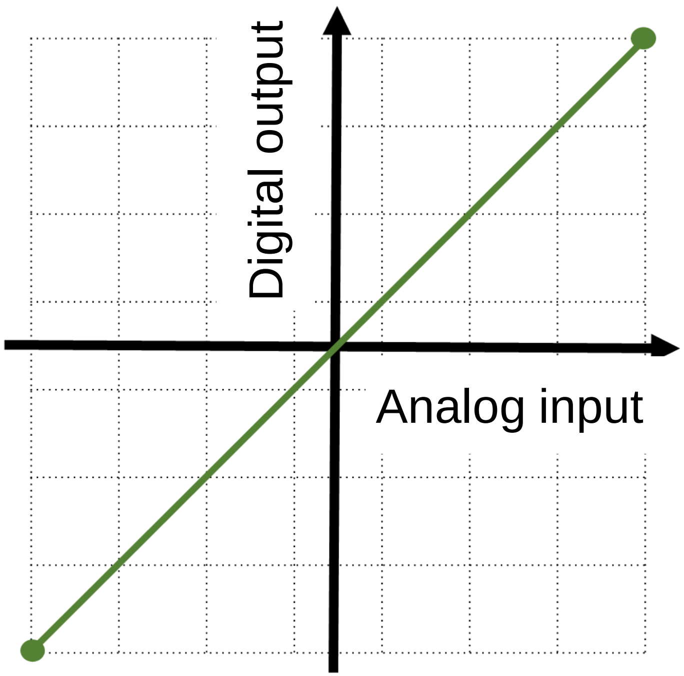
＜Application＞

- Measurement
- Audio system
- Satellite communication

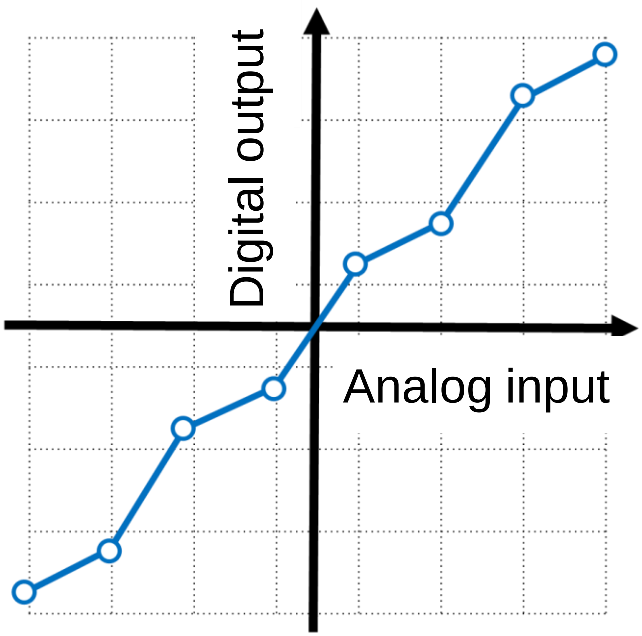


Linearity of ΔΣ ADC

Ideal characteristic (linear)



Actual (nonlinear)



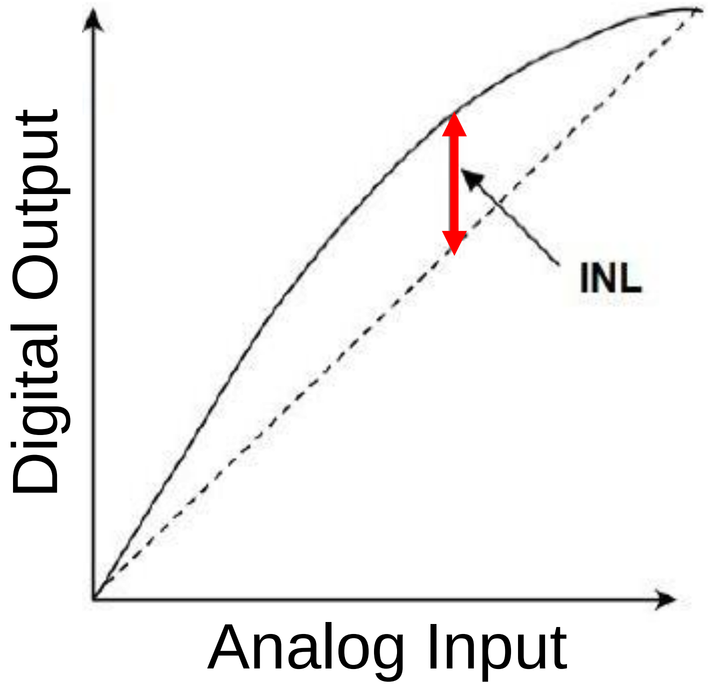
Circuit imperfection, variation ➡ Nonlinear

Linearity :

✓Important performance item

✓Need its accurate test in a short time.

Integral Non-Linearity: INL



If INL is large :

- ✓ Missing codes occur
- ✓ Lack of monotonicity

Deviation between the ideal input threshold value and the measured threshold level of a certain output code.

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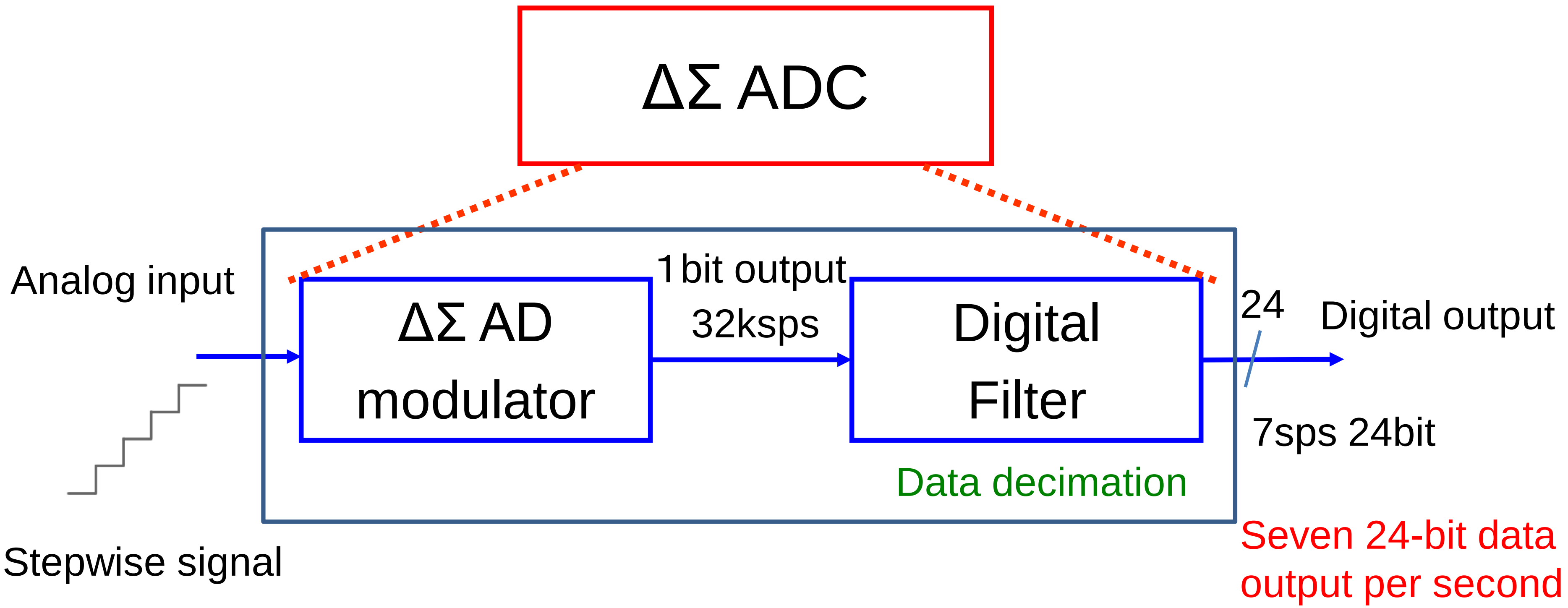
Problem of Direct Linearity Test



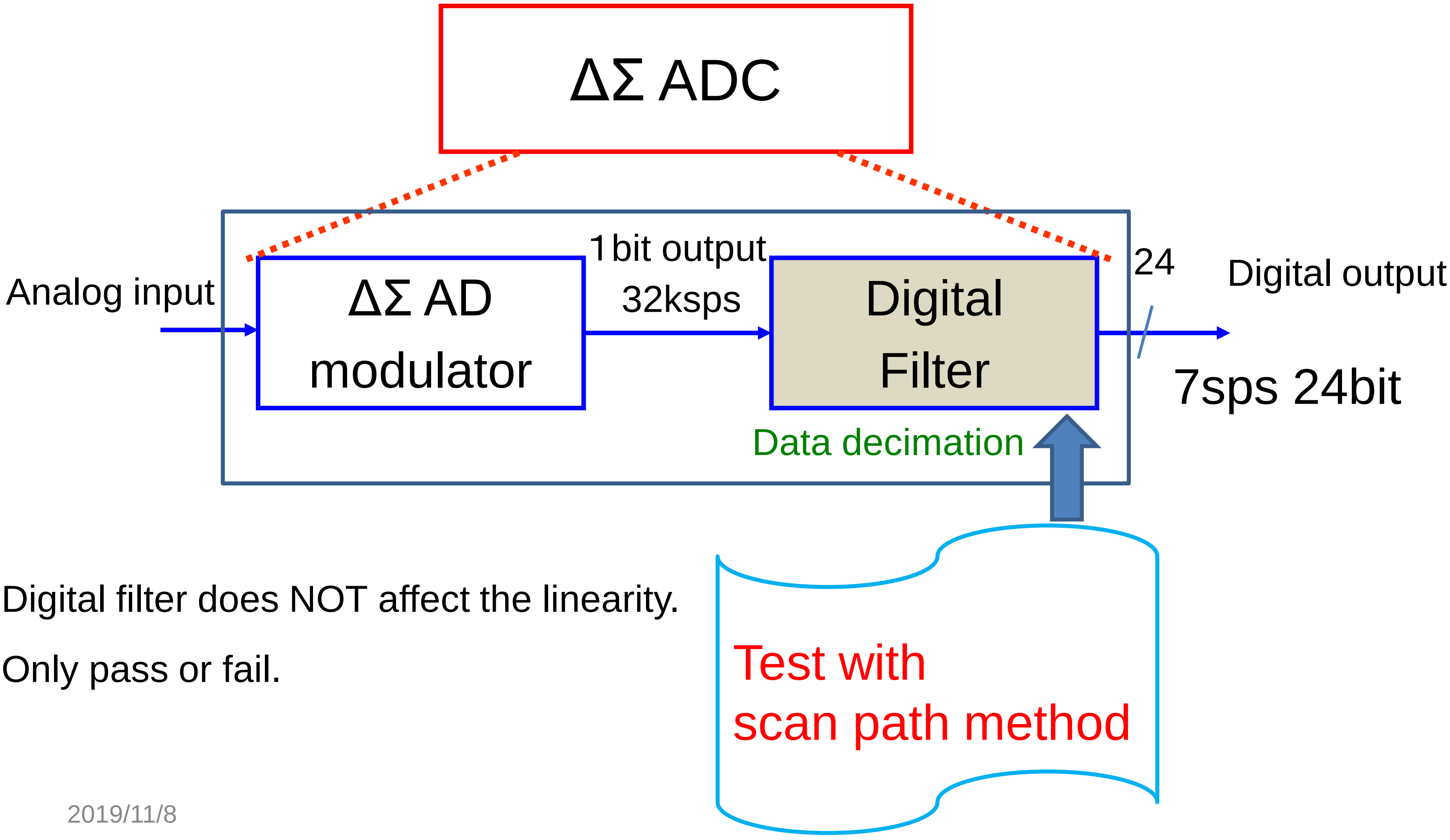
<u>Linearity test time</u>

Assuming 4 point per code

$(1/7) \times 2^{24} \times 4$ seconds = 104 day !

→ Totally unrealistic

Digital Filter Test

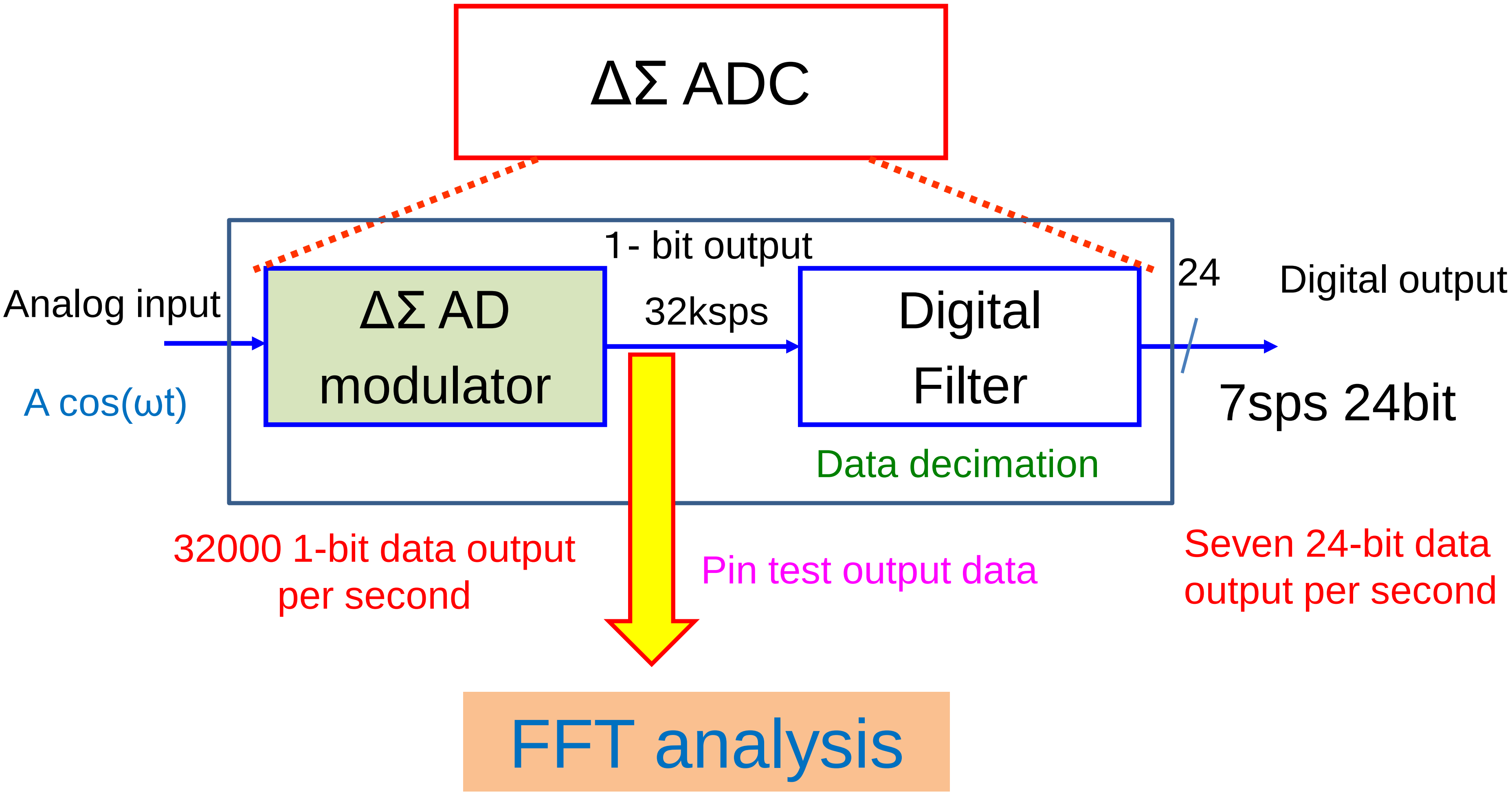


Digital filter does NOT affect the linearity.

Only pass or fail.

ΔΣ AD Modulator Test

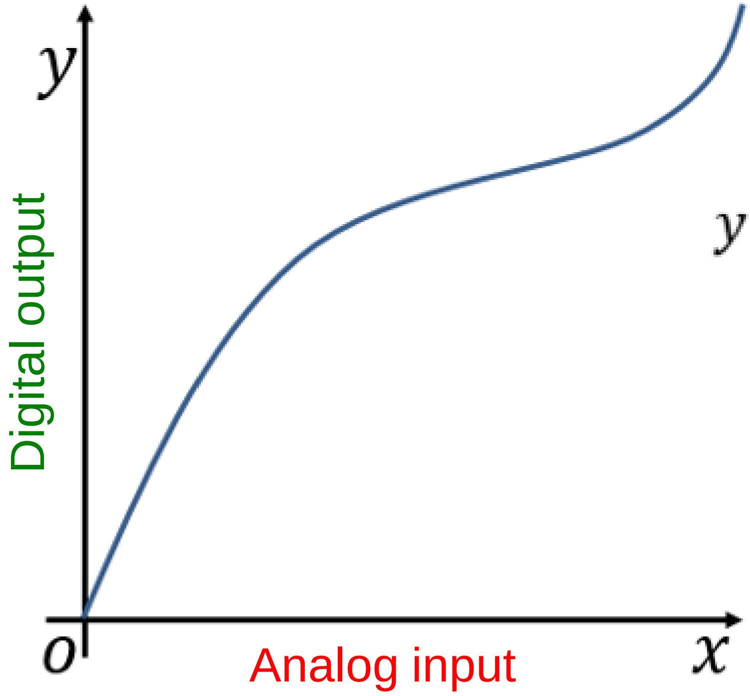
Proposed: Cosine Input & FFT Analysis



I/O Characteristic Modeling of Modulator

Modeling by polynomial approximation

✓ Assumption: I/O characteristics are continuous in the AD modulator.



$$y = a_0 + a_1 x + a_2 x^2 + \cdots + a_n x^n$$

3rd order model for simplicity :

$$y(t) = a_1 x(t) + a_3 x(t)^3$$

Polynomial Coefficient Estimation

Analog cosine input :
x(t) = A cos(ωt)

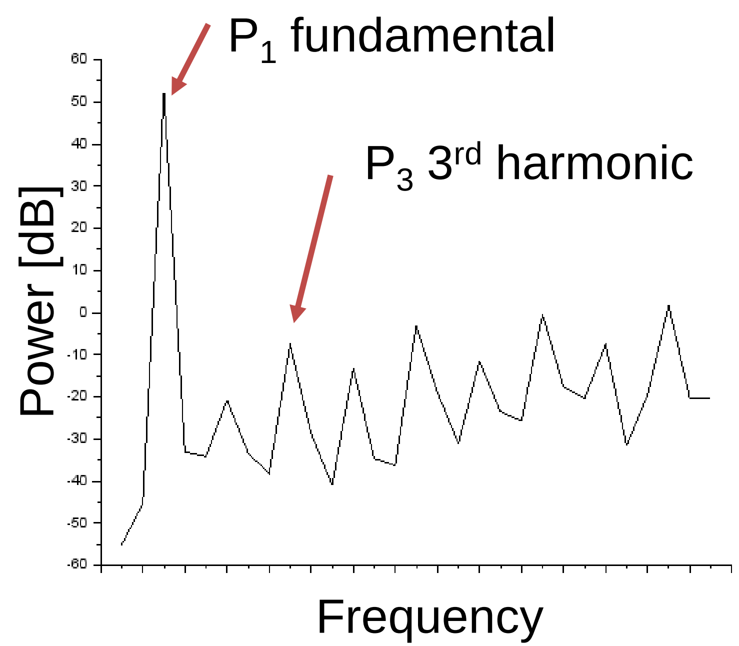
Modulator 1-bit output stream

FFT

Measure fundamental &
3rd harmonic power

Estimate a_1,a_3 :
$y(t) = a_1 x(t) + a_3 x(t)^3$

Proposed algorithm



Fundamental / 3rd Harmonic Power and Polynomial Coefficients

Cosine input :

$$x(t) = A\cos \omega t$$

Output characteristic model :

$$y(t) = a_1 x(t) + a_3 x(t)^3$$

$$y(t) = a_1 A\cos \omega t + a_3 (A\cos\omega t)^3$$

$$(a_1 A + \frac{3}{4} a_3 A^3)\cos\omega t \quad + \quad \frac{1}{4} a_3 A^3 \cos 3\omega t$$

Fundamental

$$a_1 A + \frac{3}{4} a_3 A^3$$

3rd harmonic

$$\frac{1}{4} a_3 A^3$$

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Simulation Verification of Proposed Algorithm

Proposed ΔΣ ADC linearity test method

- Highly accurate estimation of polynomial coefficients from FFT values
- Modulator 1 bit data output of 2^{20}

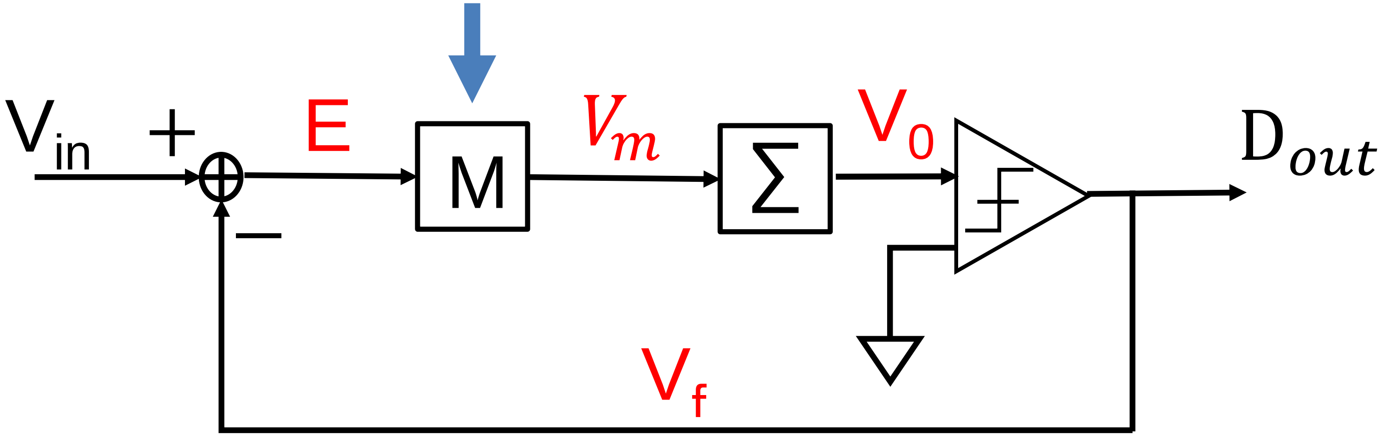
  2^{20} / (32 x 1000) = 32 seconds

- Test time drastically reduced
- 32 pieces are tested in parallel simultaneously, equivalent testing time per unit is 1 second .

1st-order Modulator, 3rd-order Nonlinearity Model

3rd-order nonlinearity model

$V_m = E - k * E^3$ (k>0)

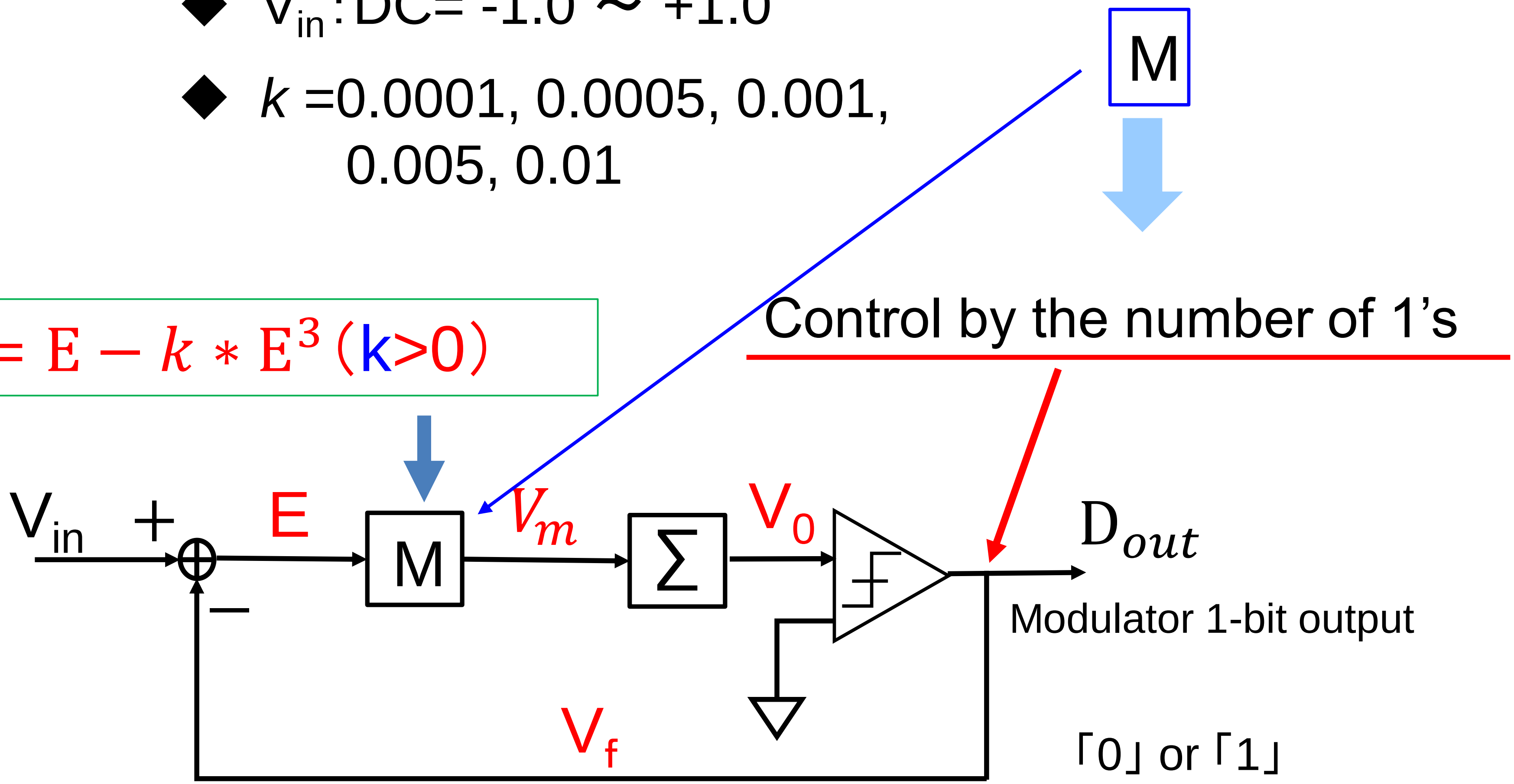


1st-order modulator

DC Input Simulation

- Number of data : $N=2^{20}$
- V_{in} : DC= -1.0 ～ +1.0
- k =0.0001, 0.0005, 0.001, 0.005, 0.01

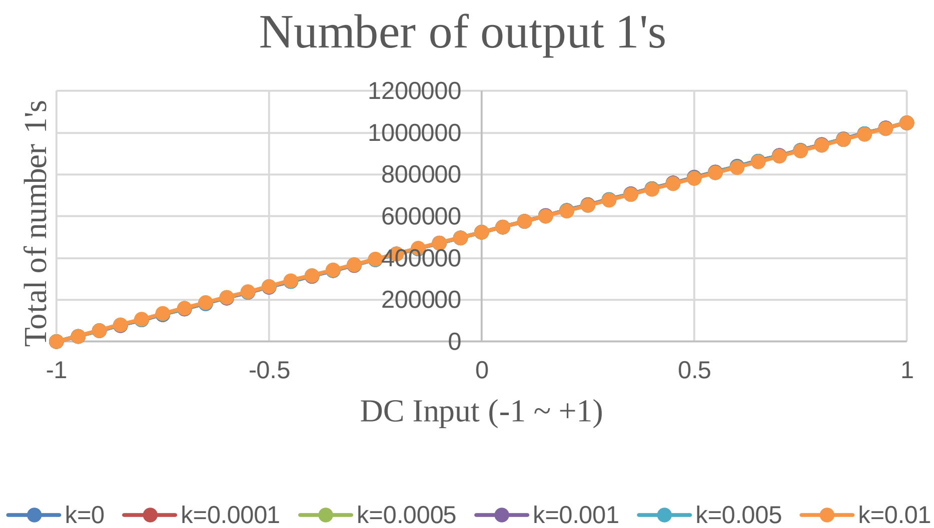
$$V_m = E - k * E^3 \ (k>0)$$



1st -order modulator

DC Input Simulation Result

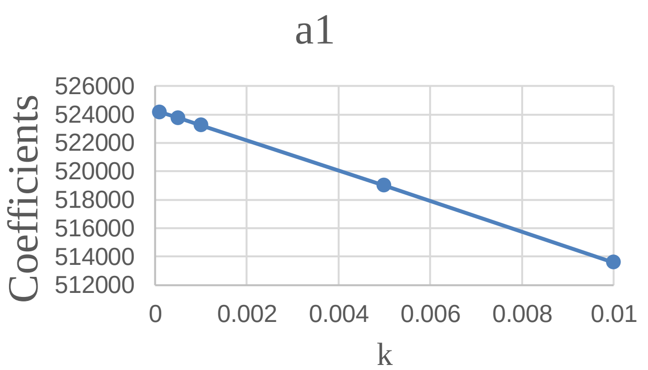
Number of modulator output: $N=2^{20}$

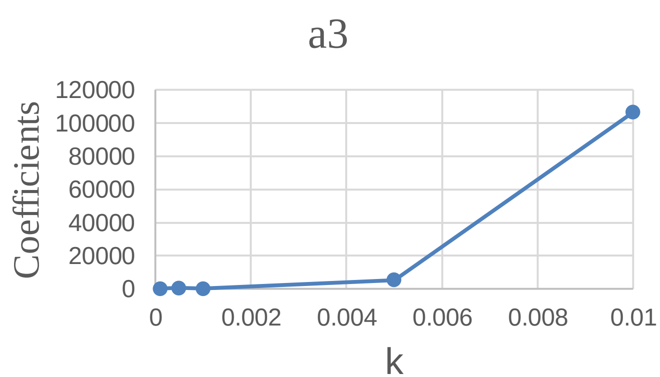


k	a_3	a_1
0.0001	104.84	524180
0.0005	524.48	523760
0.0010	1050.5	523240
0.0050	5282.5	519000
0.0100	10643.0	513610

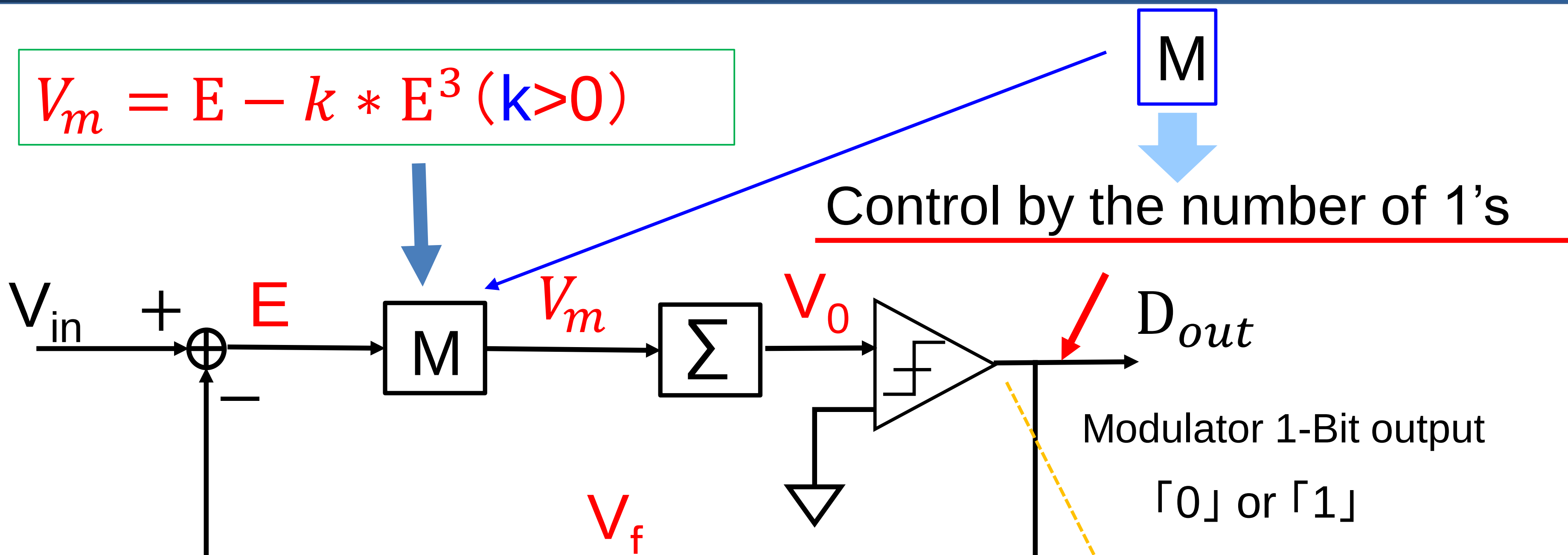
DC characteristic curve fitting

$$y = a_3 * x^3 + a_1 * x$$



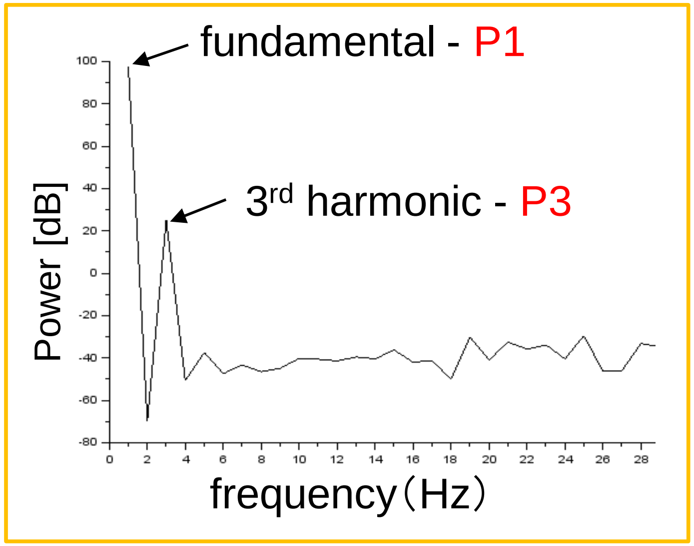


Cosine Input Simulation Configuration



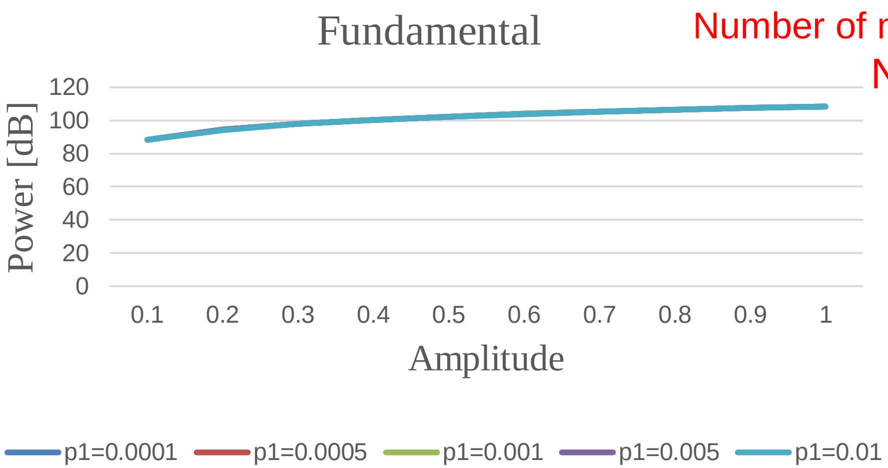
1st-order modulator

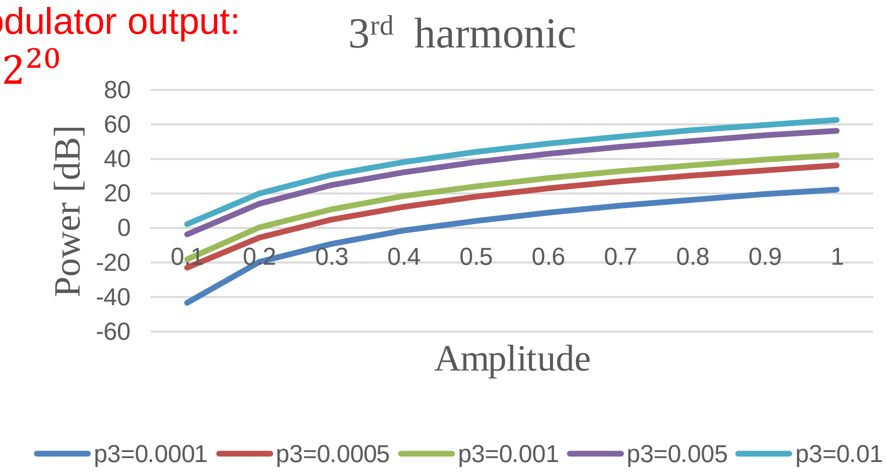
- Number of data : $N=2^{20}$
- V_{in} : $A\cos(\omega t)$ $(A = 0.1\sim1)$
- k=0.0001, 0.0005, 0.001, 0.005, 0.01



Cosine Input Simulation Result

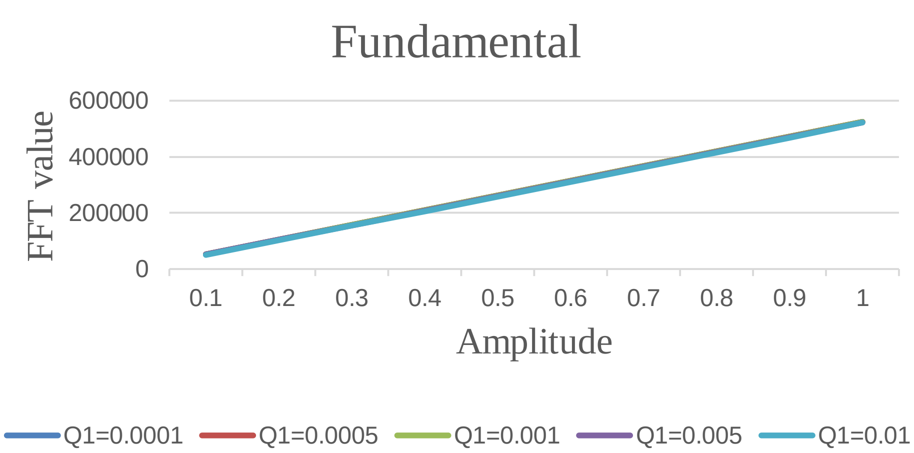
Number of modulator output: $N=2^{20}$

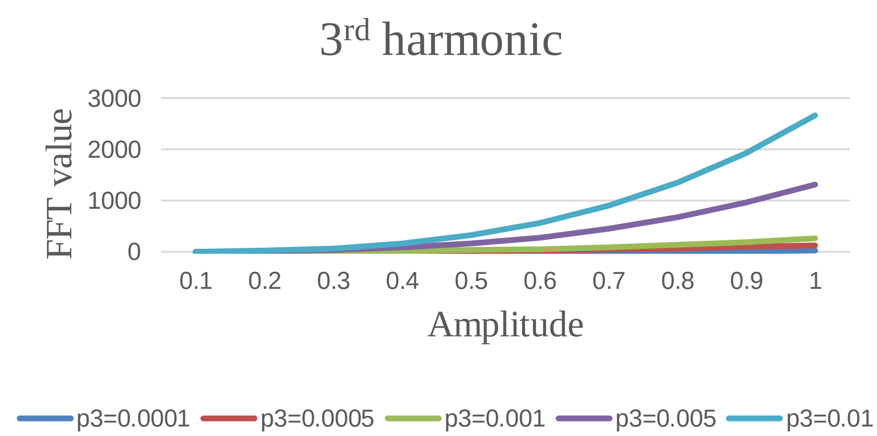




Power = $20\log(FFT_{value}) - 6.02$ [dB]

FFT result





Find Spectrum Power from DC Characteristics

- 1^{st} - order modulator
- Number of 1-bit output data： $N=2^{20}$

By nonlinearity

Fundamental： $a_1 A + \frac{3}{4} a_3 A^3$

3^{rd} harmonic： $\frac{1}{4} a_3 A^3$

A：amplitude

k	a_3	a_1
0.0001	104.84	524180
0.0005	524.48	523760
0.0010	1050.5	523240
0.0050	5282.5	519000
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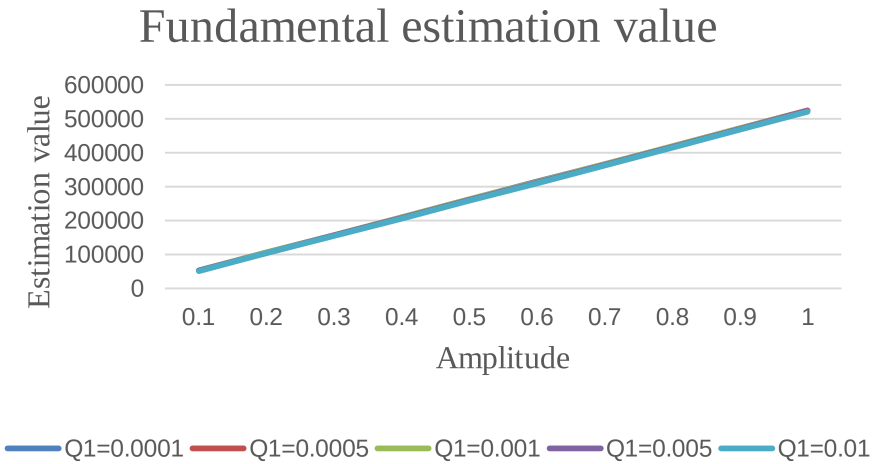
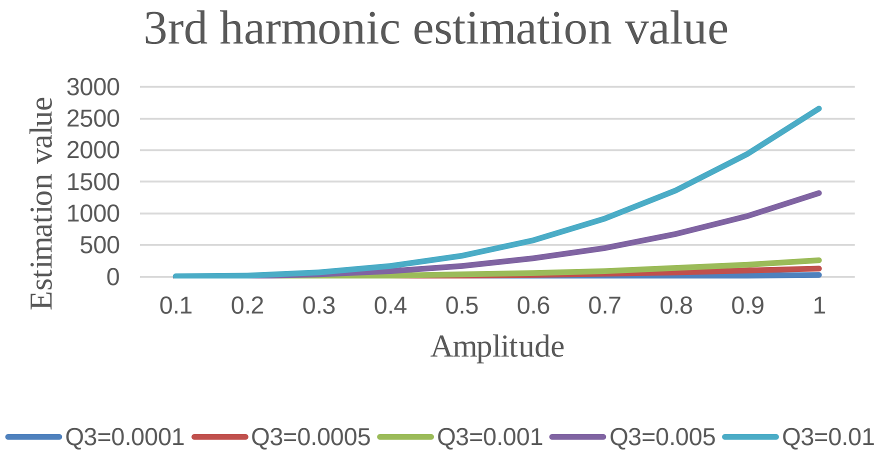
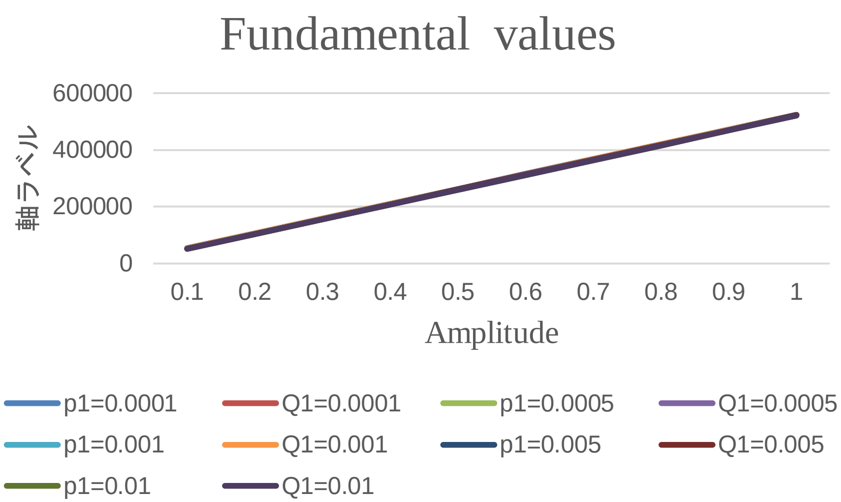
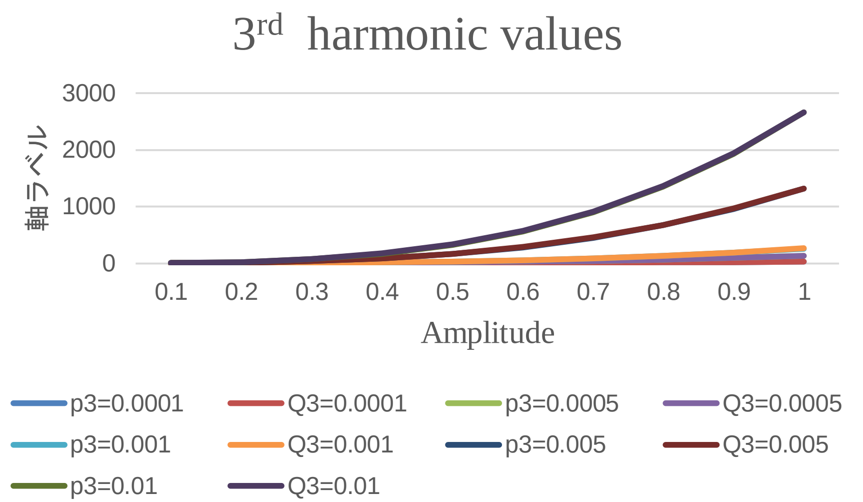




$N=2^{20}$

Comparison Between Estimated and FFT Values

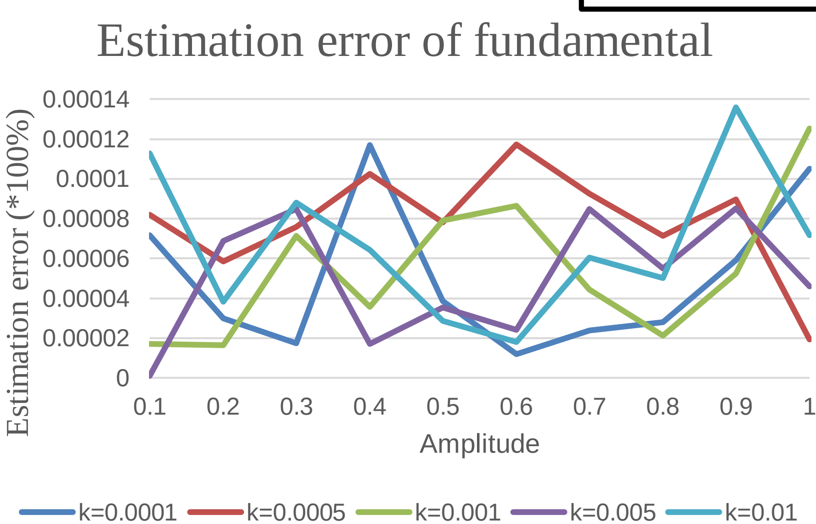


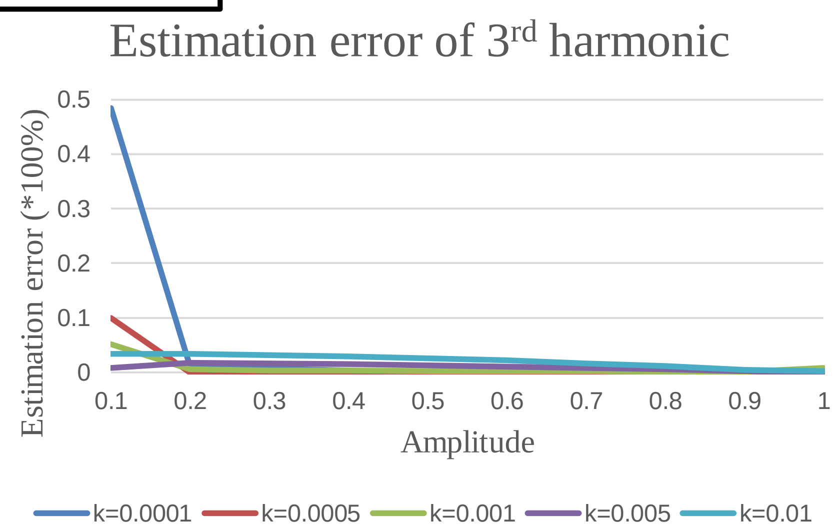


P_1 : fundamental obtained by FFT
Q_1 : estimated fundamental

$$\text{Error} = \frac{Q_{\text{values}} - P_{\text{values}}}{Q_{\text{values}}}$$

P_3 : 3rd harmonic obtained by FFT
Q_3 : estimated 3rd harmonic

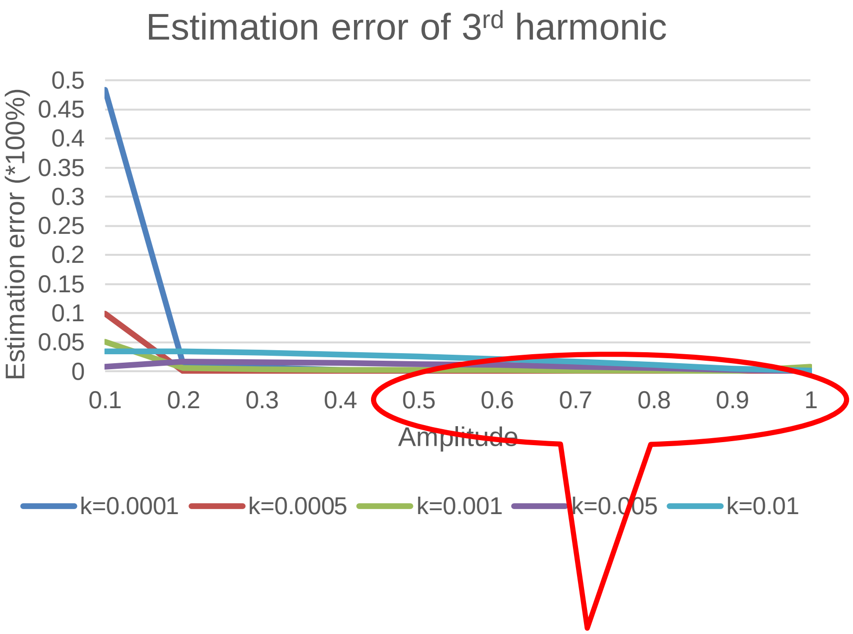


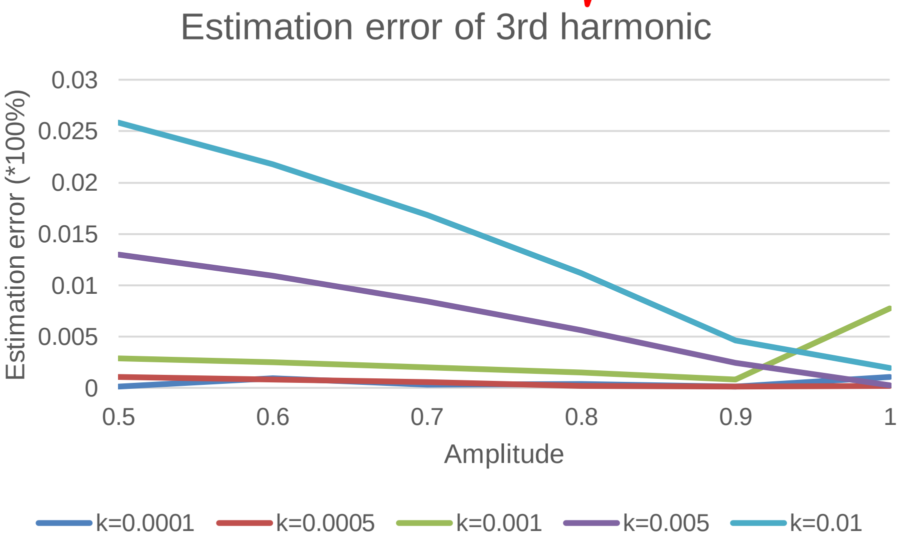


$N=2^{20}$

Accurate Estimation Condition for 3rd Harmonic

1st -order modulator





Good condition

3rd harmonic

Amplitude = 0.9

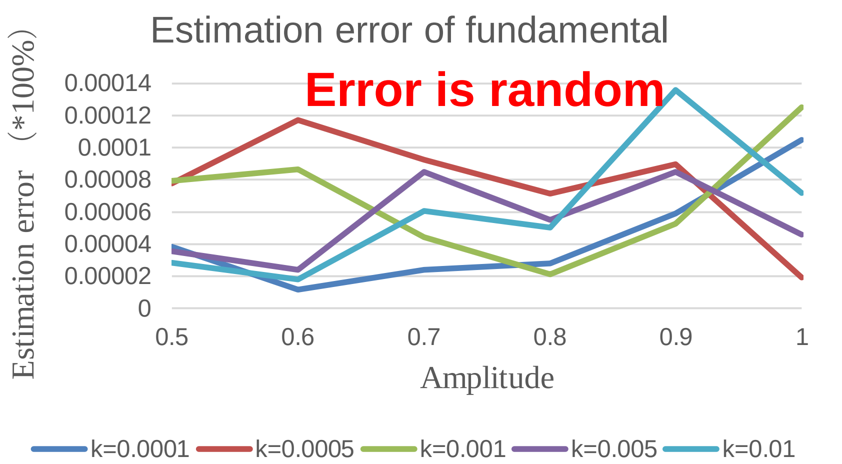
Error = 0.0123%

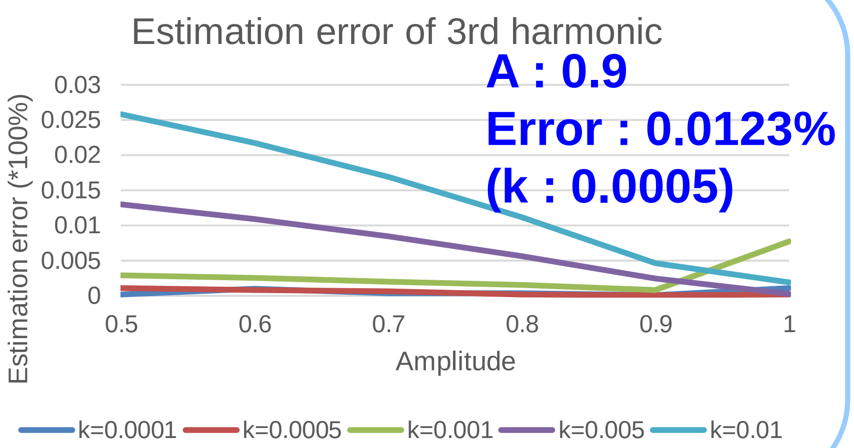
(k = 0.0005)

N=2^{20}

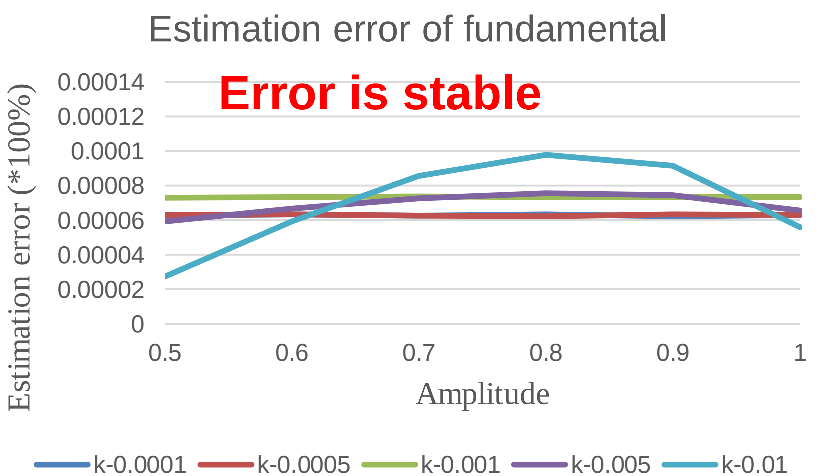
Comparison of 1st and 2nd -order Modulators

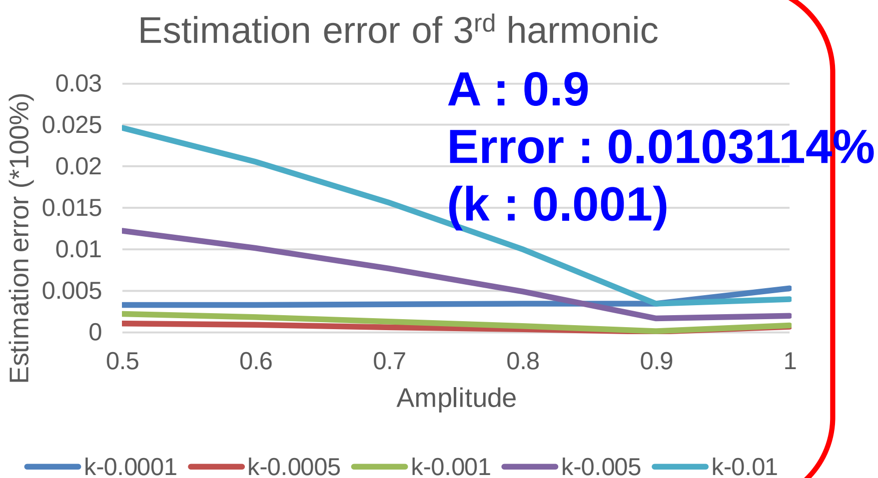
1st -order modulator





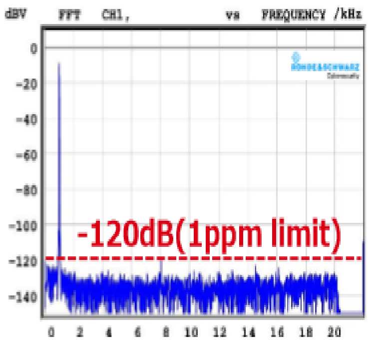
2nd -order modulator





DUT Measurement Result

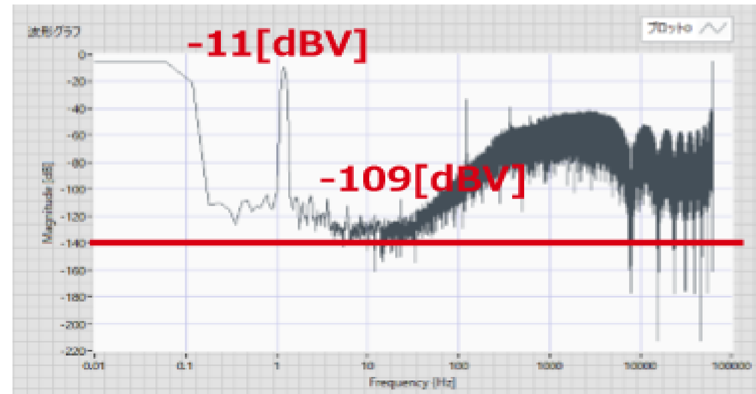
➢ **Measurements results from Rohm semiconductor company**



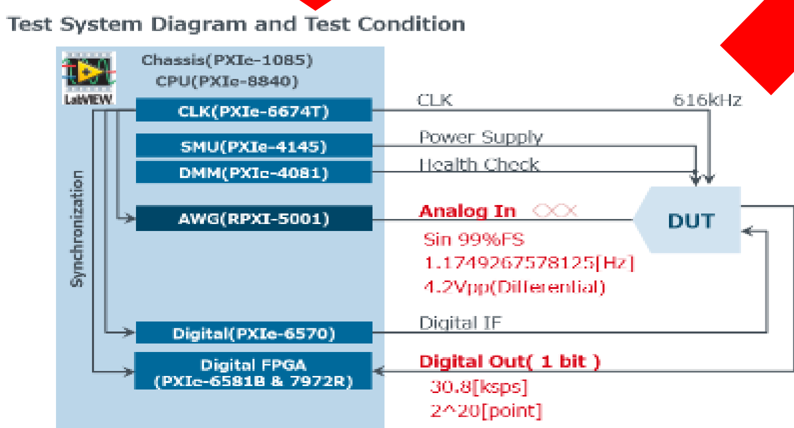
Output : 1kHz 44.1ksps
THD : 122dB(~Fifth Harmonics)
SN : 132dB(Filter:20kHzLPF)

Meet the requirements

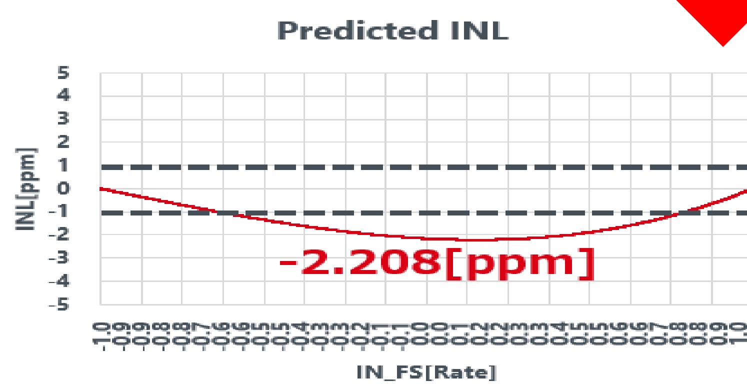
Signal from our developed AWG
(AWG: Arbitrary Waveform Generator)



Experimental result of
the modulator output FFT



Use of NI PXI system
for experiment



Obtained INL prediction
with the proposed method

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Conclusion

- High resolution, low speed ΔΣ ADC linearity short time testing algorithm

✓ Polynomial modeling of modulator input / output characteristics
✓ FFT of modulator 1-bit output stream for cosine input
✓ Estimate polynomial coefficients from fundamental and harmonic powers

- Verified by simulation and experiments that the proposed method is feasible.

Drastic testing time reduction:
104days → 32 seconds

Future Work

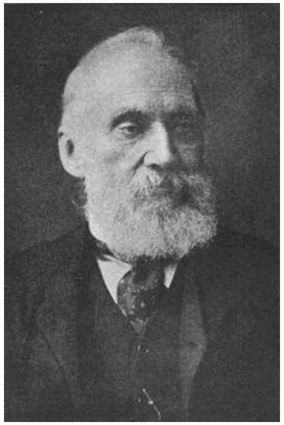
Consideration of the followings:

- Higher-order distortions
  - ⇨ High-order polynomial modeling
- Application to high-order modulators
- Application to multi-bit modulators

Final Statement

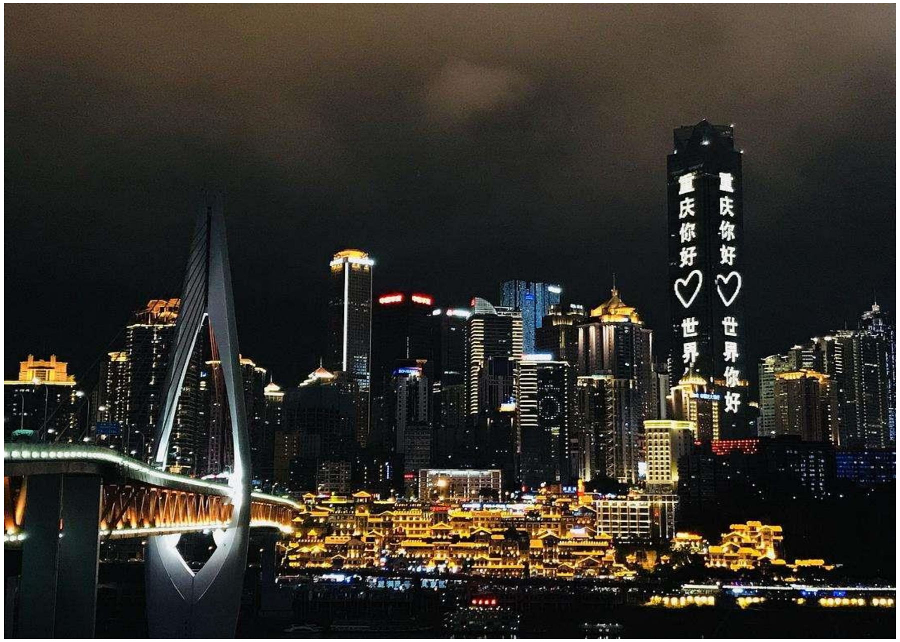
No Science without Measurement

No Production without Testing



Lord Kelvin

Thanks for listening!



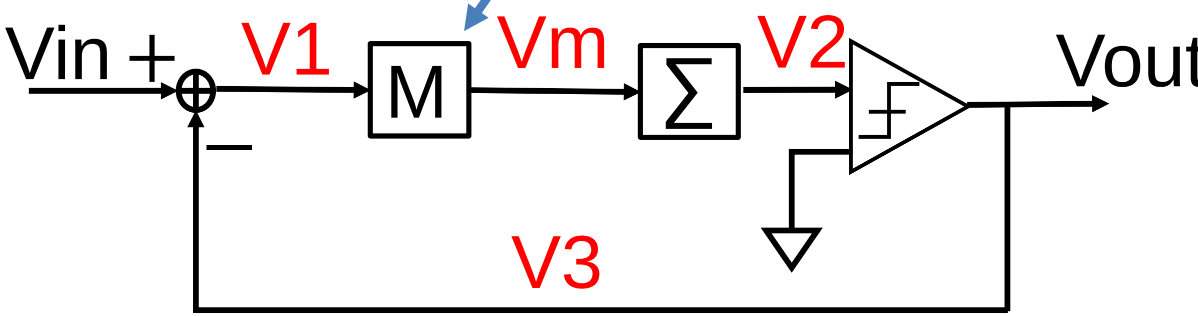
Appendix

DC Input Amplitude

First order modulator :
Input: DC = 1
Sampling: 16Bit

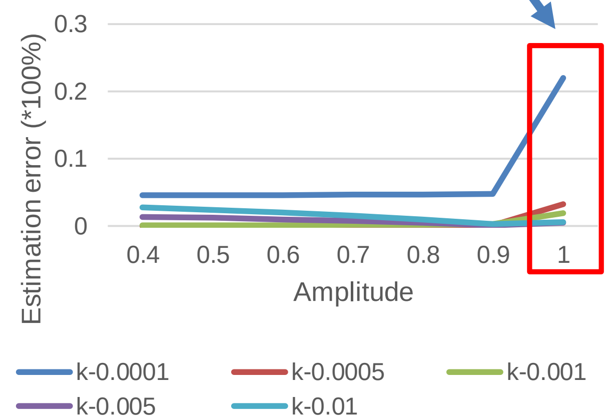
Vm=V1-k*V1^3 （k>0）

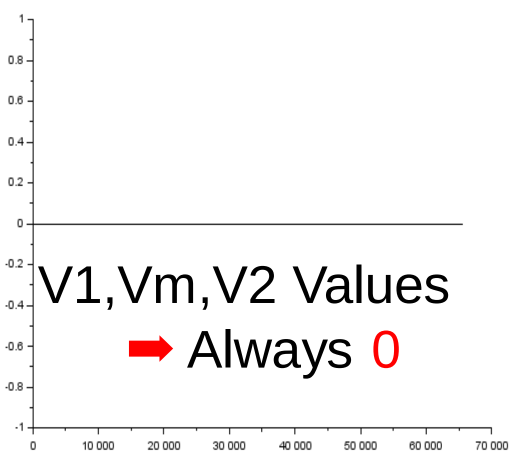
Nonlinearity Model



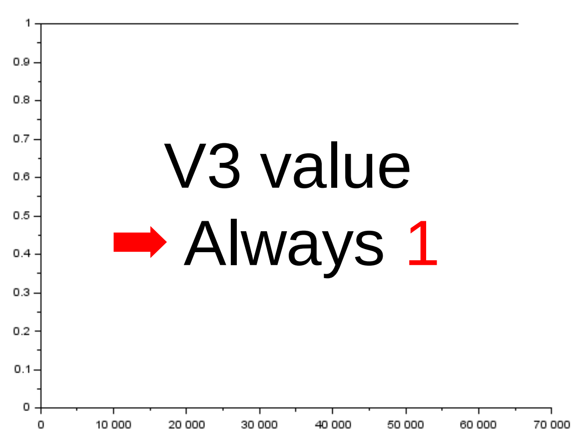
V1(i)=Vin(i)-V3（i）
Vm(i)=V1(i)-k*V1(i)^3 (K>0)
V2(i)=V2(i-1)+Vm(i)

If A=1
Estimation error
become bigger





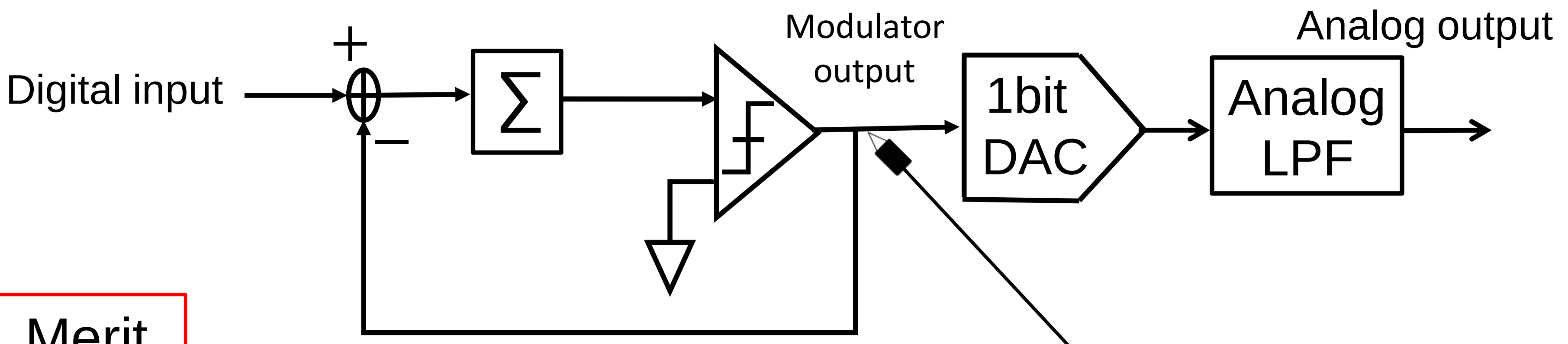
V1,Vm,V2 Values
➡ Always 0

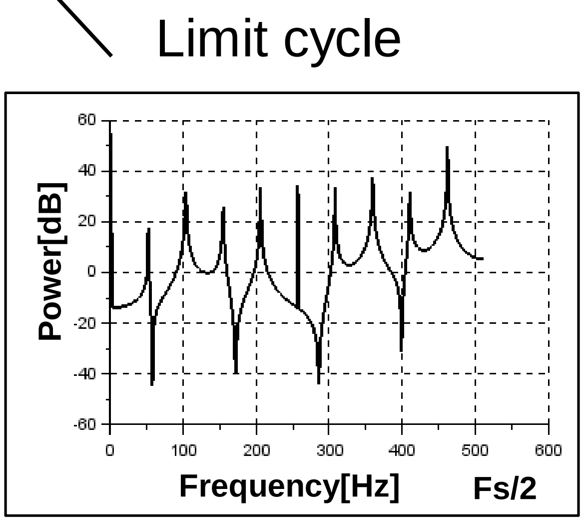


V3 value
➡ Always 1

So, A=1.
➡ It can't be modulator.

Merits & Demerits of ΔΣ DAC





Merit

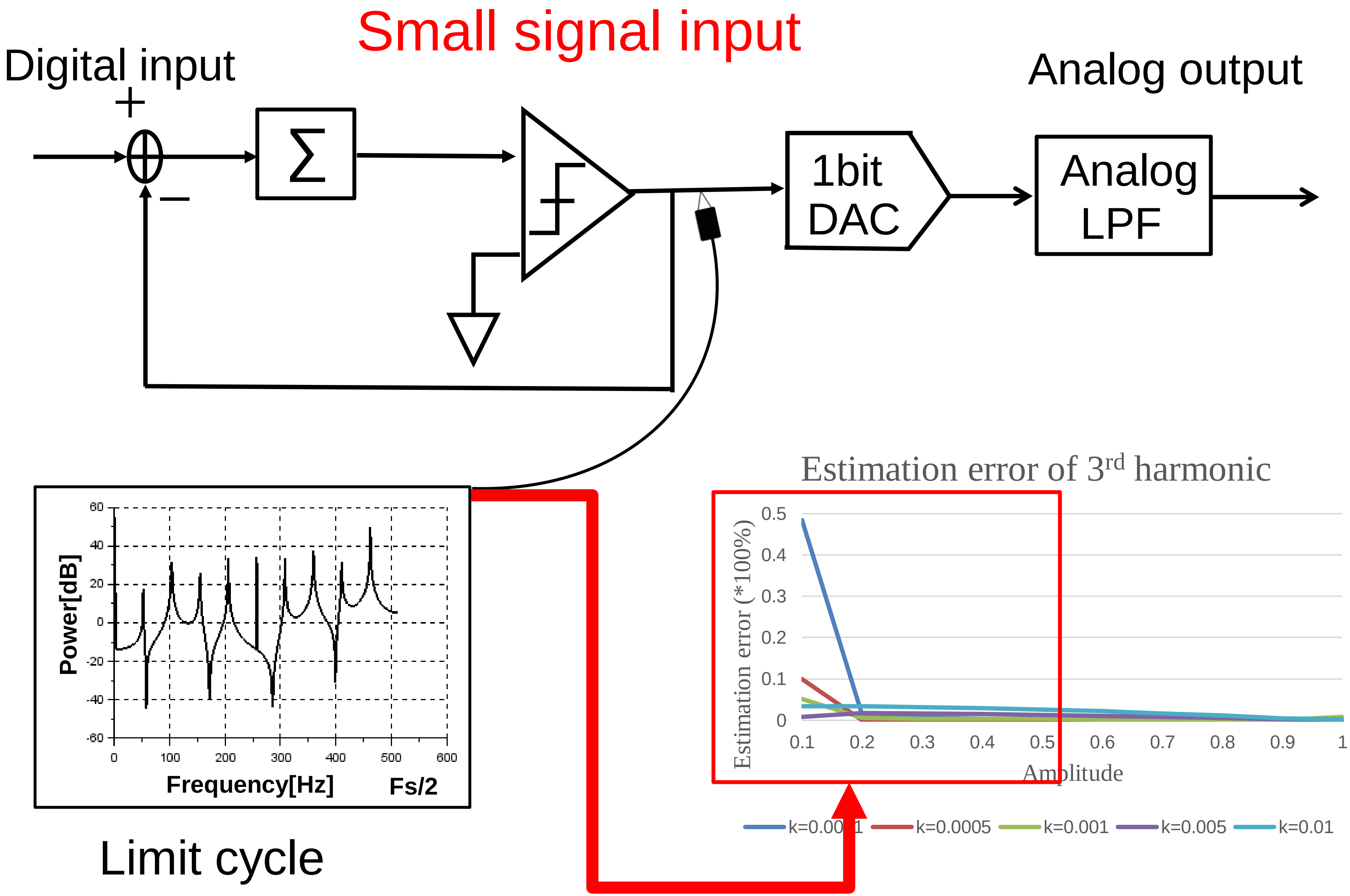
- Mostly digital circuit
- High linear & high resolution for low frequency signal generation

Demerit

- Limit cycle problem for small input

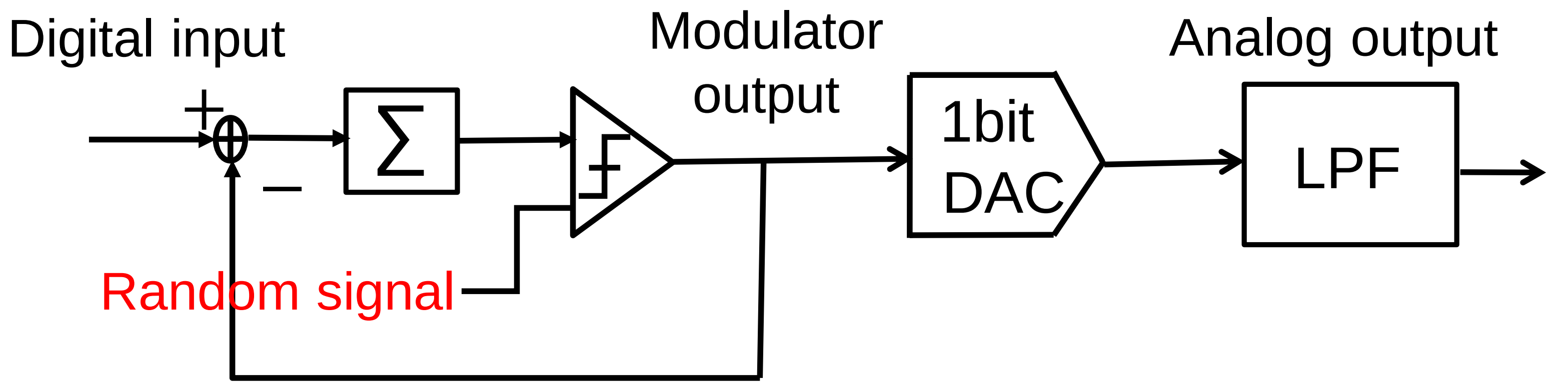
※ Due to modulator nonlinearity by quantizer

DC small signal input



Limit cycle

Limit cycle solution



< Features >

① NOT sacrifice input range

② NOT affect signal band, thanks to noise-shaping

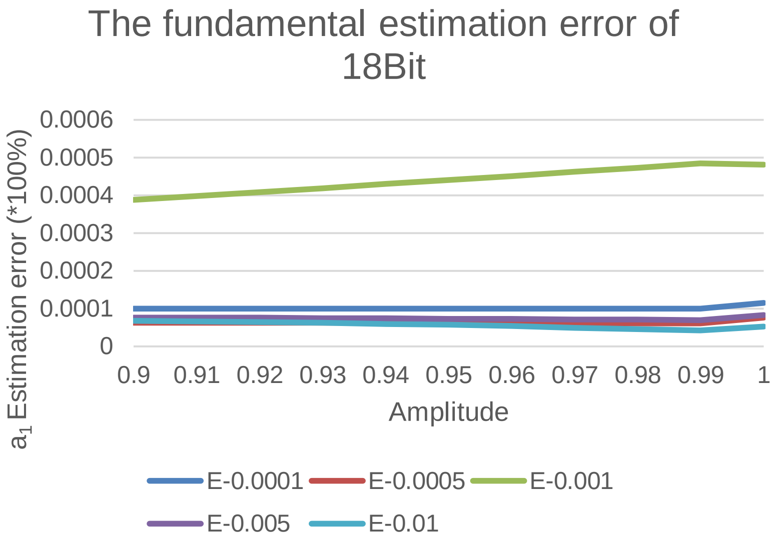
③ Easily generate random signal.

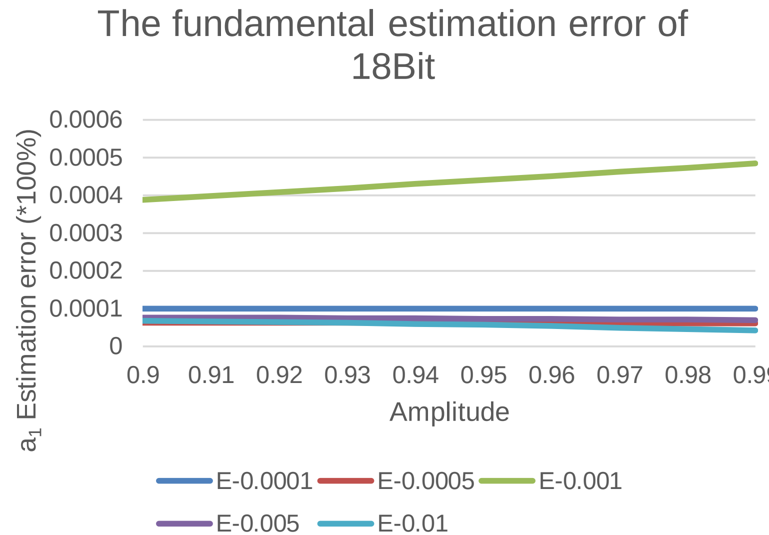
I published at ICSICT in 2018
https://ieeexplore.ieee.org/document/8564958

First-order modulator (3rd nonlinearity)

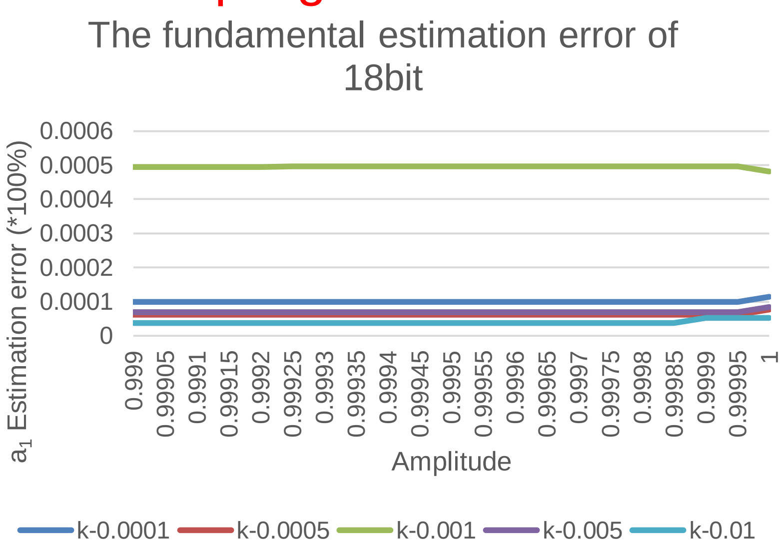
fundamental

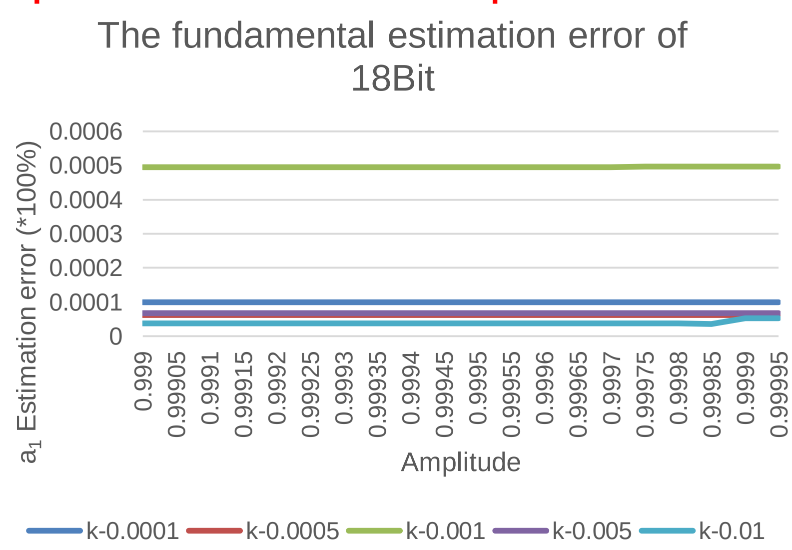
Sampling:18Bit　A : 0.9 ~ 1　amplitude increase step：0.01





Sampling:18Bit　A : 0.999 ~ 1　amplitude increase step：0.0005



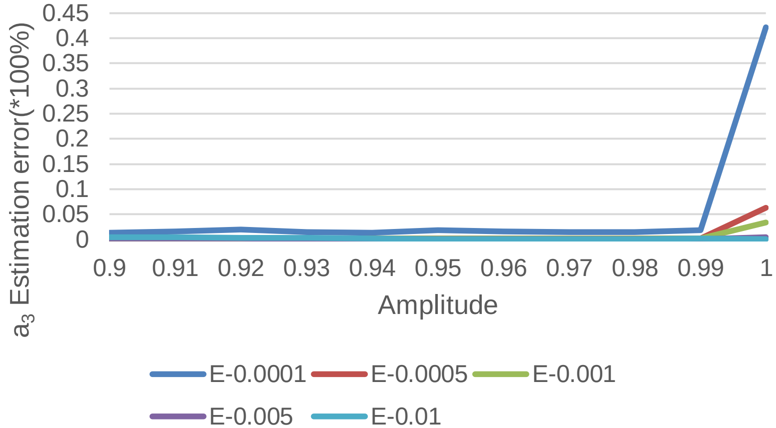


First-order modulator (3rd nonlinearity)

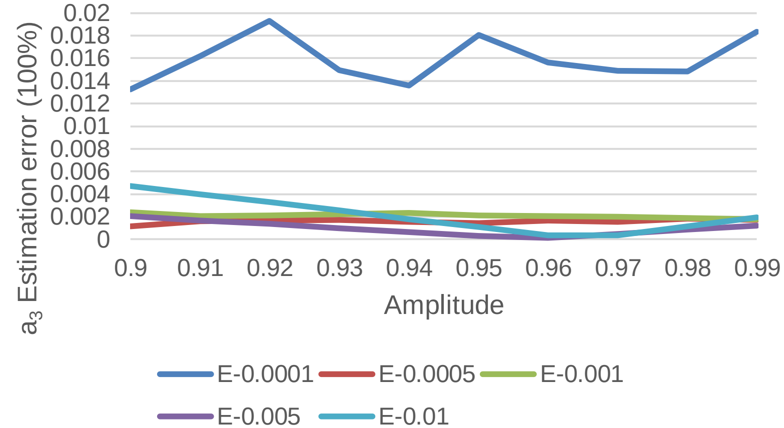
3rd harmonic

Sampling:18Bit A : 0.9 ~ 1 amplitude increase step : 0.01

The 3rd harmonics estimation error of 18Bit

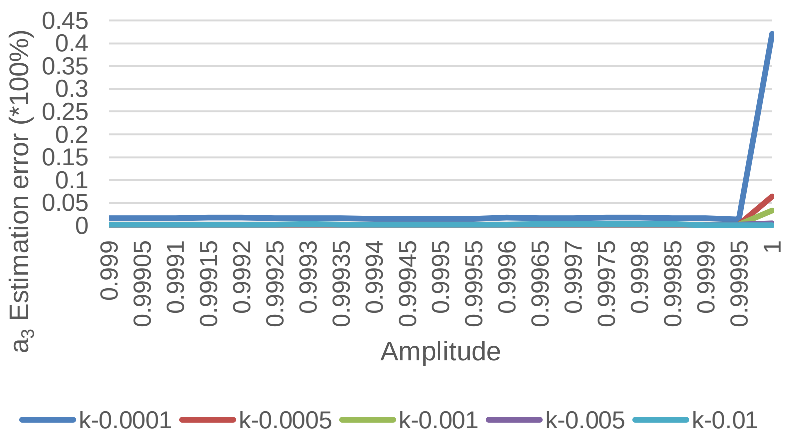


The 3rd harmonics estimation error of 18Bit

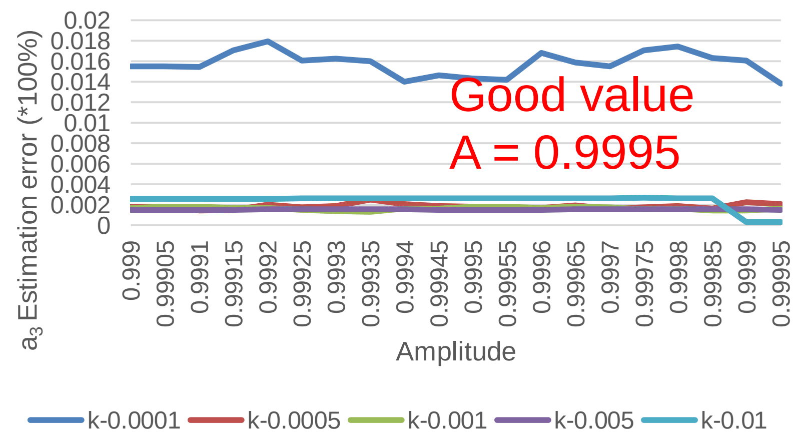


Sampling:18Bit A : 0.999 ~ 1 amplitude increase step : 0.0005

The 3rd harmonic estimation error of 18Bit



The 3rd harmonics estimation error of 18Bit



3rd harmonic

First-order modulator