C3-1 10:15-10:45
Oct. 31, 2019 (Thu)

Invited

Fine Time Resolution TDC Architectures -Integral and Delta-Sigma Types

Haruo Kobayashi, Kosuke Machida, Yuto Sasaki, Yusuke Osawa
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Gunma University

群馬大学
GUNMA UNIVERSITY

Outline

- Research Background
- Integral-type TDC
  - Time Hold Circuit
  - Equivalent-Time Sampling
  - Integral TDC
  - Vernier Frequency TDC
- Delta-Sigma TDC
  for Phase Noise Measurement
- Conclusion

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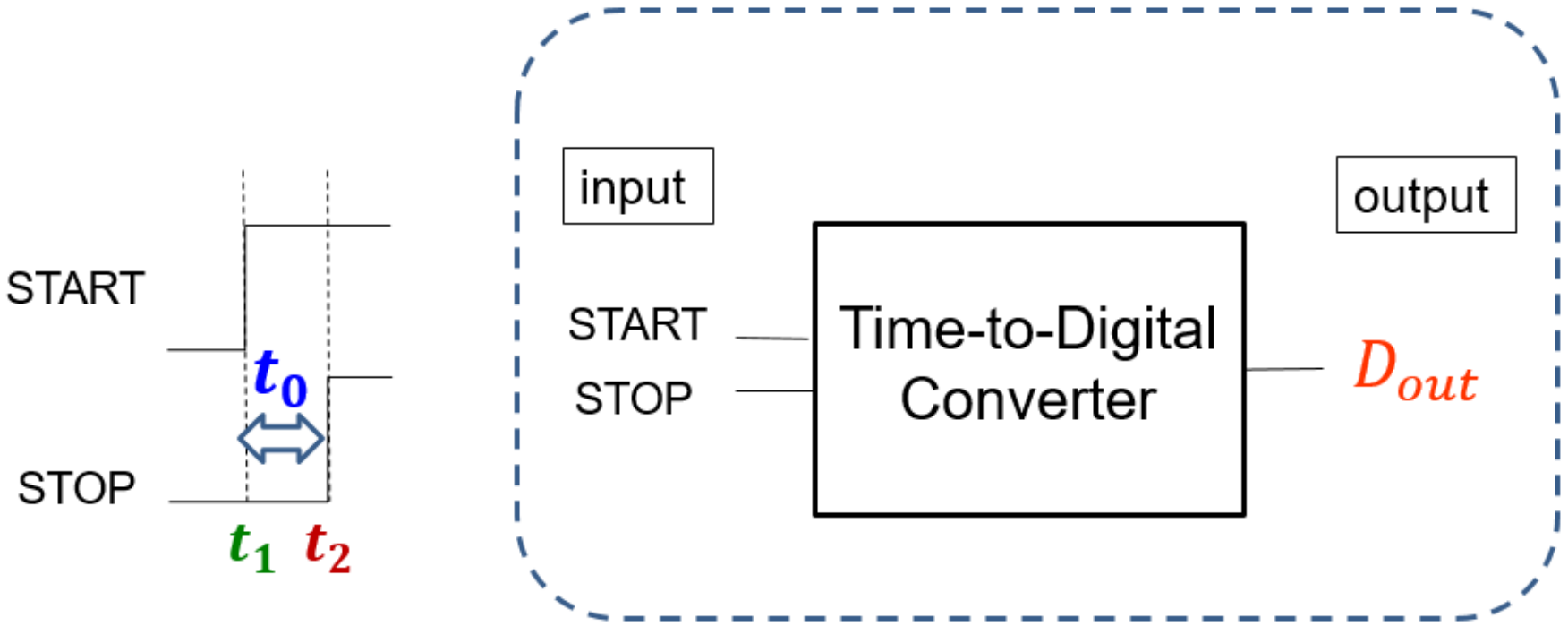
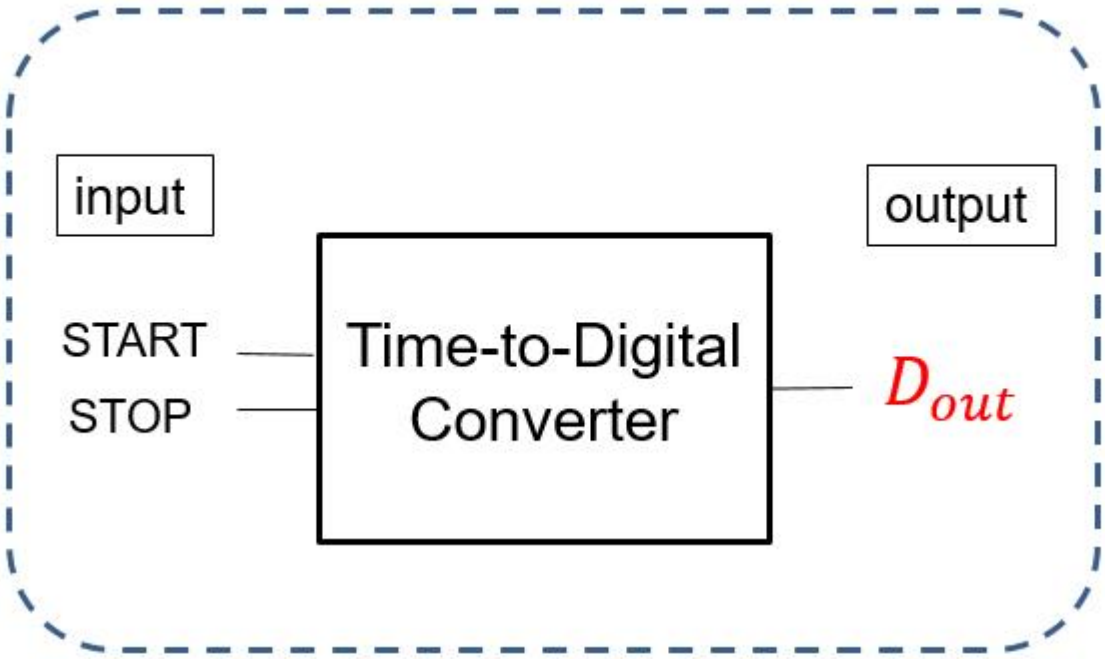
Time-to-Digital Converter

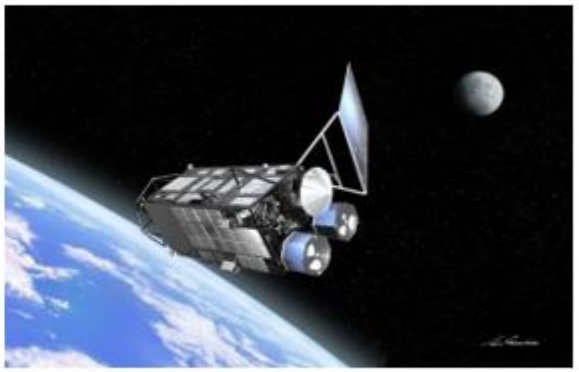


- Time-to-digital converter (TDC) measures **timing difference** t_0 between t_1 , t_2 as a **digital value** D_{out}

TDC Application Examples



Inter-vehicular distance measurement



Satellite distance measurement

Target TDC Architectures

TDC architectures have been inspired by ADC architectures

Flash TDC	⟺	Flash ADC
SAR TDC	⟺	SAR ADC
Integral-type TDC	⟺	Integral-type ADC
ΔΣ TDC	⟺	ΔΣ ADC

⬇

Slow but very fine time resolution

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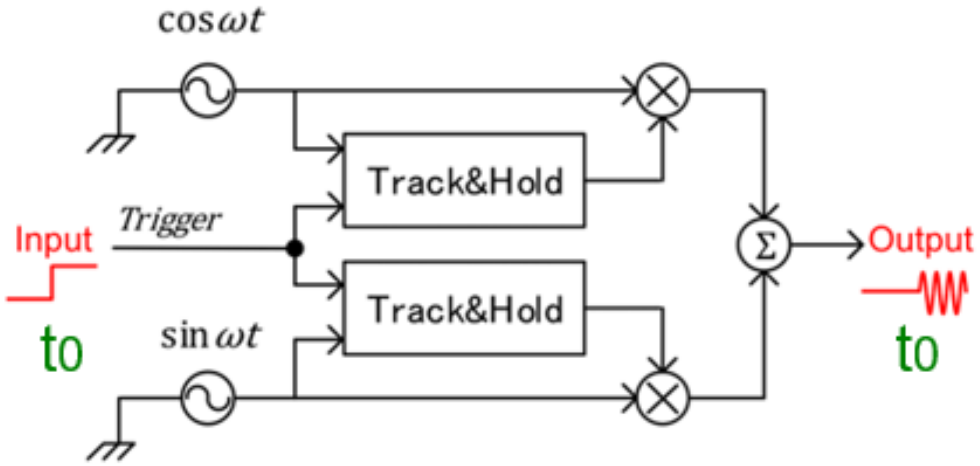
  - Equivalent-Time Sampling
  - Integral TDC

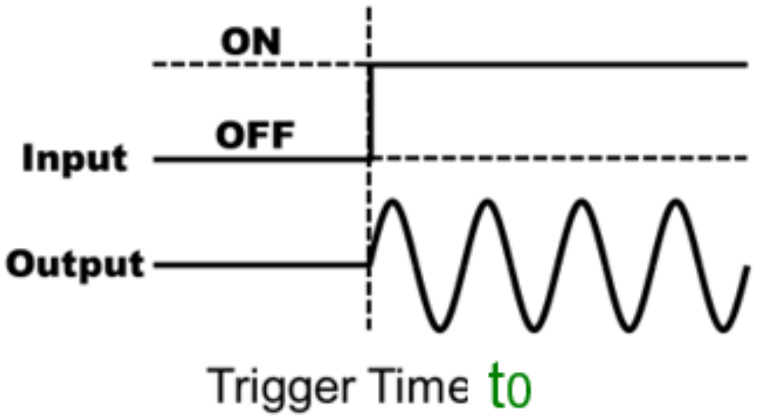
Myth : Time cannot be held.

Truth: It can be held.

Y. Ozawa, T. Ida, S. Sakurai, R. Jiang, R. Takahashi, H. Kobayashi, R. Shiota
”SAR TDC Architecture for One-shot Timing Measurement,”
IEEE International Symposium on Intelligent Signal Processing and Communication Systems, Xiamen, China (Nov. 2017)

Trigger Circuit

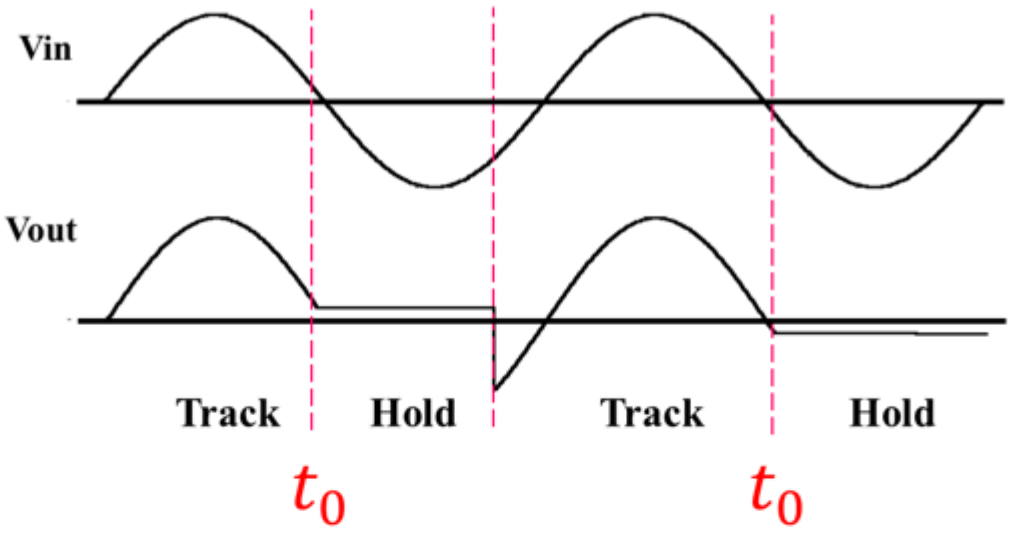


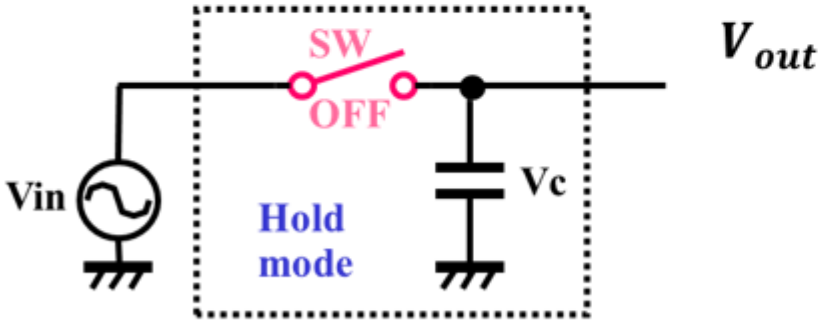


- Output starts to oscillate at rising timing edge of input

[1] M. Nelson (Tektronics)
"A New Technique for Low-Jitter Measurements Using Equivalent-Time Sampling Oscilloscope"
Automatic RF Techniques Group 56th Measurement (Dec. 2000)

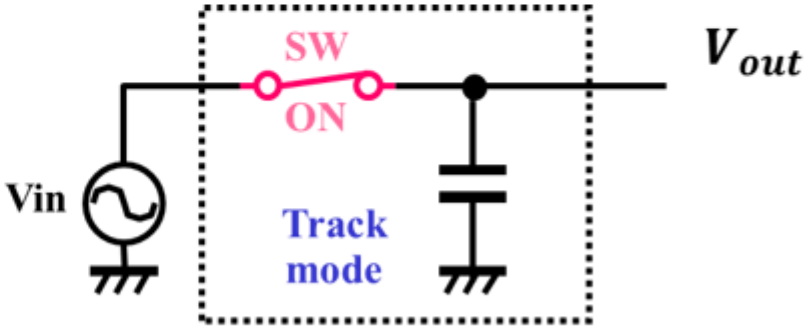
Track/Hold Circuit





T / H circuit

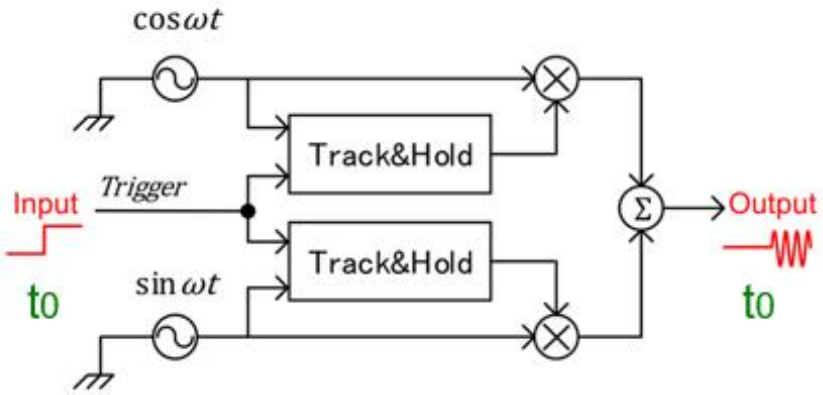
$V_C = V_{out}$

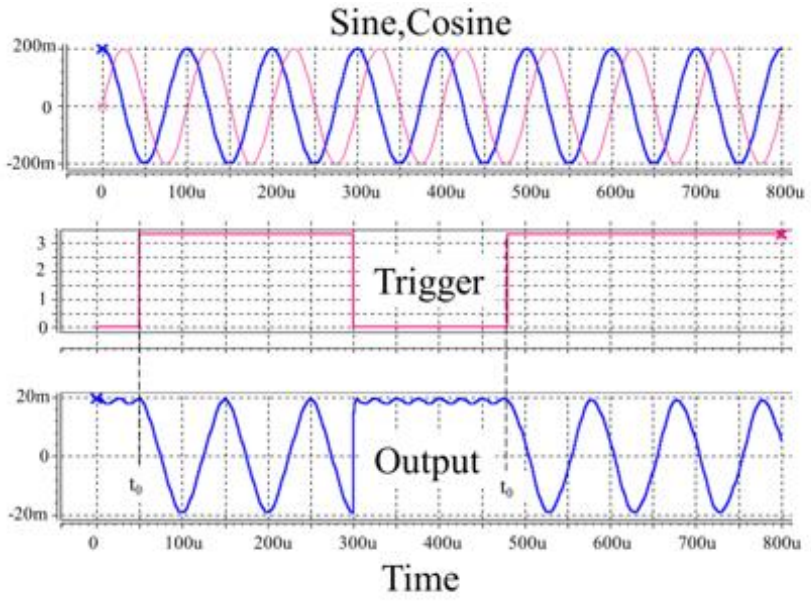


T / H circuit

$V_{in} = V_{out}$

Trigger Circuit Waveforms





T/H circuit

- **track mode**

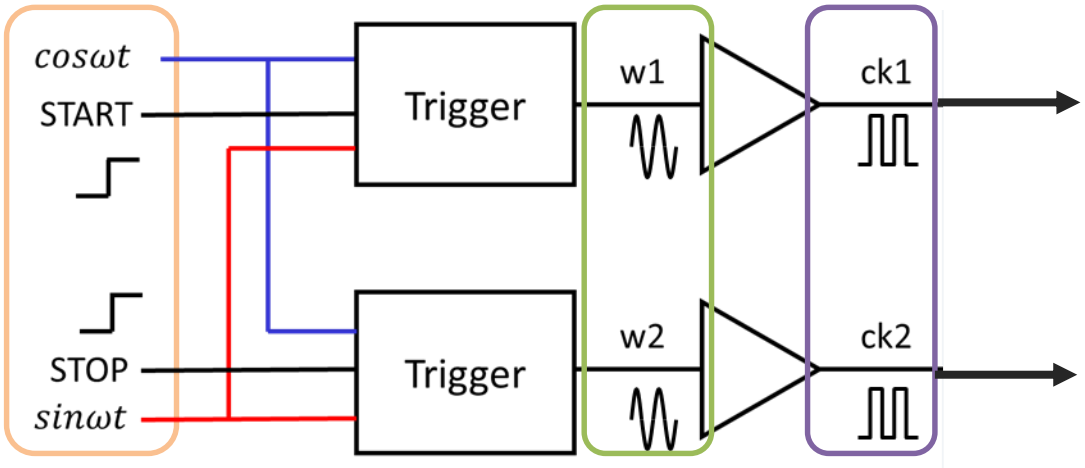
$$\text{Vout} = \cos(\omega t)\cos(\omega t) + \sin(\omega t)\sin(\omega t)$$
$$= \cos^2(\omega t) + \sin^2(\omega t)$$
$$= 1$$

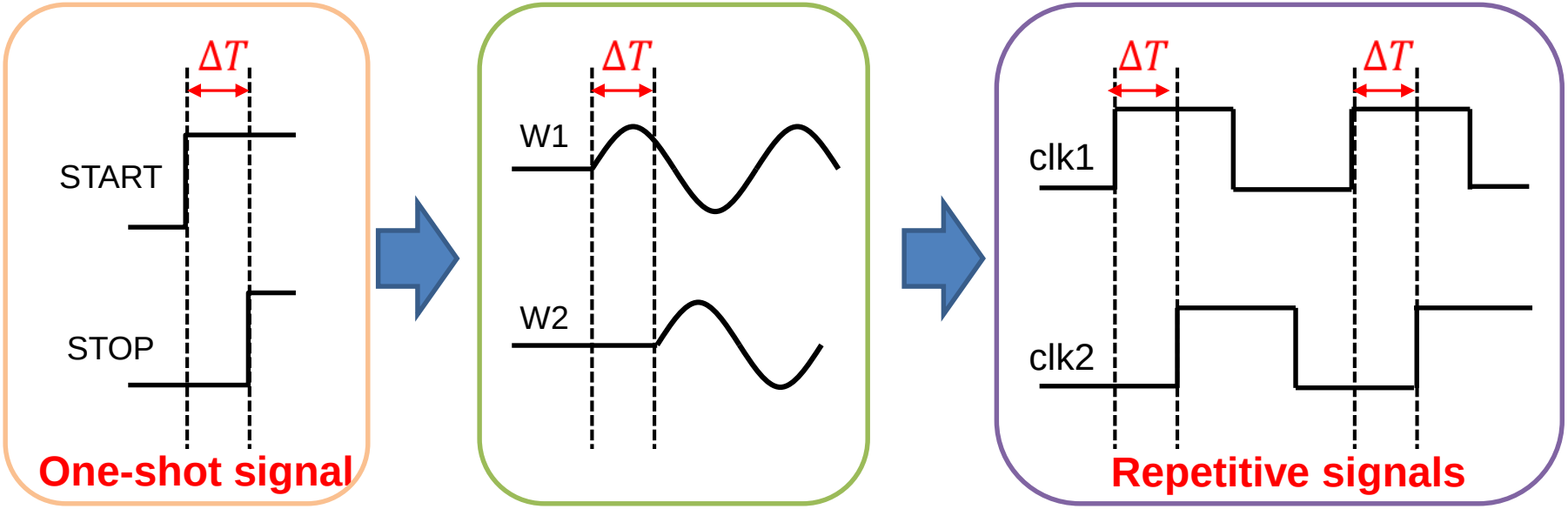
- **hold mode**

$$\text{Vout} = \cos(\omega t)\cos(\omega t_0) + \sin(\omega t)\sin(\omega t_0)$$
$$= \cos(\omega(t - t_0))$$

※ **trigger time:t_0**

Time difference can be held !





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  - Time Hold Circuit
  - Equivalent-Time Sampling
  - Integral TDC
  - Vernier Frequency TDC

Y. Sasaki, Y. Zhao, A. Kuwana, H. Kobayashi,
"Highly Efficient Waveform Acquisition Condition
in Equivalent-Time Sampling System"
27th IEEE Asian Test Symposium, Hefei, Anhui, China (Oct. 2018)

Equivalent-Time Sampling

In a sampling oscilloscope,
a repetitive high-frequency waveform can be sampled with low-frequency sampling clock and reconstructed.

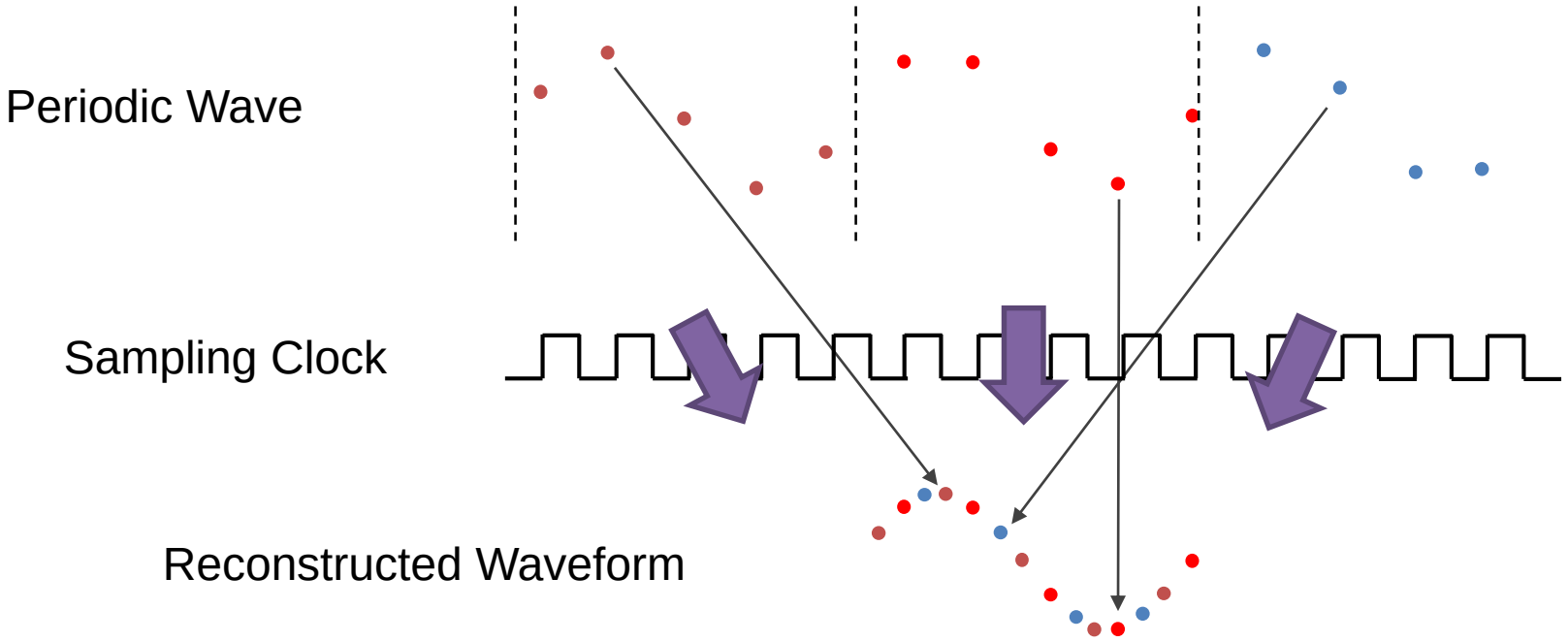
3 time-bases

① Coherent Sampling
   for periodic waveform

② Sequential Sampling
   for repetitive waveform, w/o pre-trigger function

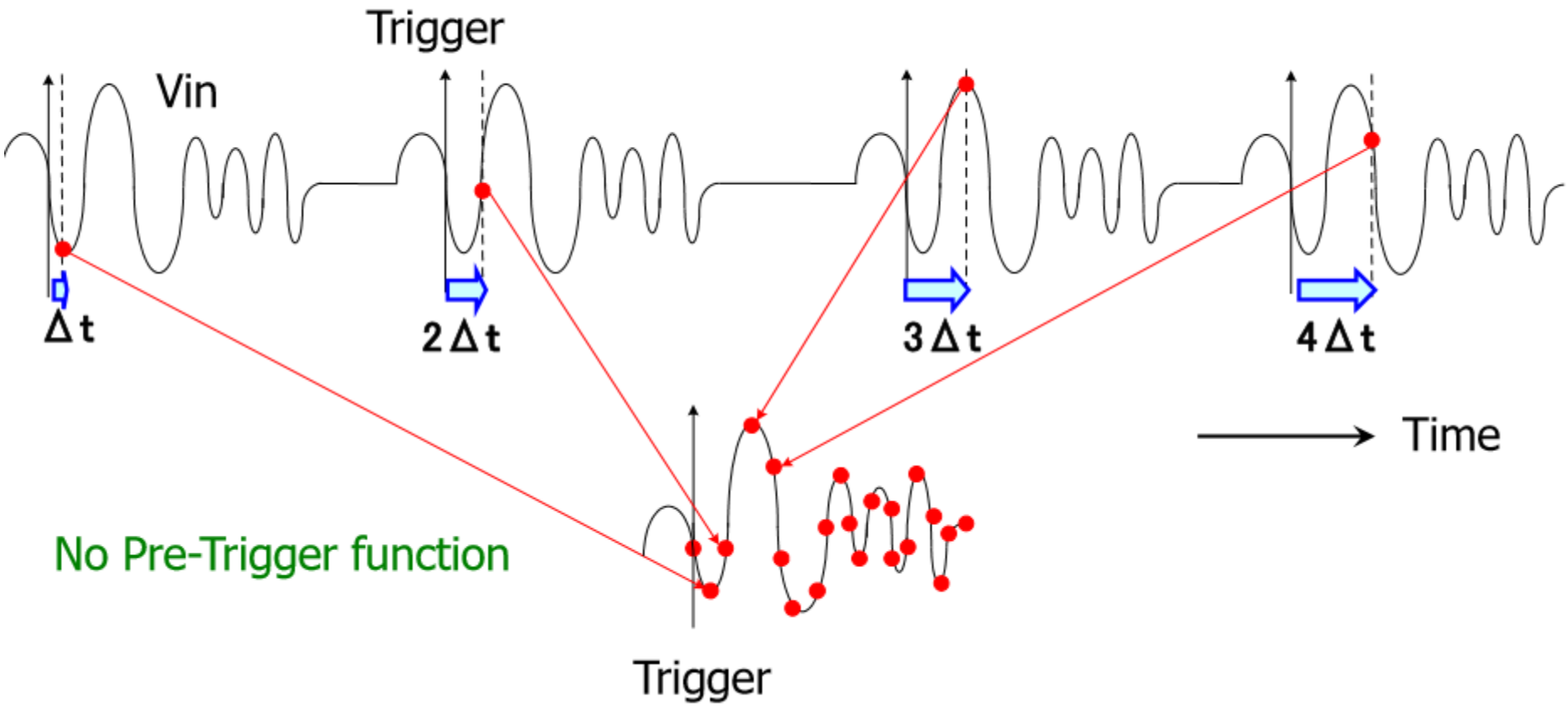
③ Random Sampling
   for repetitive waveform, w/ pre-trigger function

Coherent Sampling

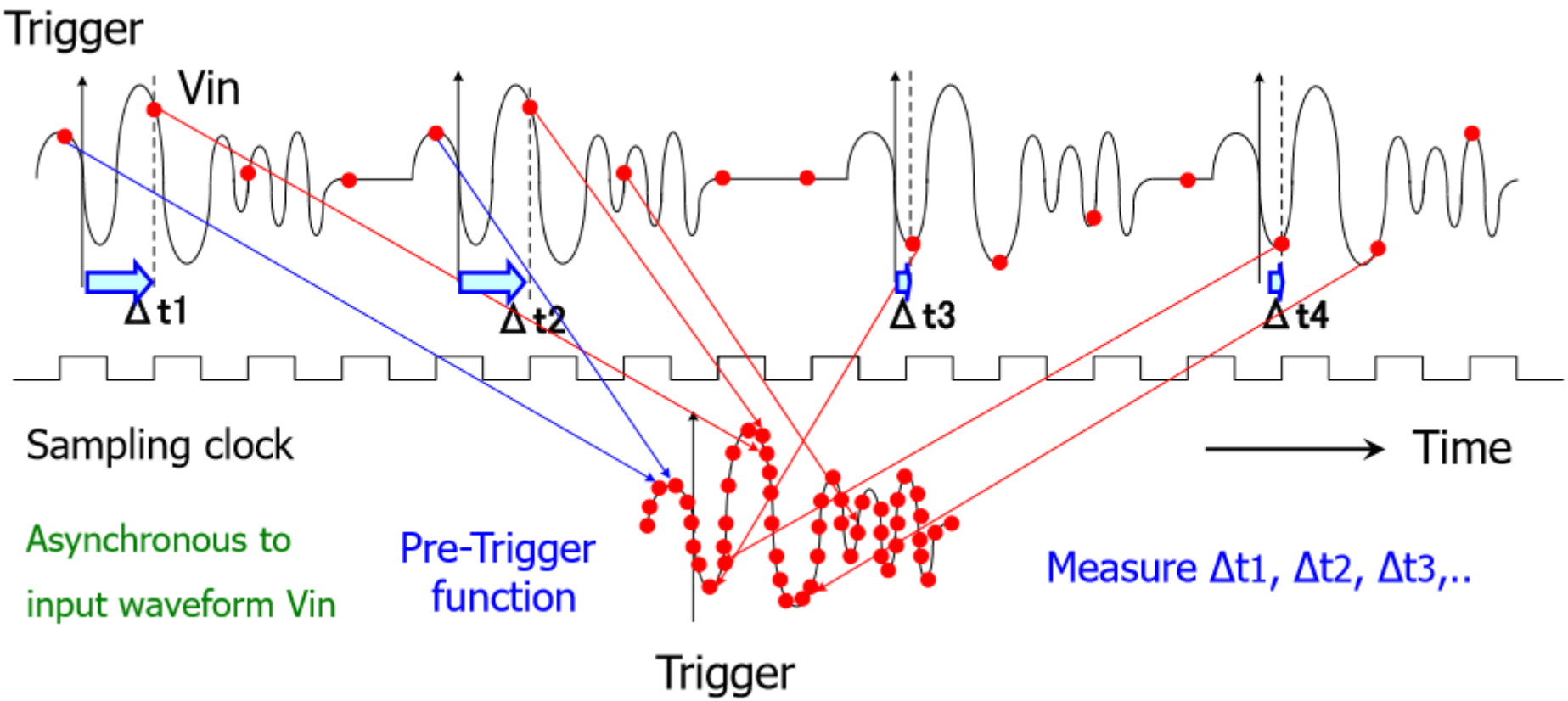


Finer time resolution than sampling clock period

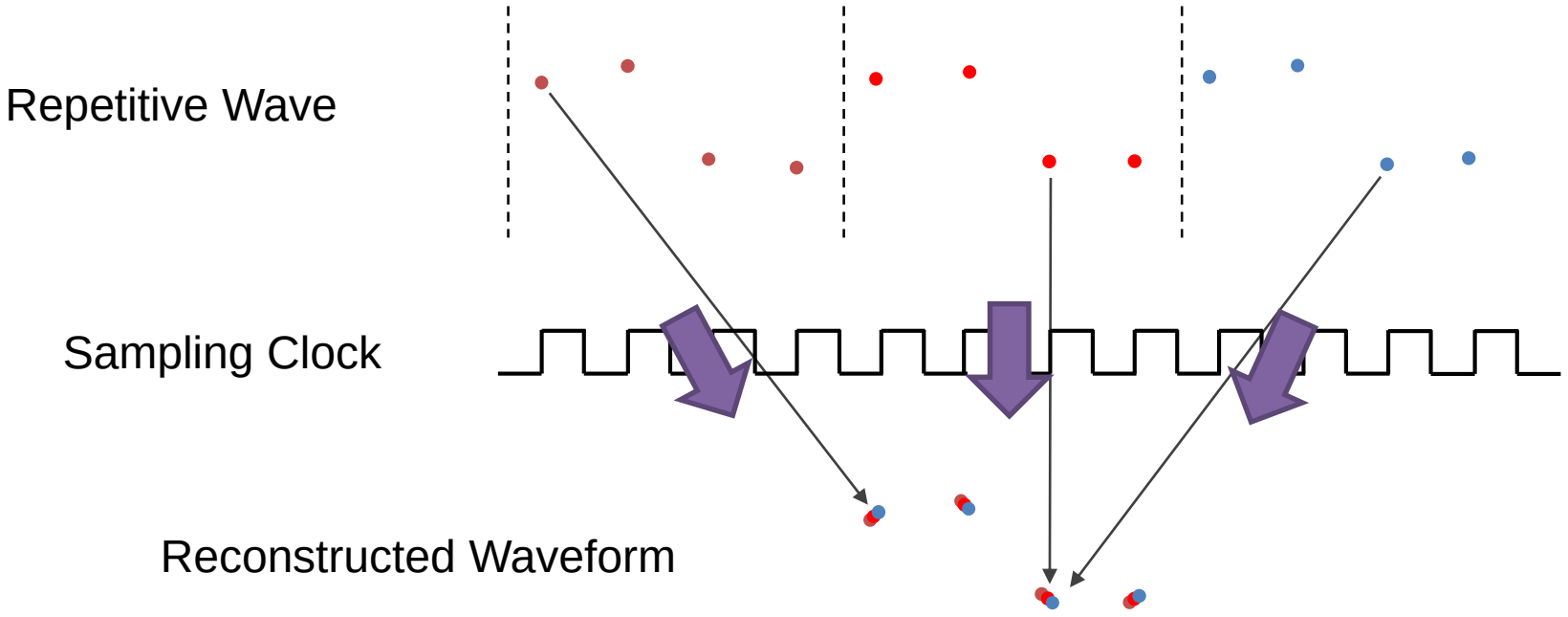
Sequential Sampling



Random Sampling

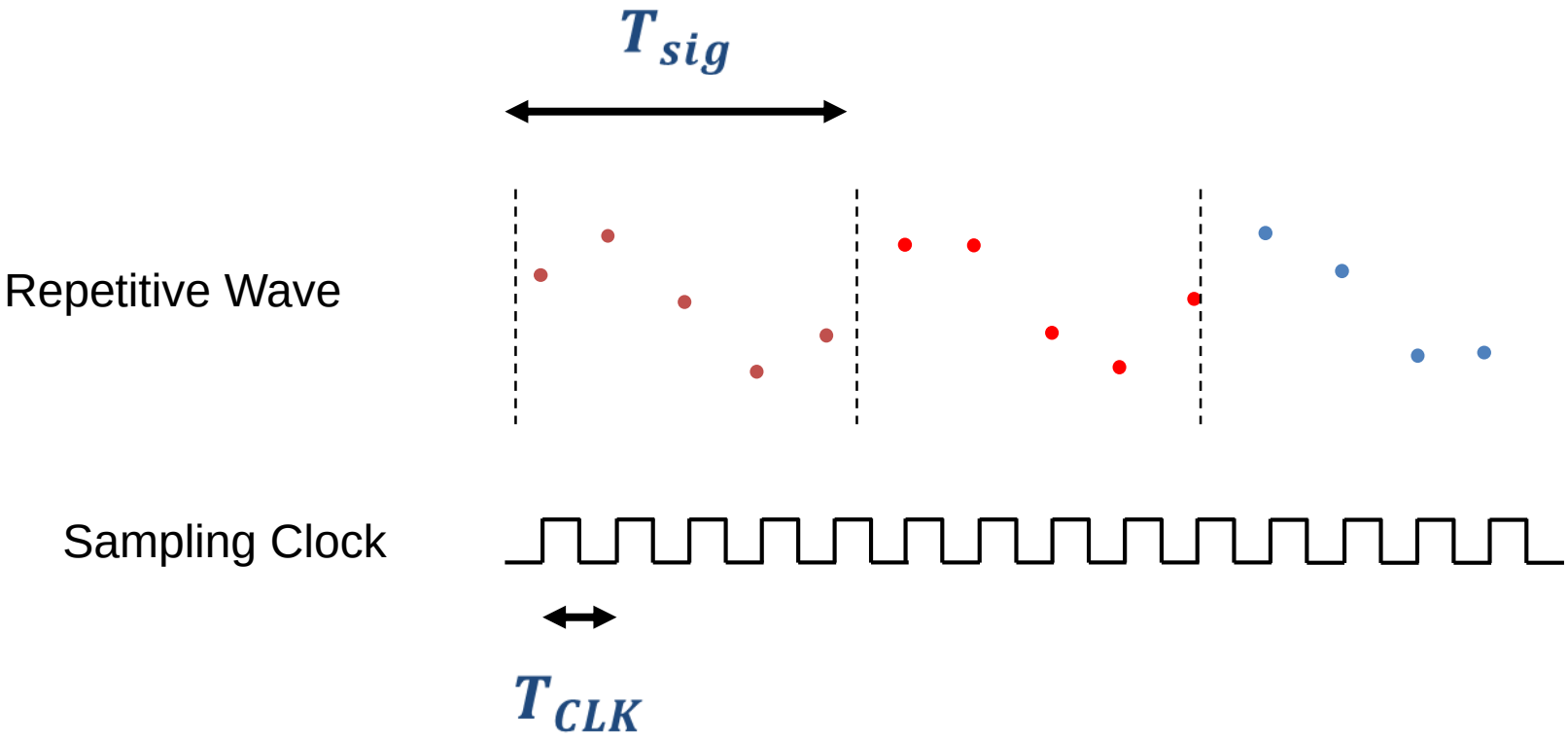


Waveform Missing Phenomena



Toothless waveform appears

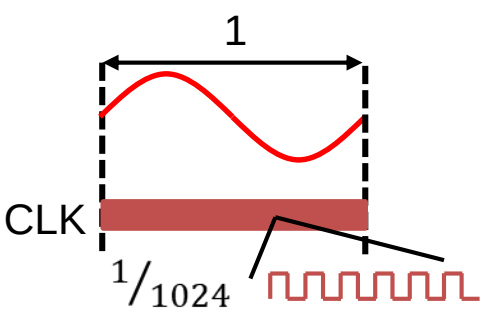
Waveform Sampling Condition

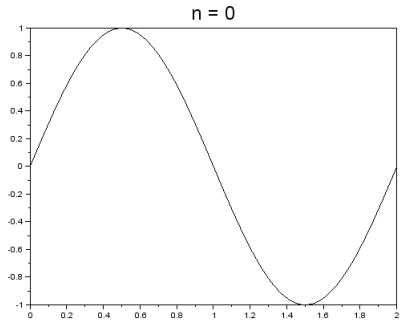


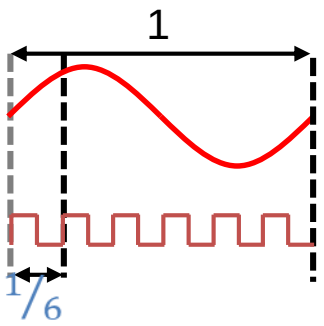
$$T_{CLK} = \ ? \ \times T_{sig}$$

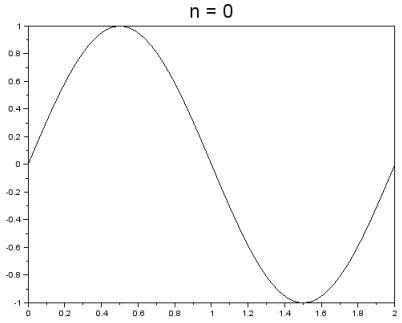
Waveform Missing Conditions

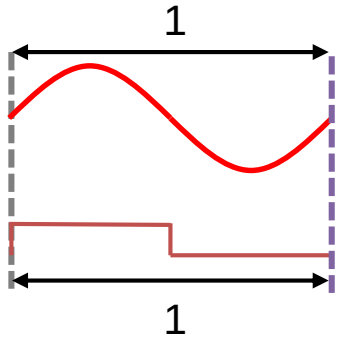
$f_{CLK} \gg f_{sin}$ $f_{CLK} \approx \frac{1}{\alpha} f_{sin} \left(\alpha = 1, \frac{1}{2}, \frac{1}{3}, \frac{2}{3}, \cdots, \frac{1}{6}, \cdots\right)$ $f_{CLK} \approx f_{sin}$

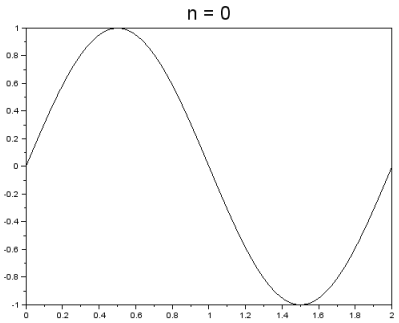










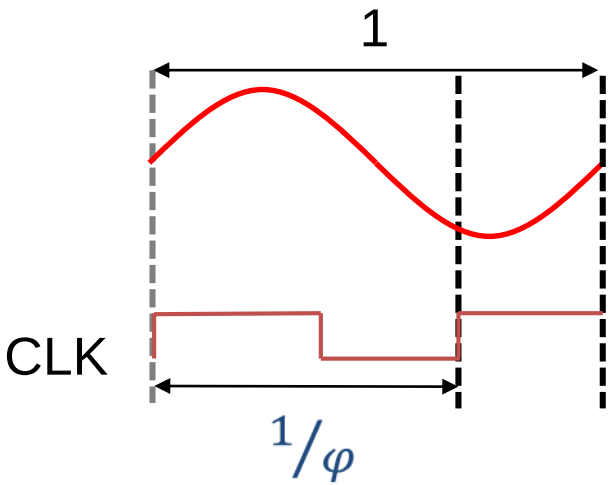


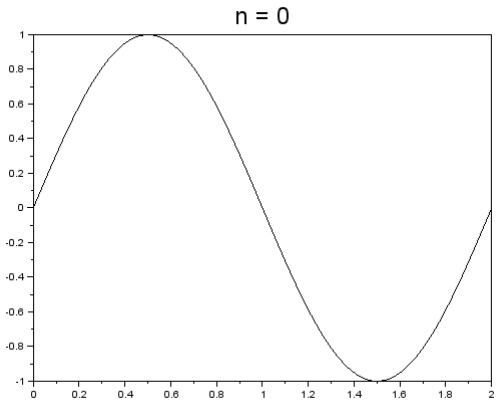
Sampling points move little ➡ Requires long time

Our Proposed Optimal Condition

$$f_{CLK} = \varphi \times f_{sig}$$

φ : Golden ratio (= 1.6180339887…)





Sampling points disperse uniformly through measurement

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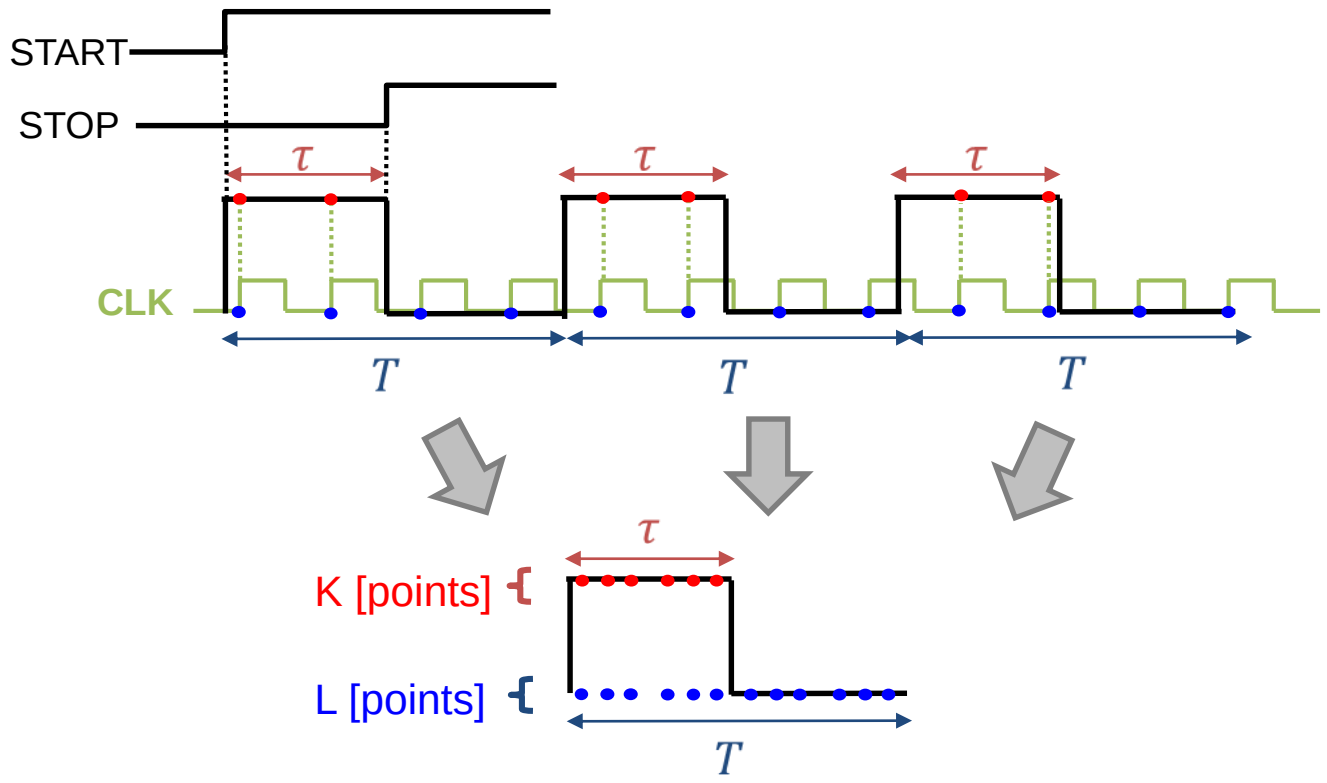
Random Sampling

Y. Sasaki, H. Kobayashi,
“Integral-type Time-to-Digital Converter,“
IEEE 14th International Conference on Solid-State and Integrated Circuit Technology,
Qingdao, China (Nov. 2018)

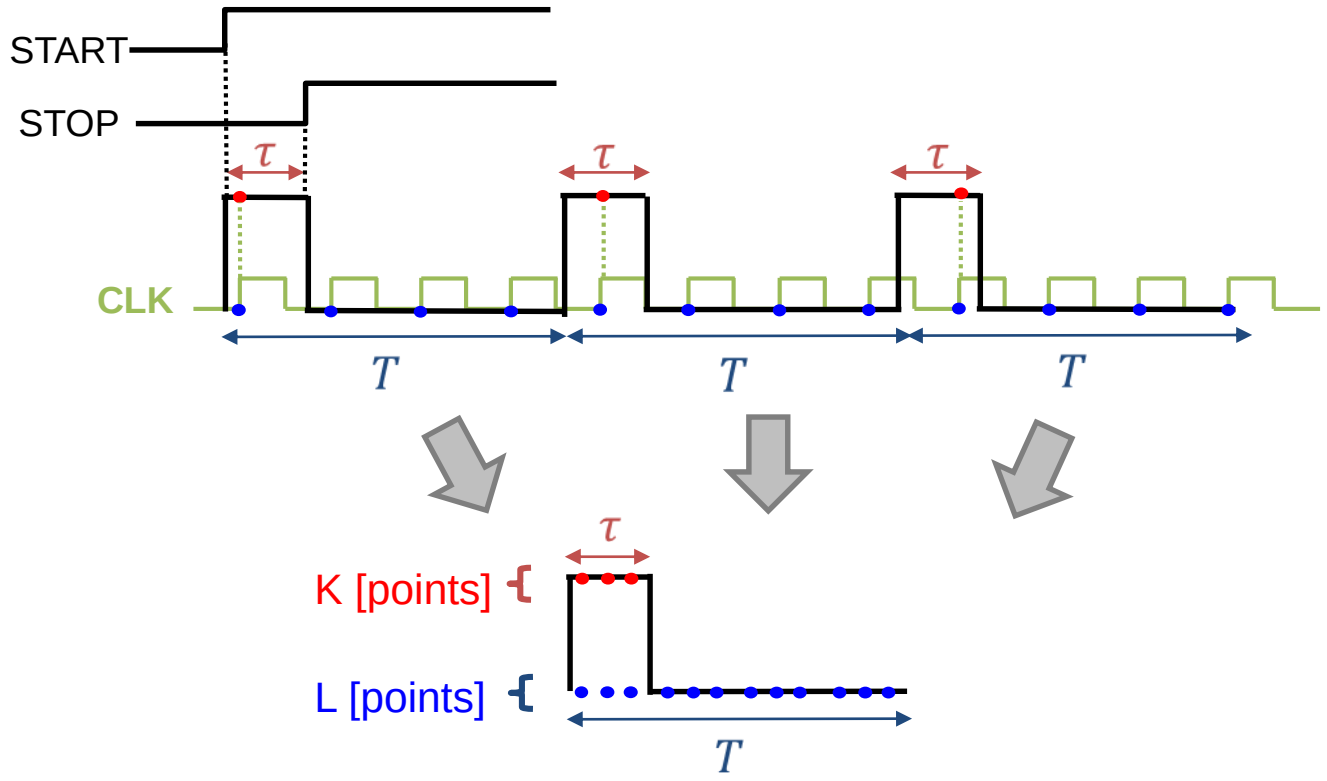
Proposed Integral TDC Principle (1/3)



Sampling a square wave with **input time difference τ** / **reference period T** duty cycle

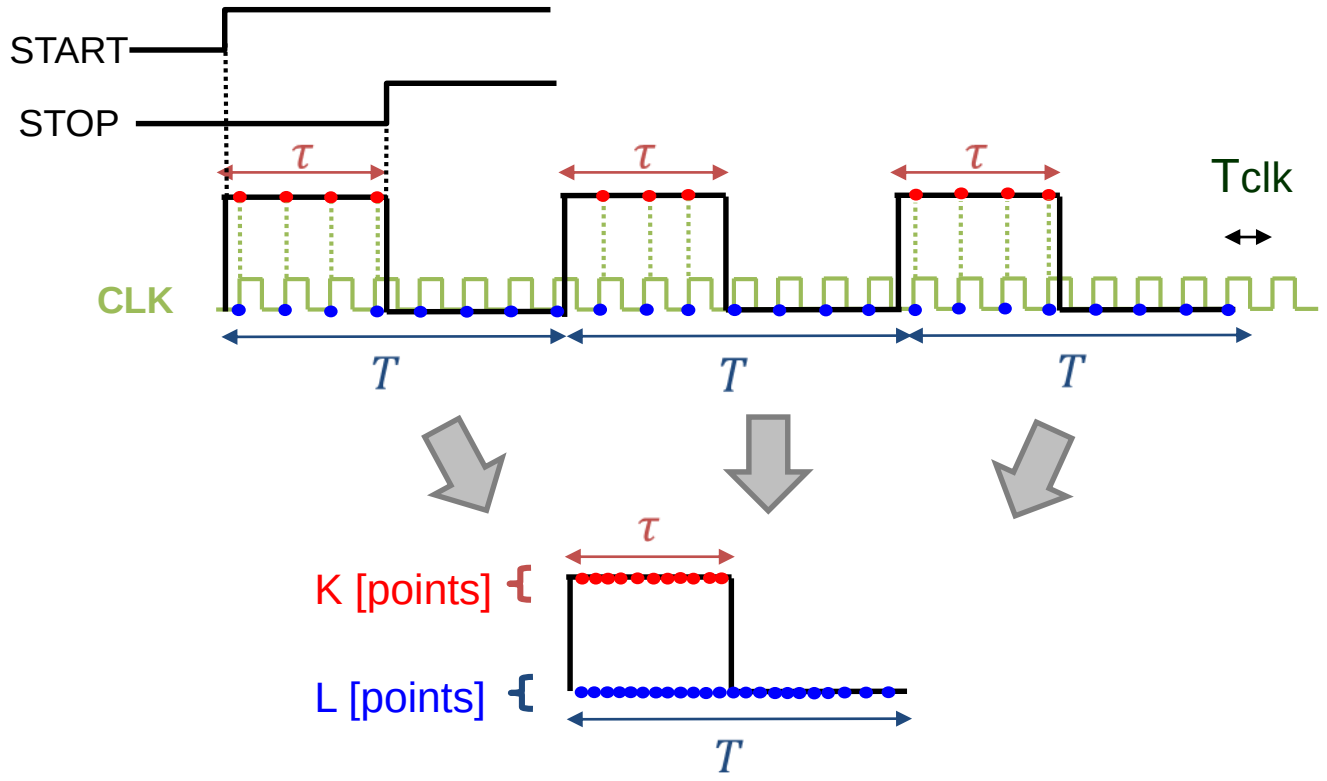
$$\lim_{L\to\infty}\frac{K}{L}=\frac{\tau}{T}$$

Proposed Integral TDC Principle (2/3)



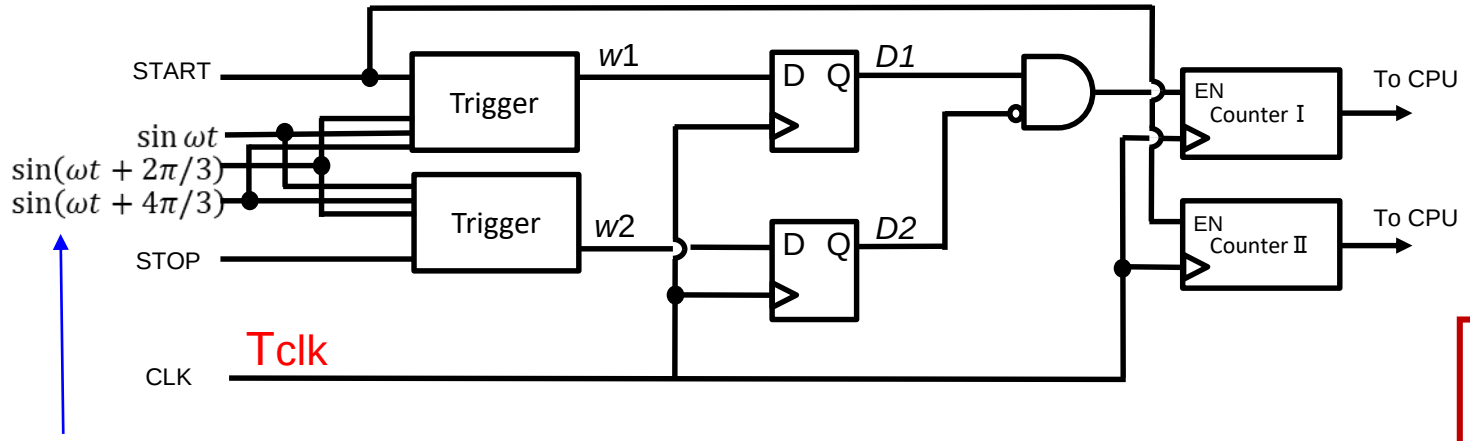
Square wave duty cycle depends on input time difference τ

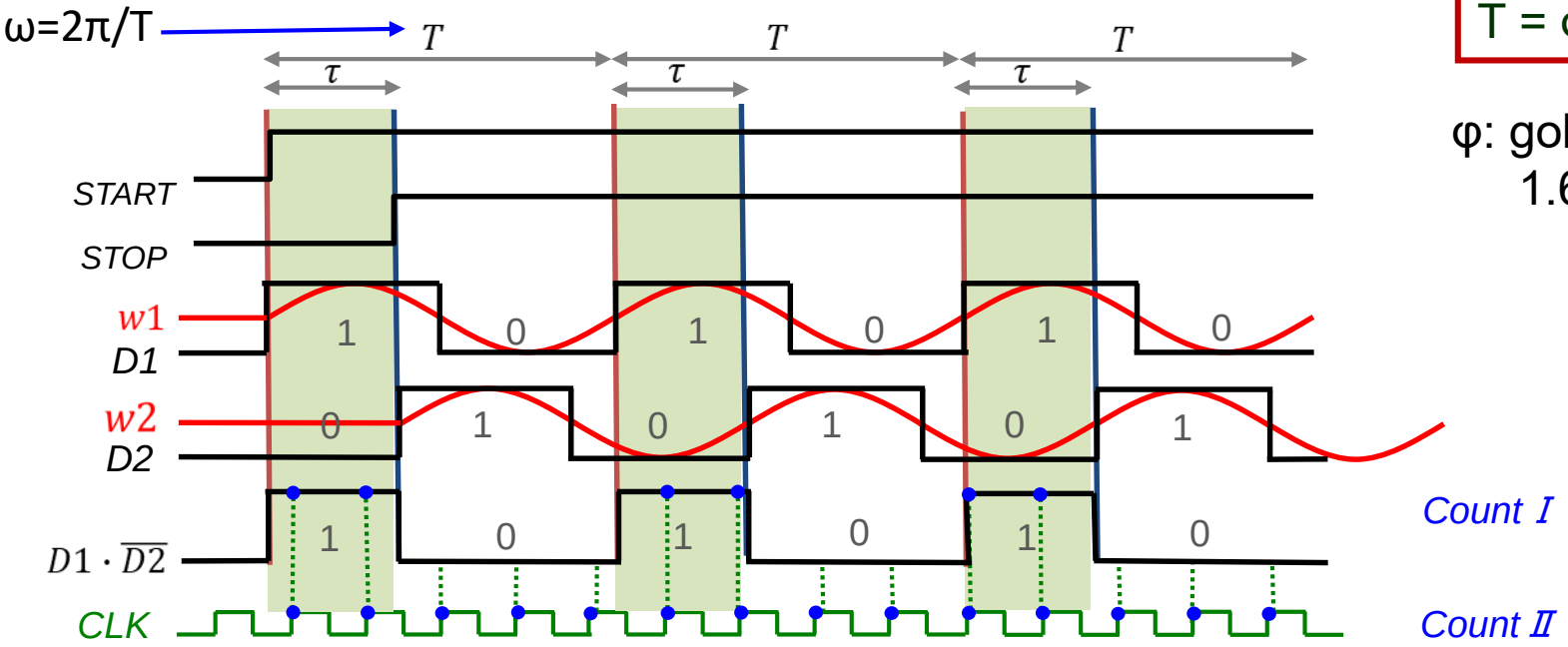
Proposed Integral TDC Principle (3/3)



Acquiring more data improves time resolution

Proposed Integral TDC Configuration

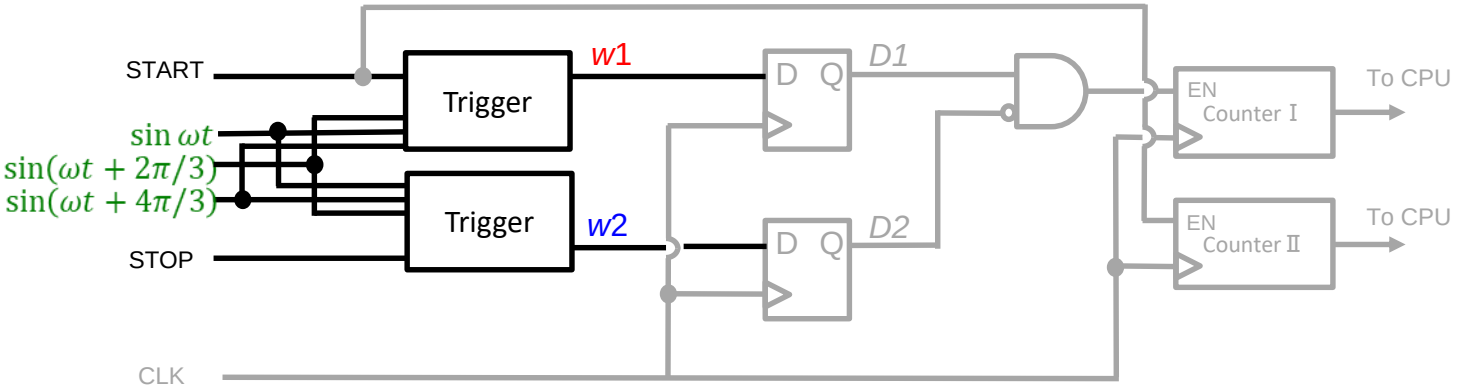




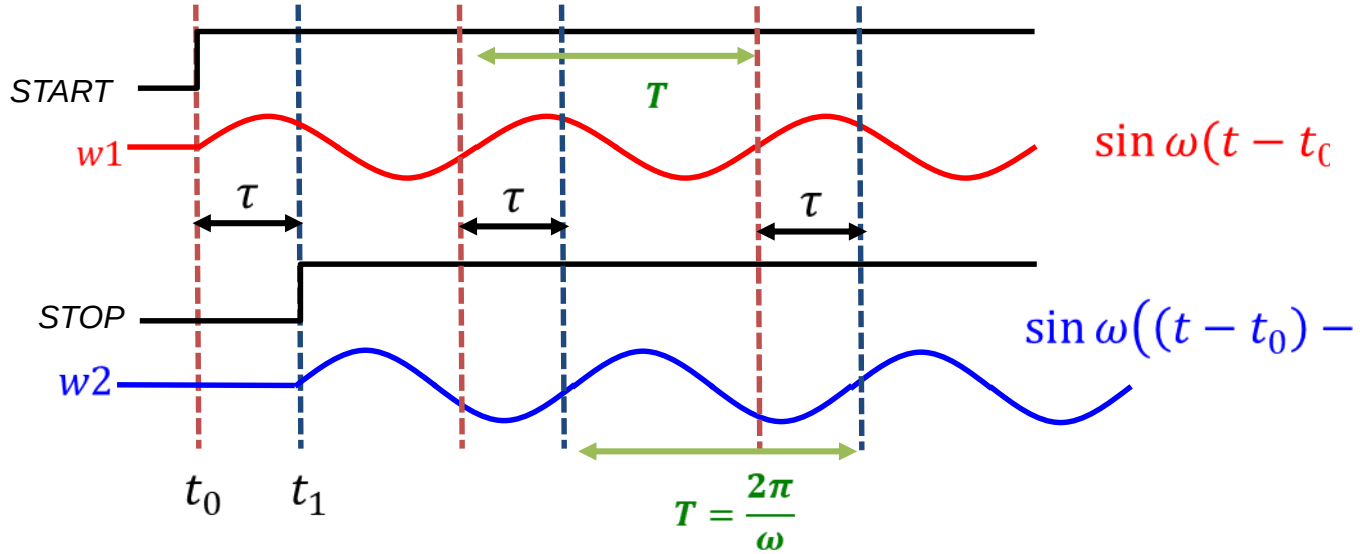
Optimal Condition
T = φ x Tclk

φ: golden ratio
1.61…

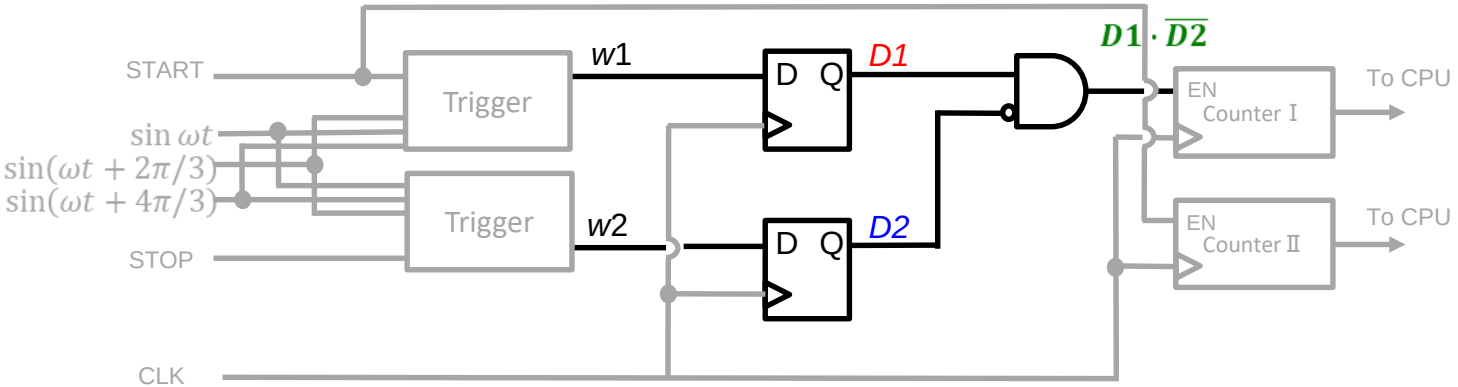
Proposed Integral TDC Operation (1/3)



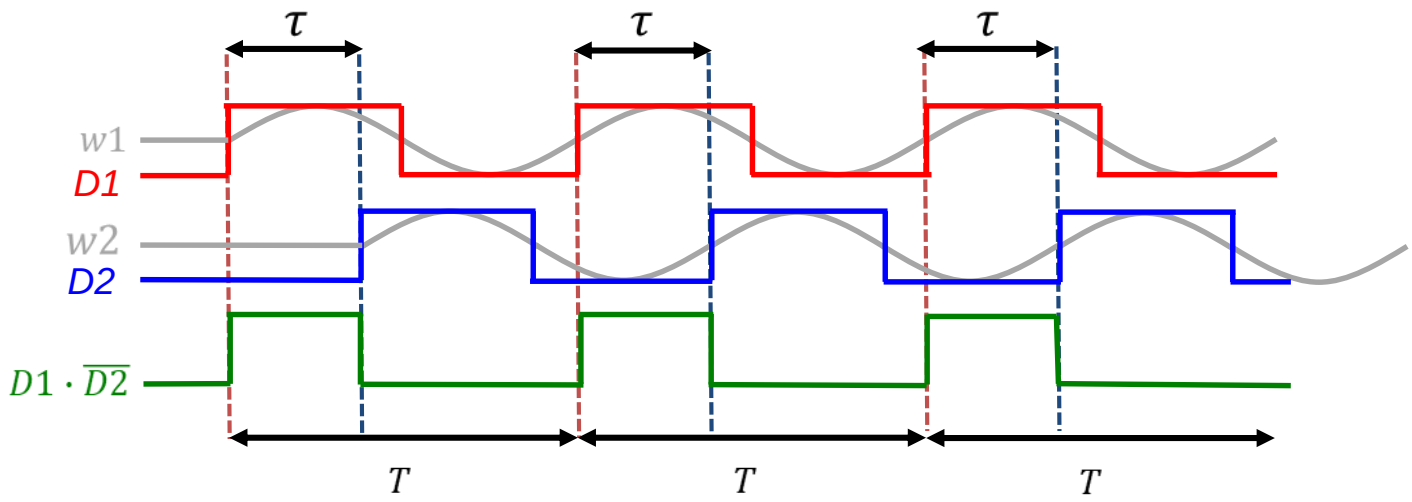
STEP1: Holding the input time difference τ as phase difference



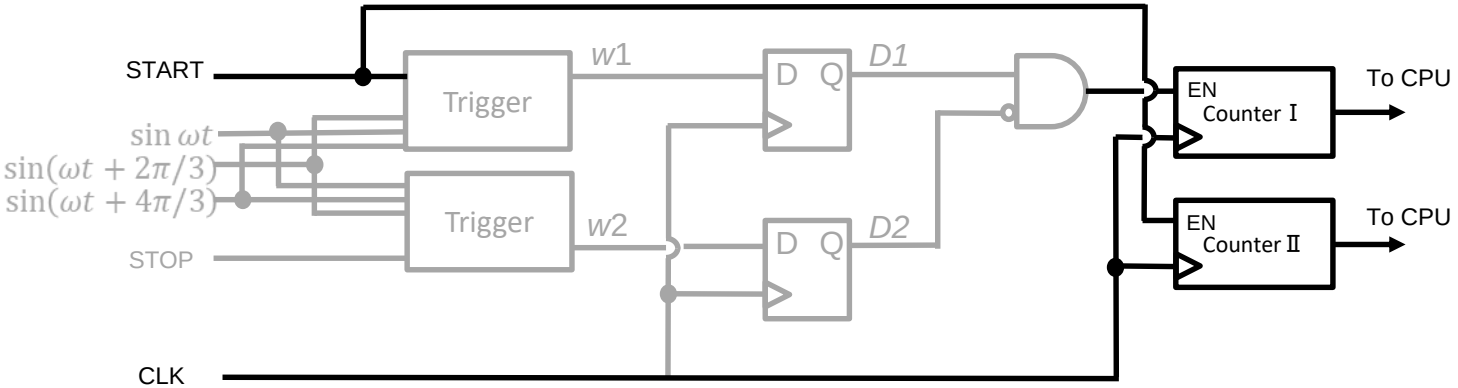
Proposed Integral TDC Operation (2/3)



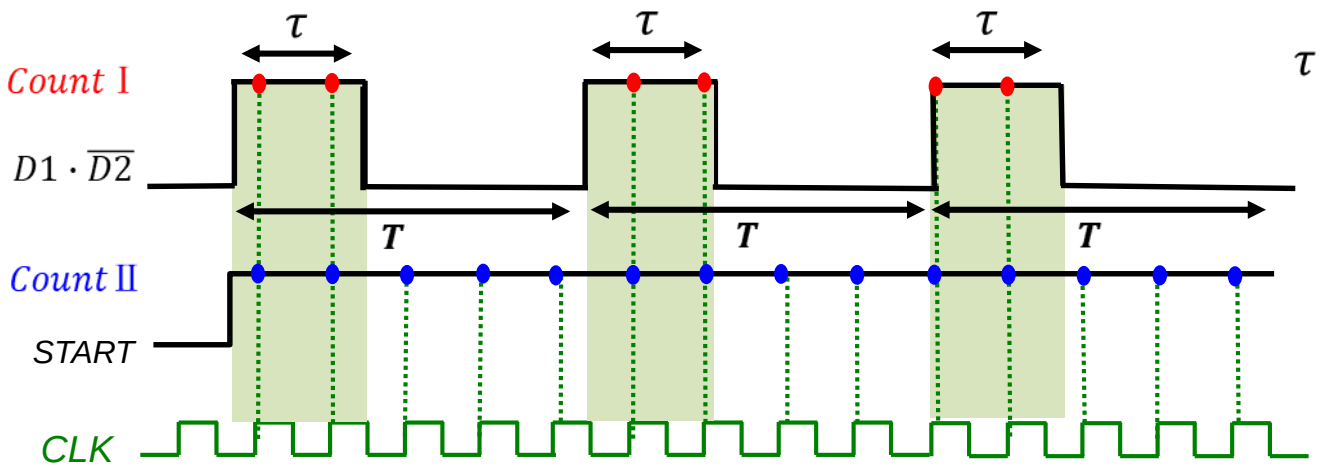
STEP2: Making the square wave with τ / T duty cycle



Proposed Integral TDC Operation (3/3)

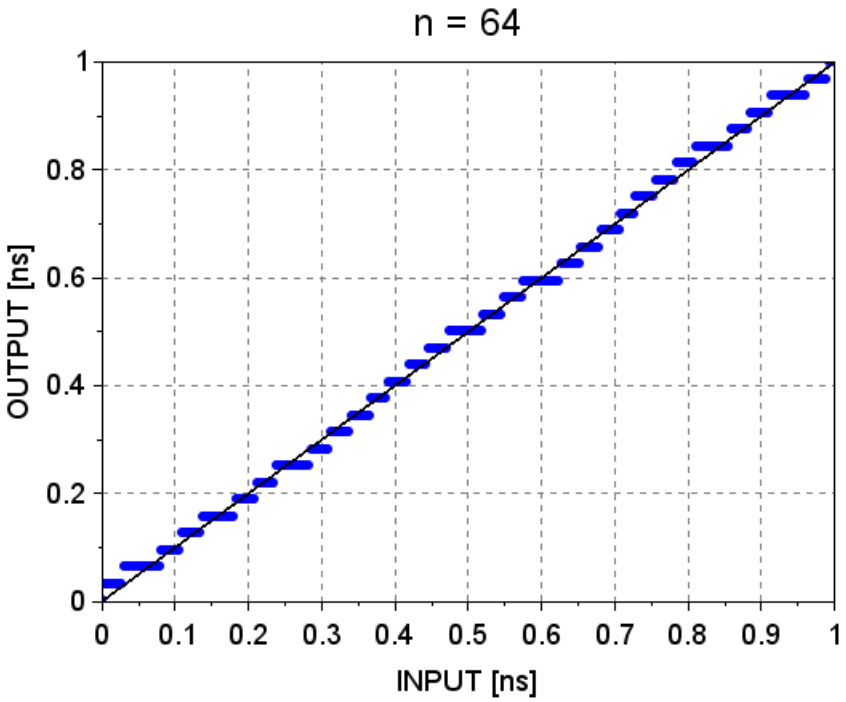


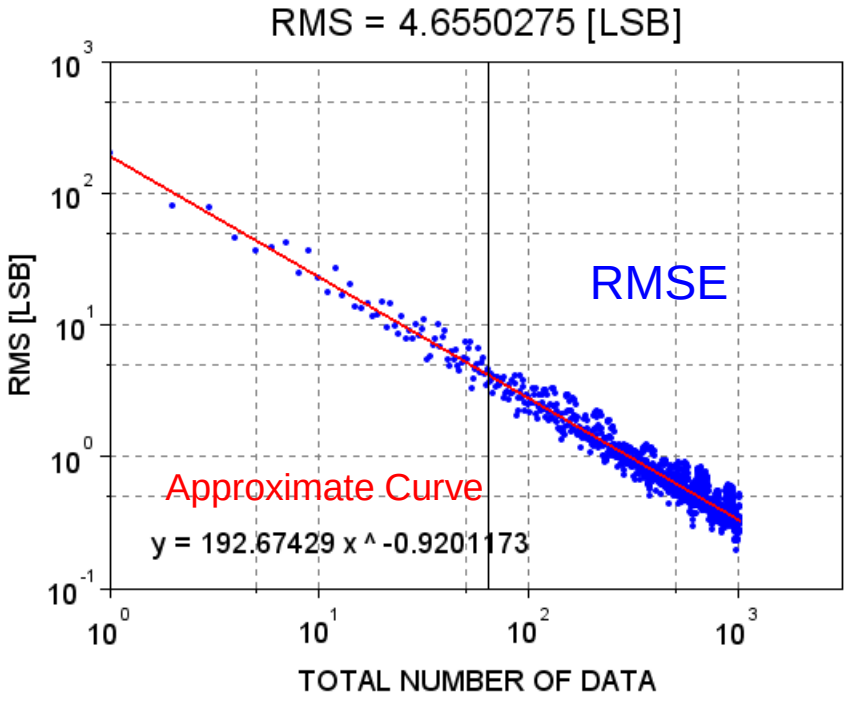
STEP3: Counting the ratio of the sampling points



$$\tau = \frac{Count\ \mathrm{I}}{Count\ \mathrm{II}} T$$

Simulation Result





Acquiring more data improves time resolution

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  - Integral TDC

Sequential Sampling

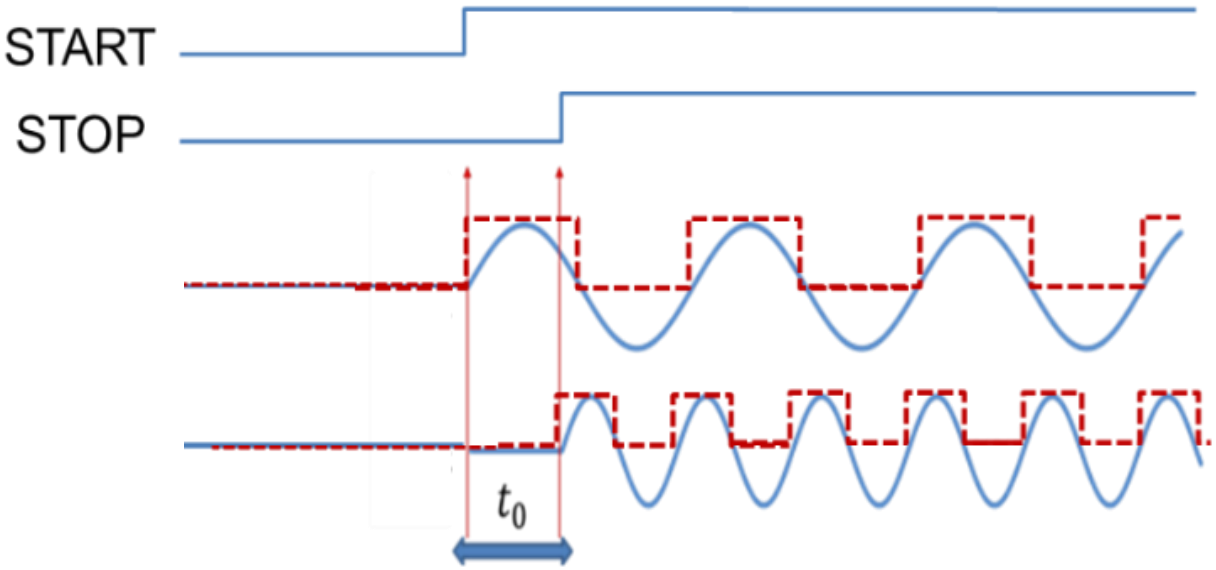
  - Vernier Frequency TDC

Z. Pengfei, K. Machida, Y. Sasaki, Y. Ozawa, A. Kuwana, H. Kobayashi
"High Resolution Time-to-Digital Converter Using Integral Architecture and Vernier Oscillators"
5th Taiwan and Japan Conference on Circuits and Systems,
Nikko, Japan (Aug. 2019)

K. Machida, Y. Ozawa, Y. Abe, H. Kobayashi,
"Time-to-Digital Converter Architectures Using Two Oscillators With Different Frequencies",
27th IEEE Asian Test Symposium, Hefei, Anhui, China (Oct. 2018)

Vernier Frequency TDC

What about using different frequencies ?

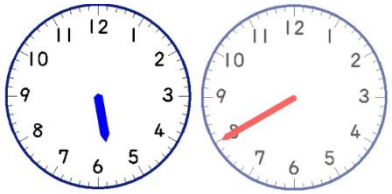


*f*1: known

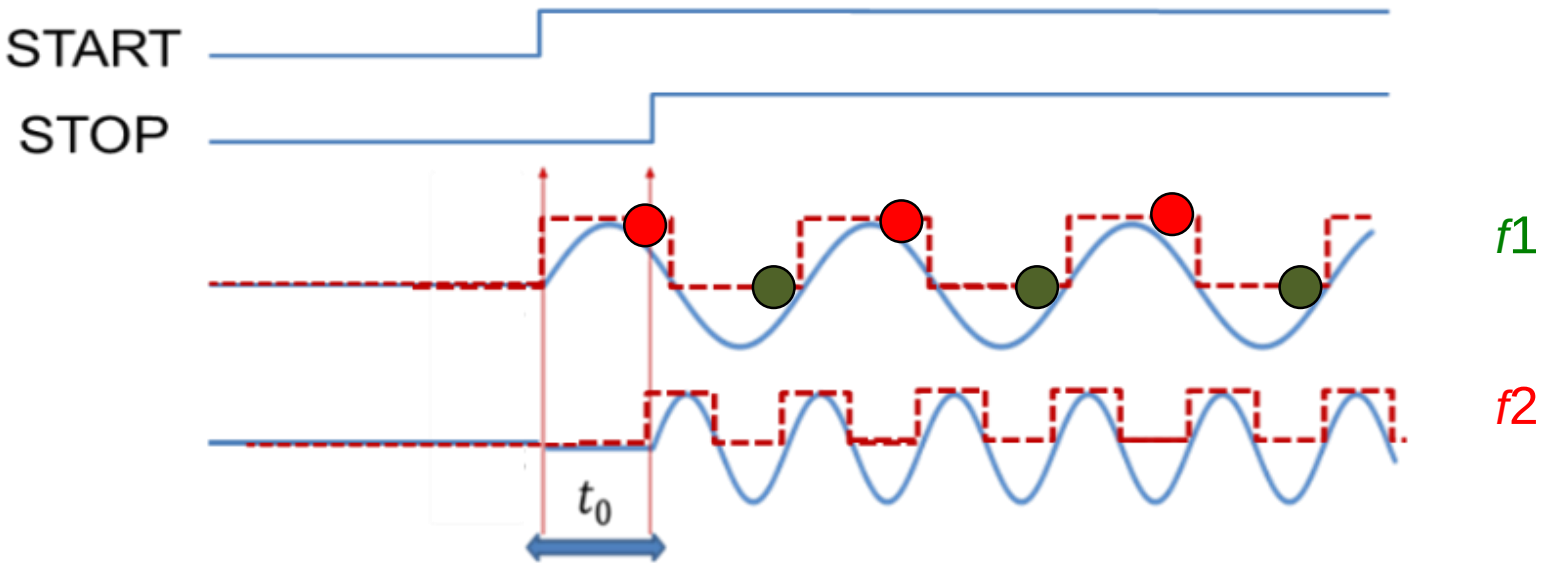
*f*2: known

Start oscillation *f*1 at START edge

*f*2 at STOP edge



Vernier Frequency TDC Operation

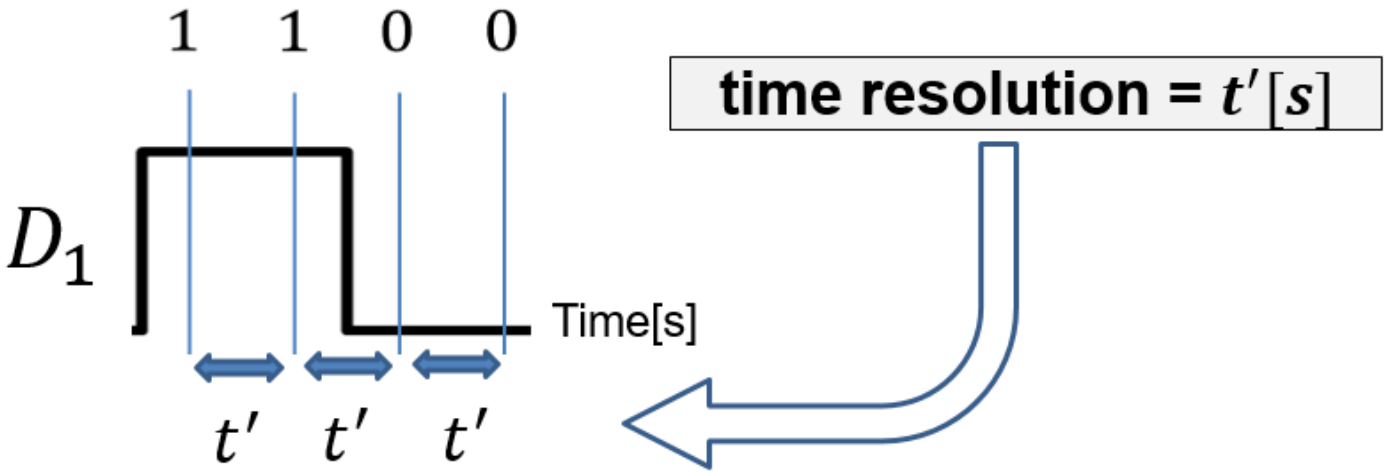


t_0 = *f* (*f*1, *f*2, number of ●, ●…, number of ● ●…)

$f1 \fallingdotseq f2$

Time resolution $t' = \left| \frac{1}{f_2} - \frac{1}{f_1} \right|$

Usage of Different but Close Frequencies



Equivalent Sampling

Different Frequencies

$$t' = \left|\frac{1}{f_2} - \frac{1}{f_1}\right| \qquad f_1 = 1[MHz] \quad f_2 = 0.9999[MHz]$$

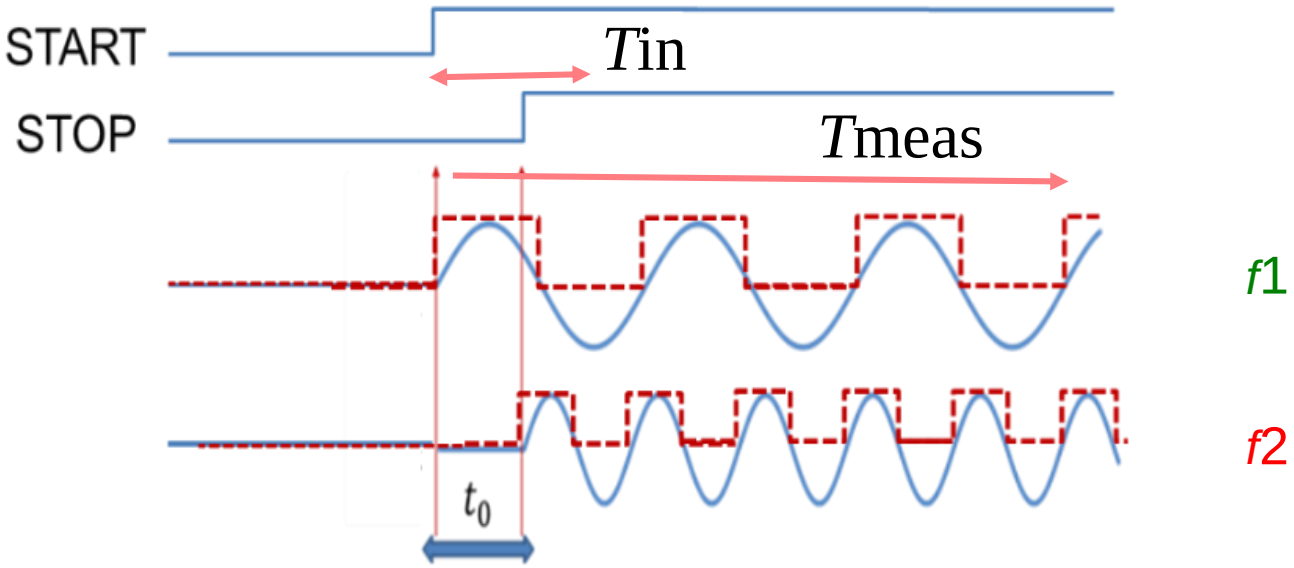
$$t' \cong 1 \times 10^{-10}[s]$$

$f1 \fallingdotseq f2$

Different frequencies →**Fine time resolution** ⟺ **Long measurement time**

Trade off

Design Tradeoff

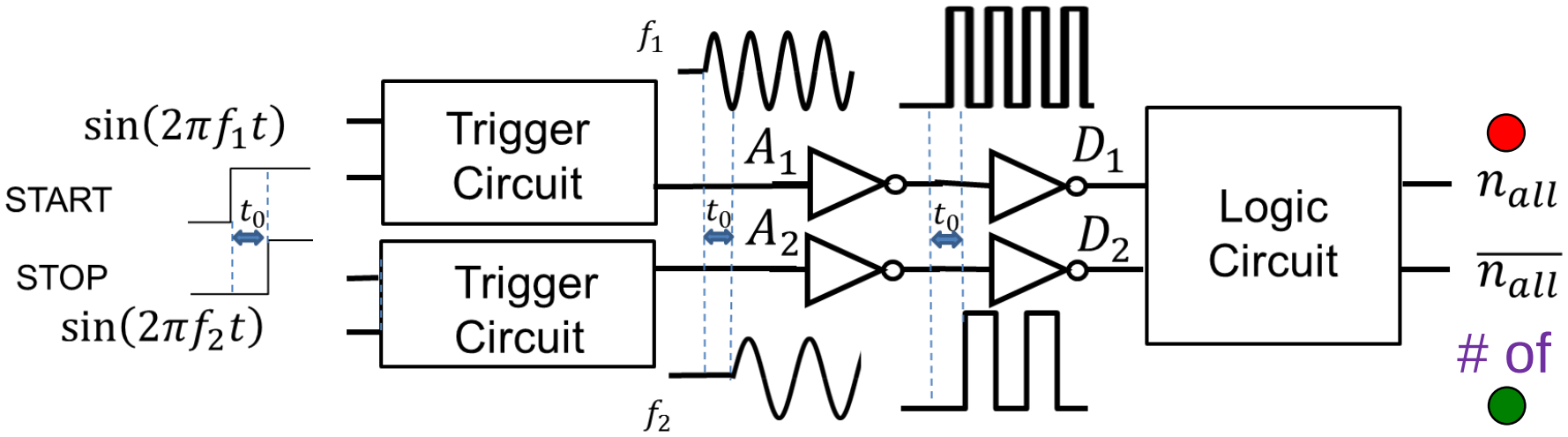


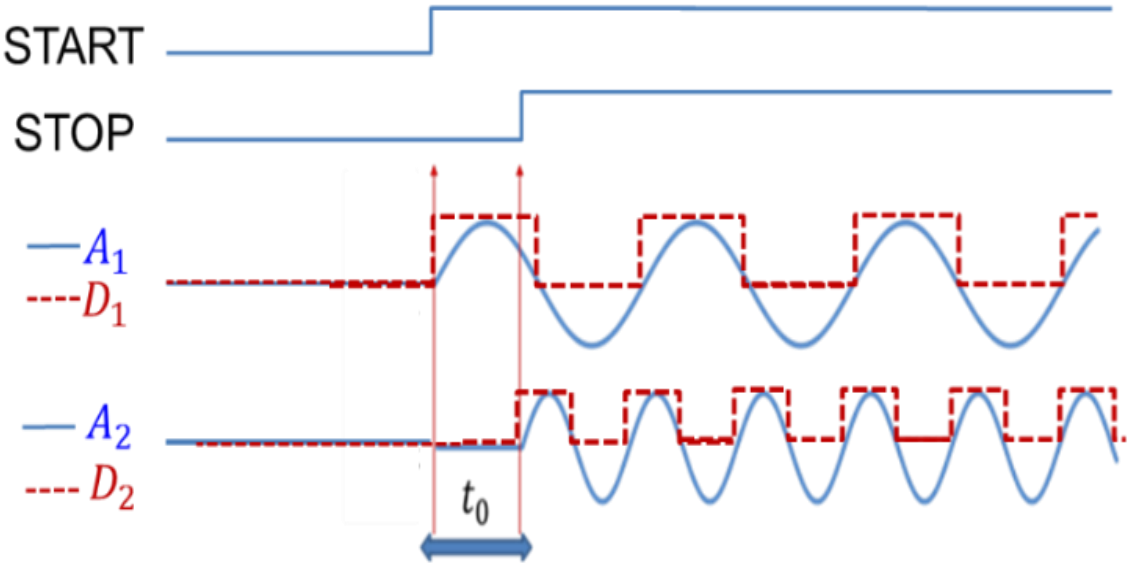
Fine time resolution $t' = \left| \frac{1}{f_2} - \frac{1}{f_1} \right|$

$Tin = 1/f1, 1/f2$ ⟷ $Tmeas = Tin \times Tin / t'$

Wide input time range — Long Measurement time

Proposed TDC Architecture

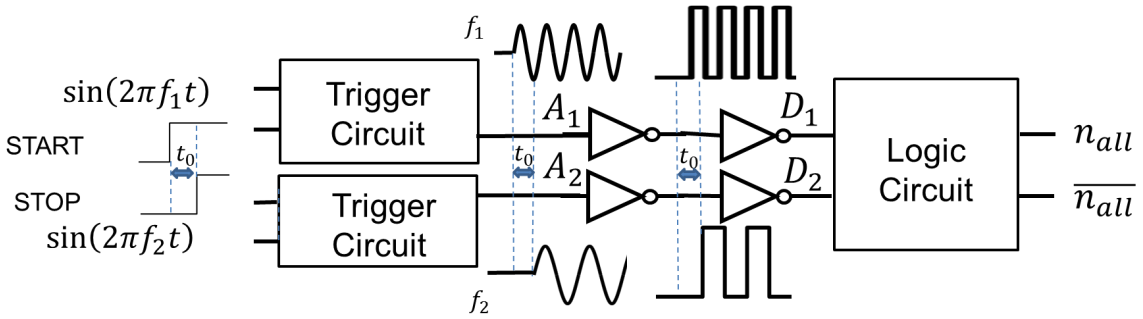


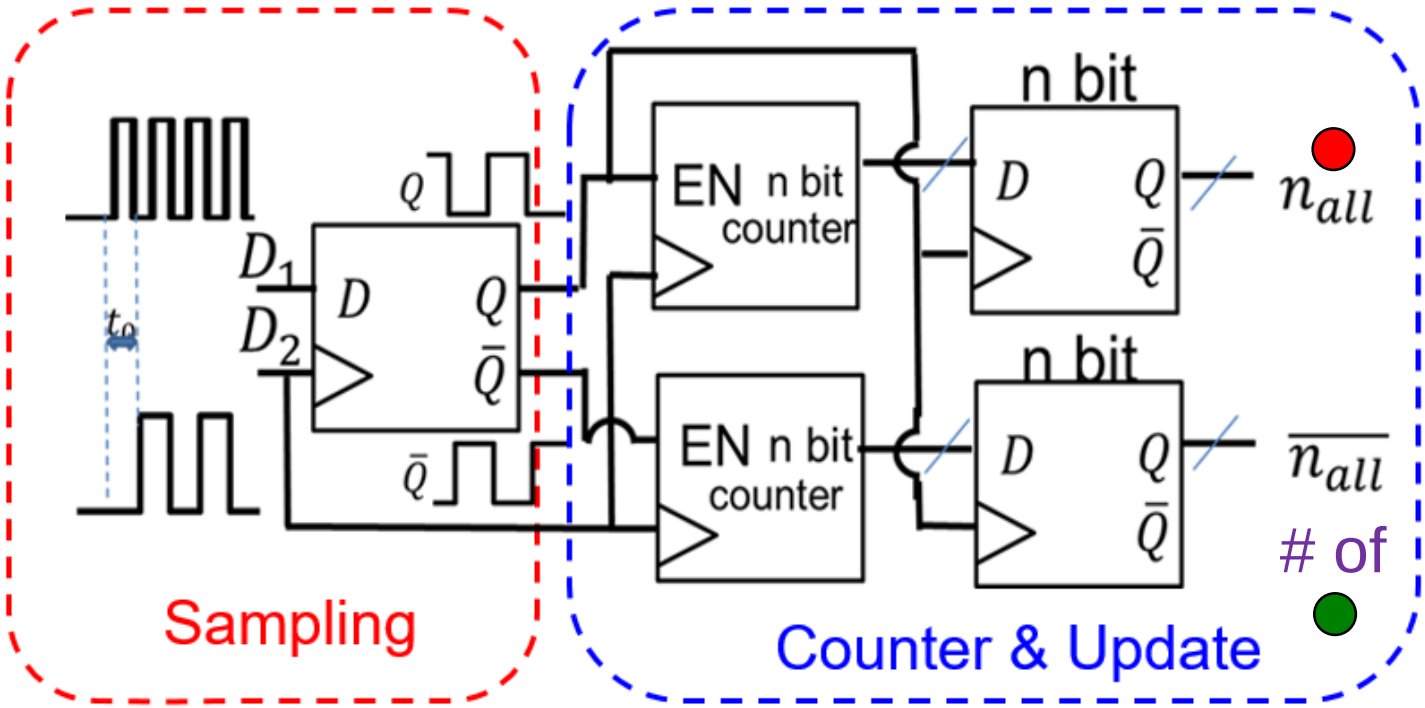


f1: known

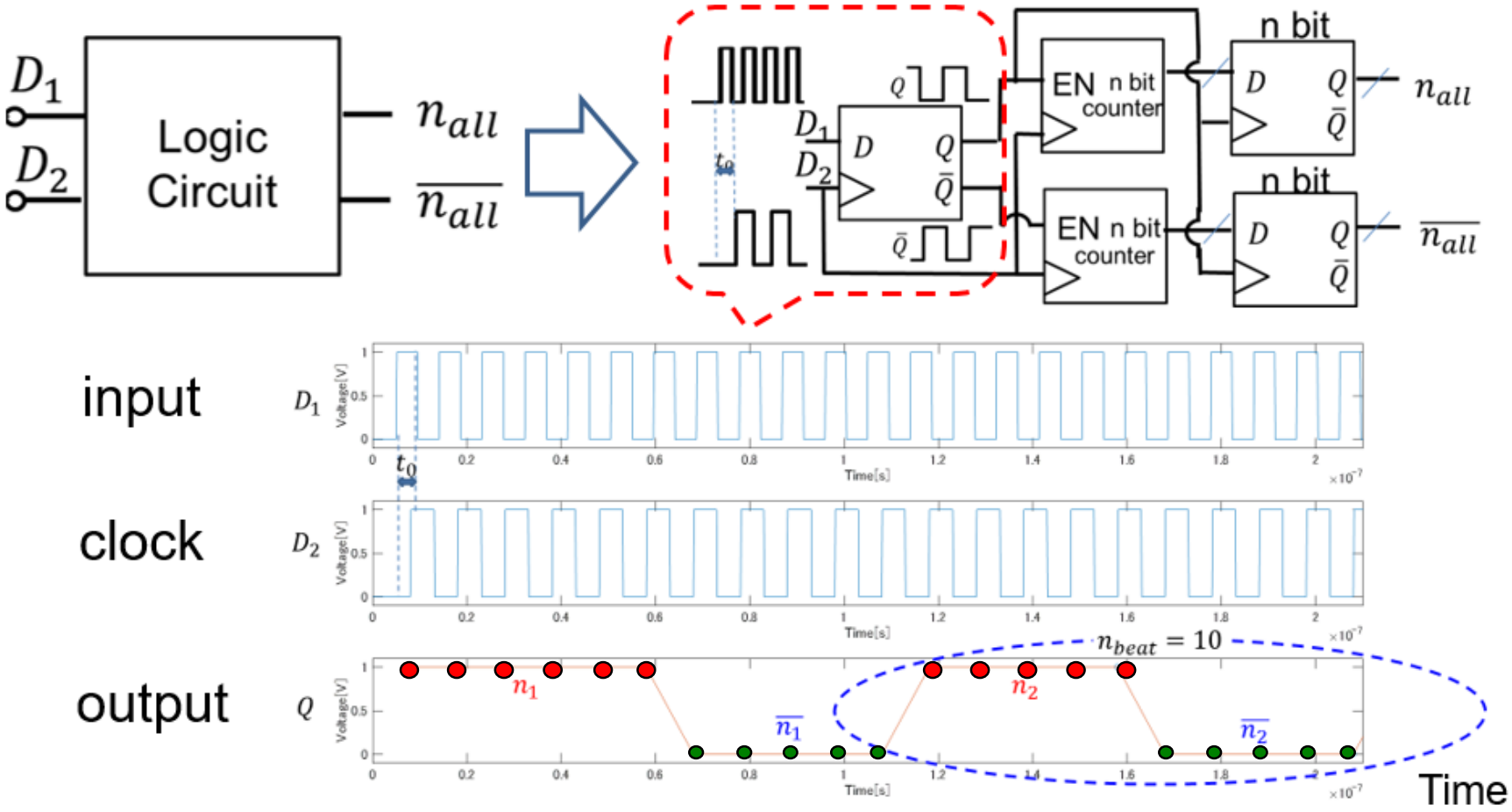
f2: known

Logic Circuit for Time Measurement





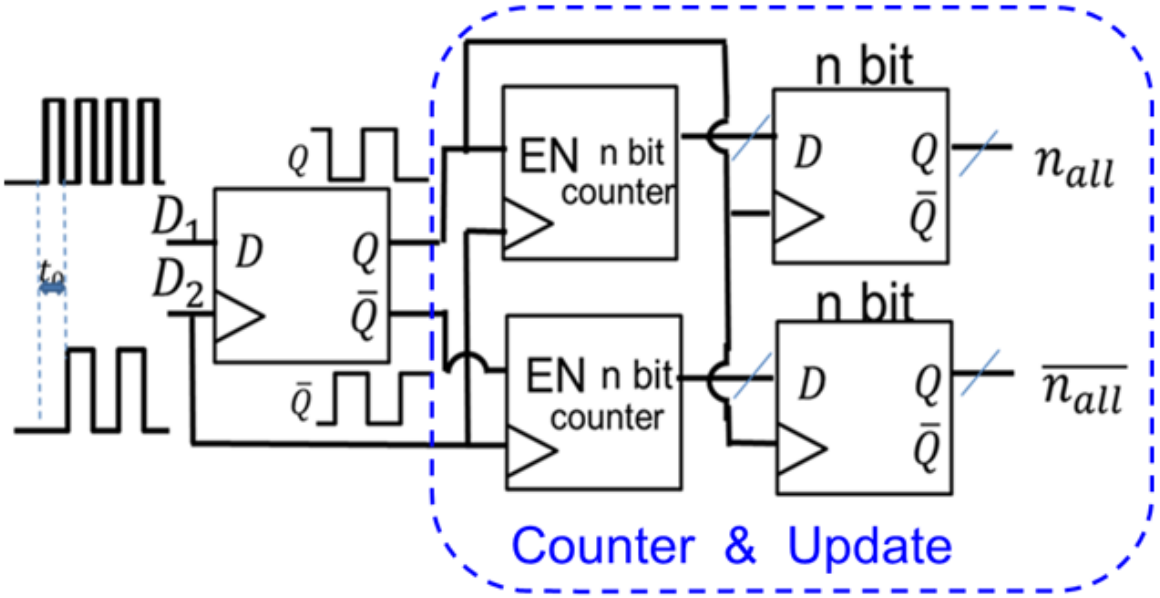
D1 Sampling by D2

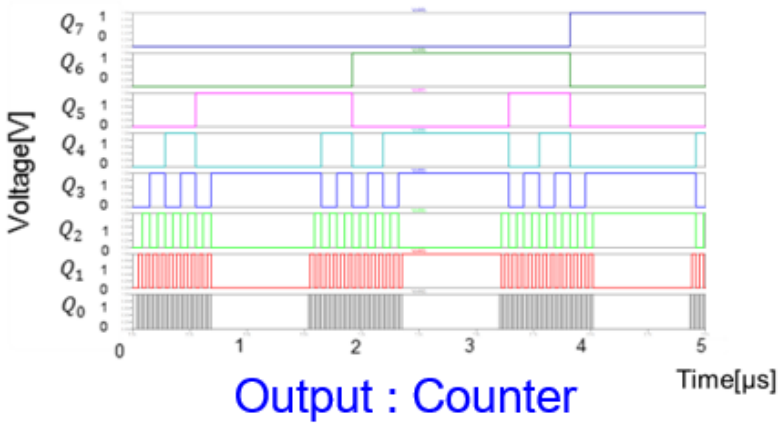


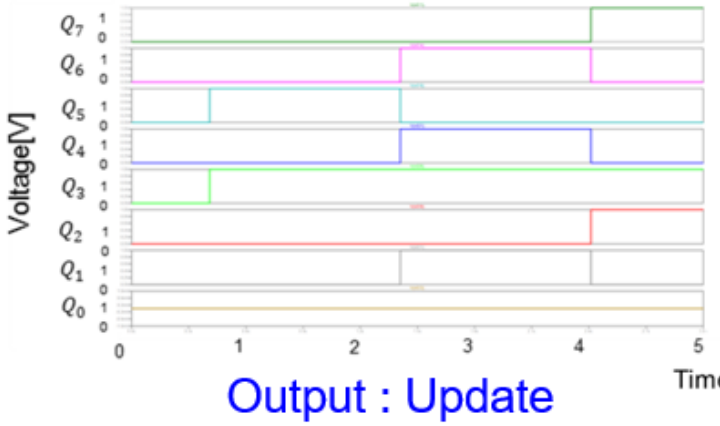
$$n_{all}(= n_1 + n_2 \dots) \qquad \overline{n_{all}}(= \overline{n_1} + \overline{n_2} \dots)$$

$$n_{beat} = n_2 + \overline{n_2} = n_3 + \overline{n_3} = \cdots = \frac{f_2}{|f_2 - f_1|}$$

Counter & Update

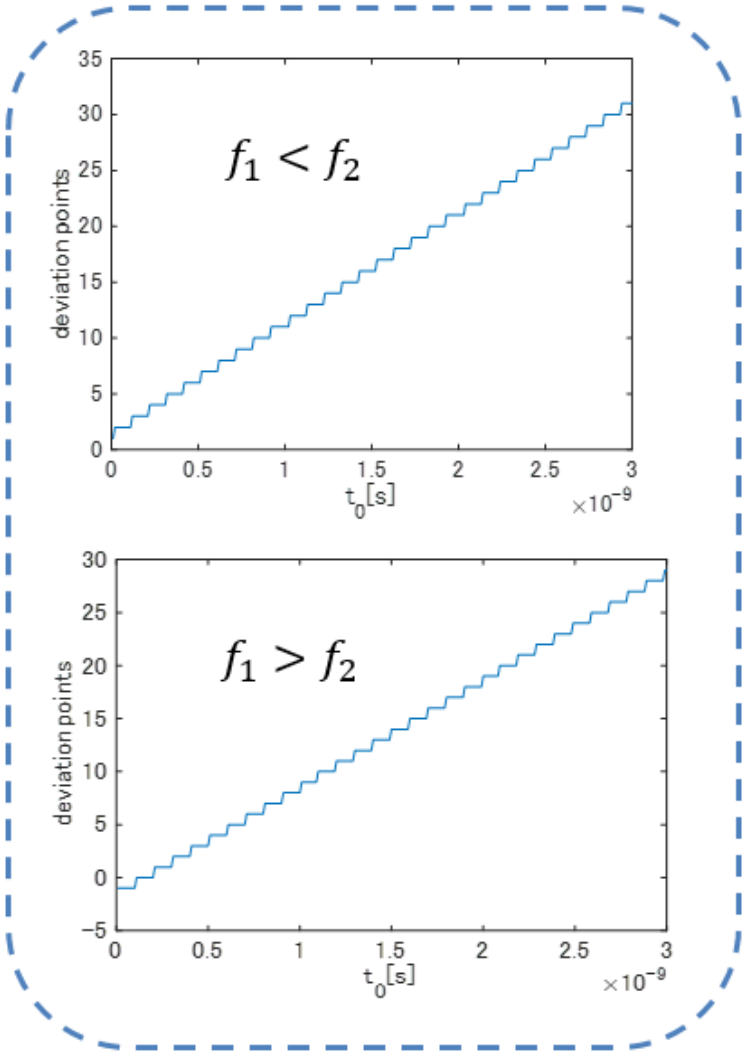


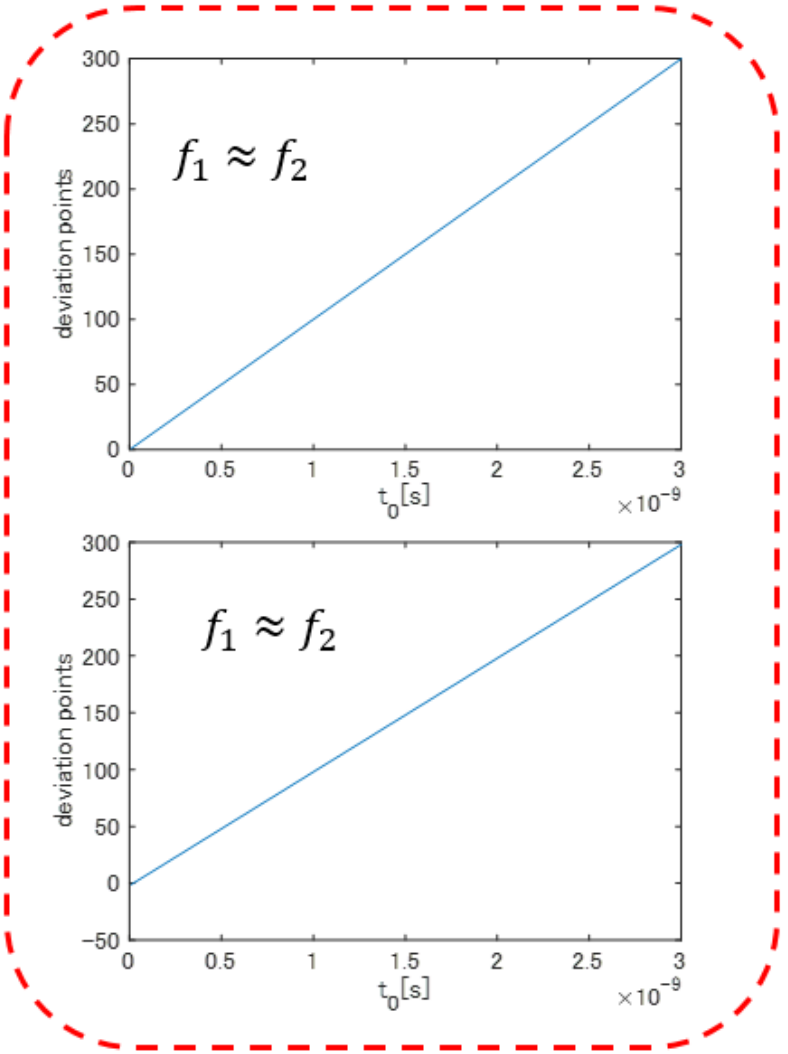




Digital value

Vernier Frequency TDC Simulation Result





Low Linearity ⇒ High Linearity

Integral TDC Conclusion

- Time difference can be held with 2 trigger circuits

- Equivalent-time sampling
  - Random sampling
    - ⇒ Integral TDC
  - Coherent sampling
    - ⇒ Optimal sampling condition
  - Sequential sampling
    - ⇒ Vernier frequency TDC

- Oscillators can be shared among multi-channel TDCs

Outline

- Research Background
- Integral-type TDC
  - Time Hold Circuit
  - Equivalent-Time Sampling

Y. Osawa, D. Hirabayashi, N. Harigai , H. Kobayashi, K. Niitsu, O. Kobayashi
“Phase Noise Measurement Techniques Using Delta-Sigma TDC”,
IEEE International Mixed-Signals, Sensors and Systems Test Workshop
Porto Alegre, Brazil (Sept. 2014).

- Delta-Sigma TDC
  for Phase Noise Measurement
- Conclusion

Outline

- Research Background & Objective
- Delta-Sigma TDC
- Phase Noise Measurement using ΔΣTDC
  with Reference Clock
- Phase Noise Measurement using ΔΣTDC
  without Reference Clock
  - Self-Referenced Clock Technique
- Conclusion

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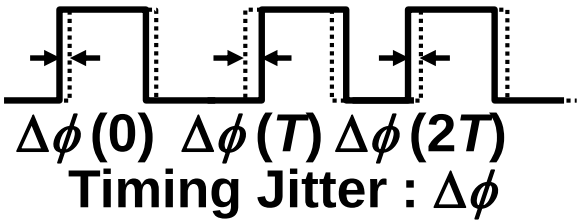
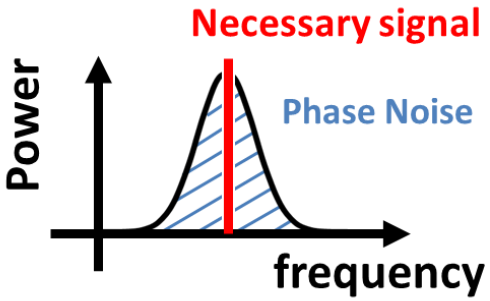
Research Background

Phase noise of clock can cause malfunctions of electronic systems



Oscillator phase noise



Electronic system performance degradation

- **RF circuit & system**
- **ADC**

Test & measurement for phase noise, jitter is important

Conventional Method

Conventional Phase Noise Measurement

- **Expensive :** Spectrum Analyzer
- **Long testing time:** ~10 seconds

Mass production

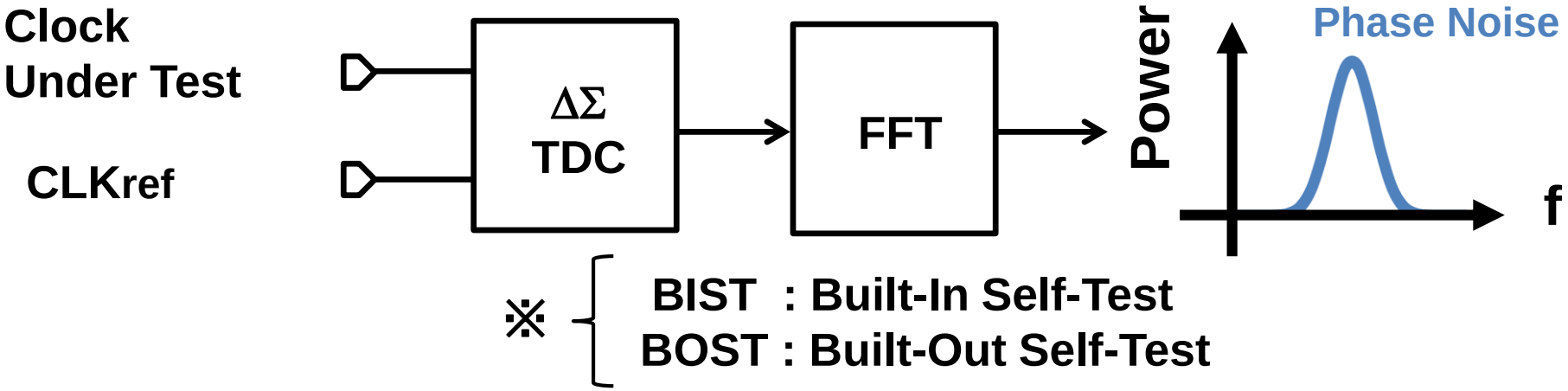
Test cost → **high**

Research Objective

Low cost, high quality phase noise measurement

- w/o Spectrum Analyzer

- w/ BIST or BOST　Simple circuit



※ BIST : Built-In Self-Test
BOST : Built-Out Self-Test

Outline

- Research Background & Objective
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- Phase Noise Measurement using ΔΣTDC without Reference Clock
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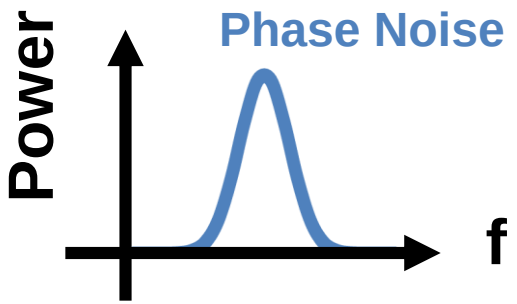
Phase Noise Measurement Flow

Phase noise : Frequency characteristics

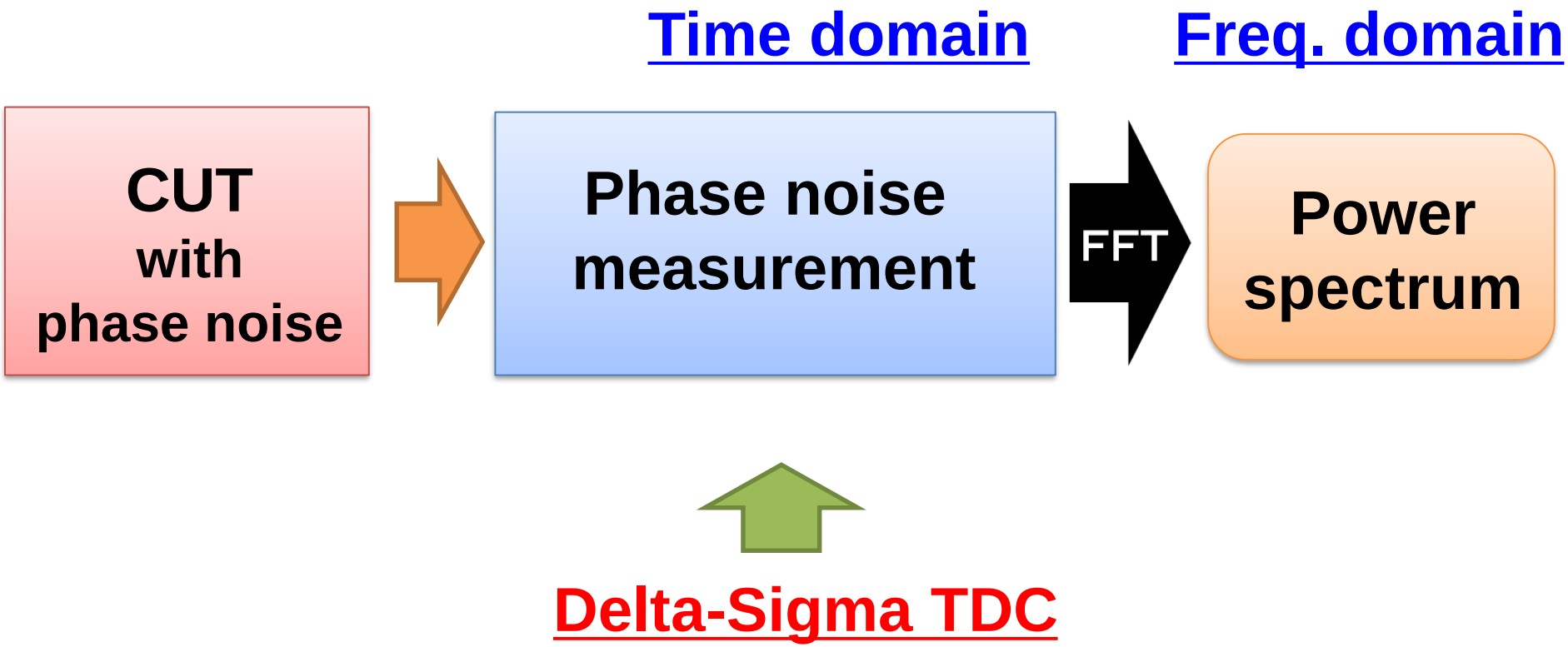


Time domain **Freq. domain**

CUT with phase noise → **Phase noise measurement** → **FFT** → **Power spectrum**

CUT : Clock Under Test

Proposed Method



Time resolution improved by longer measurement time

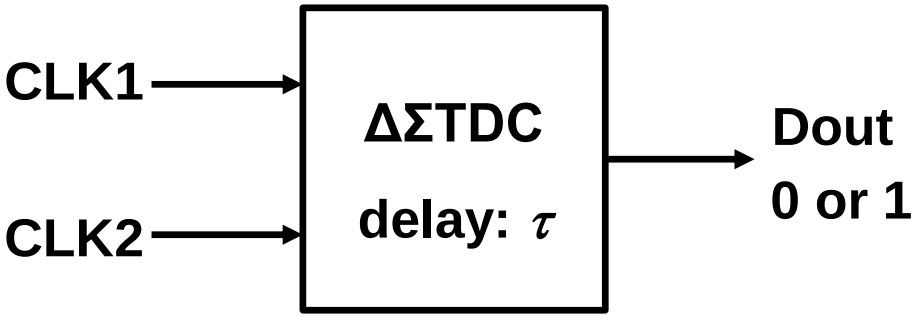
TDC : Time-to-Digital Converter

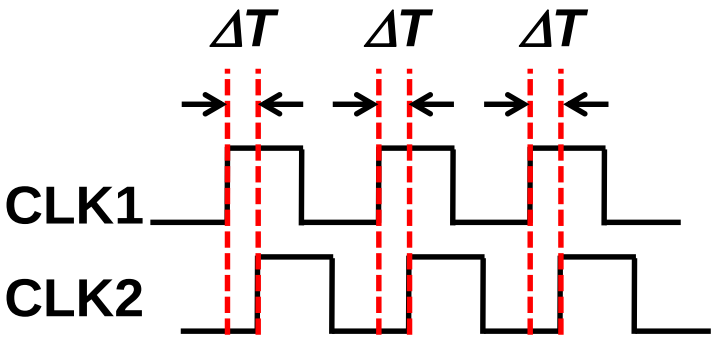
Ex: τ = 1ns, N_{DATA} =64K

T_resolution = 0.03ps

$$T\_resolution \propto \frac{2\tau}{time}$$

Principle of ΔΣTDC





Dout # of 1's is proportional to ΔT

ΔT

# of 1's

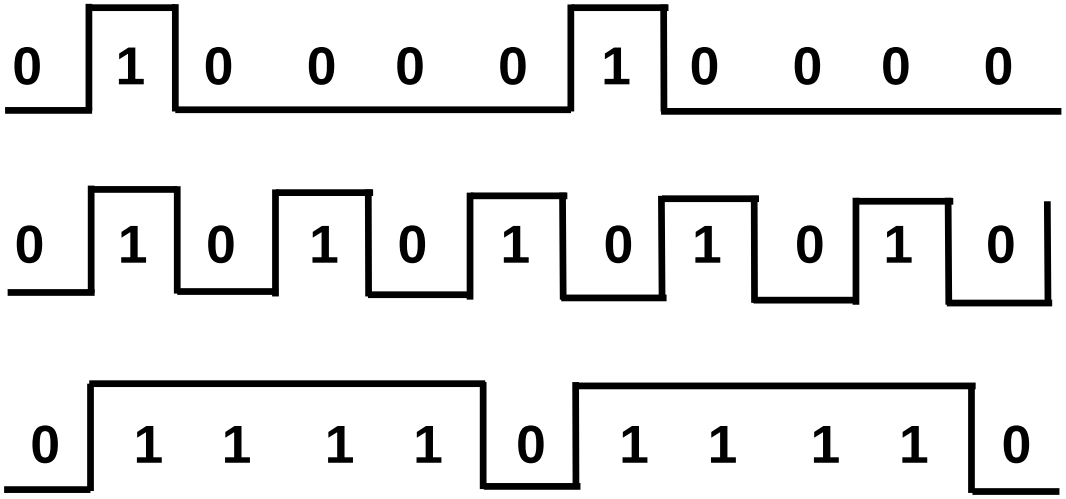
short

few

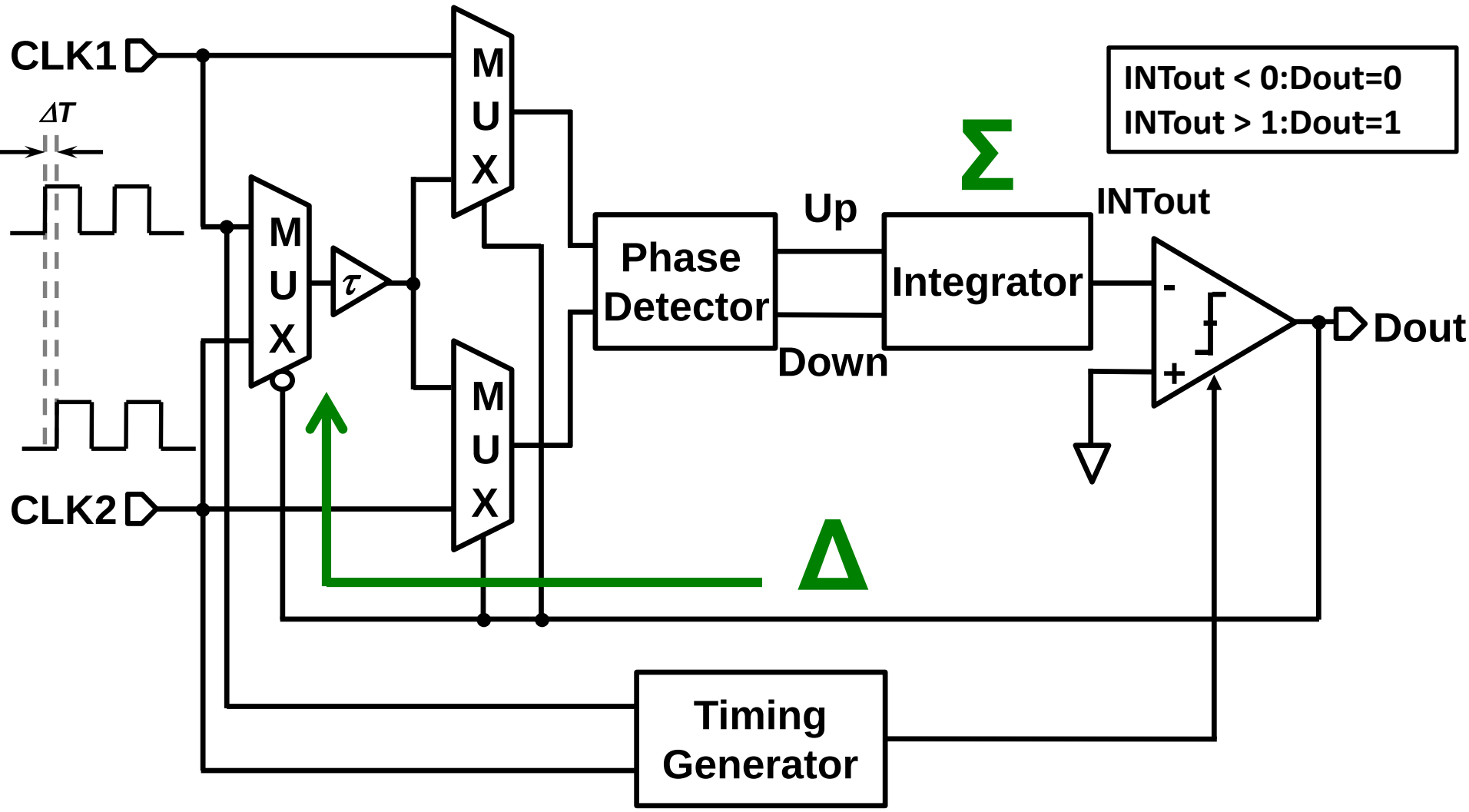
long

many

Dout



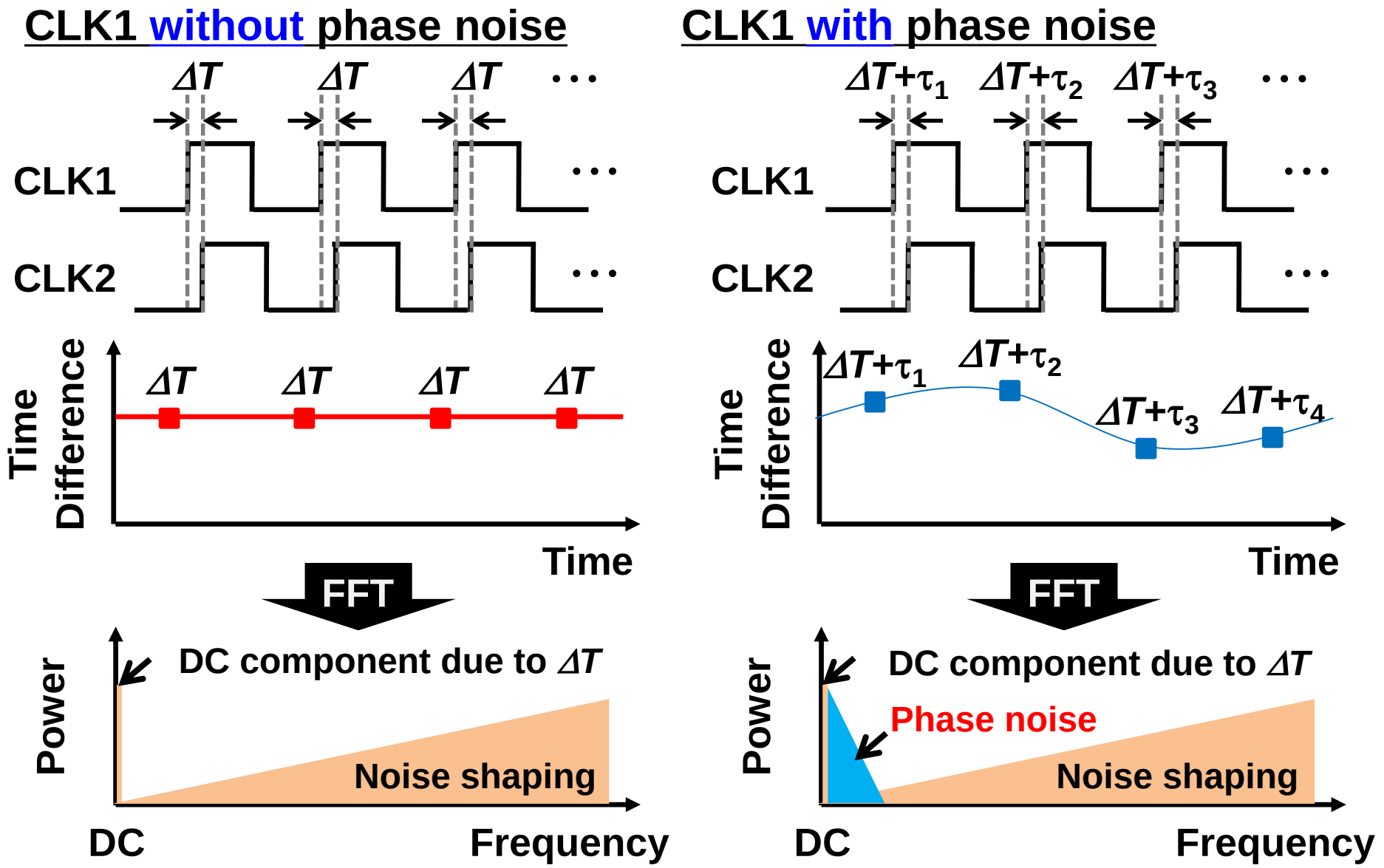
ΔΣTDC Configuration



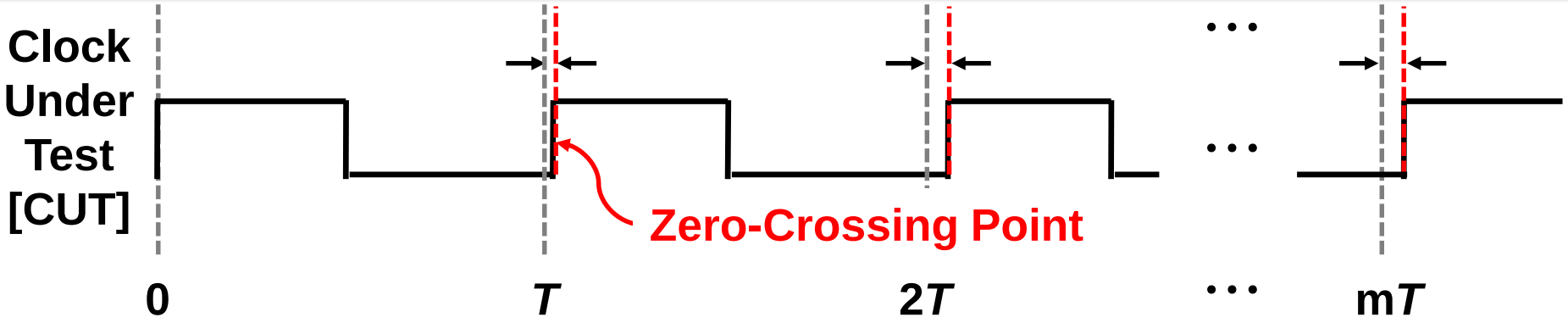
Outline

- Research Background & Objective
- Delta-Sigma TDC
- Phase Noise Measurement using ΔΣTDC with Reference Clock
- Phase Noise Measurement using ΔΣTDC without Reference Clock
  - Self-Referenced Clock Technique
- Conclusion

Principle of Phase Noise Measurement



Mathematical Analysis



$$CUT(t) \approx \sin\left(2\pi f_{in} t + \phi(t)\right)$$

$\tau(m)$: m-th zero-crossing point variation function (noise component)

$\therefore \phi(mT) = -2\pi f_{in}\tau(m)$: phase noise (time domain)

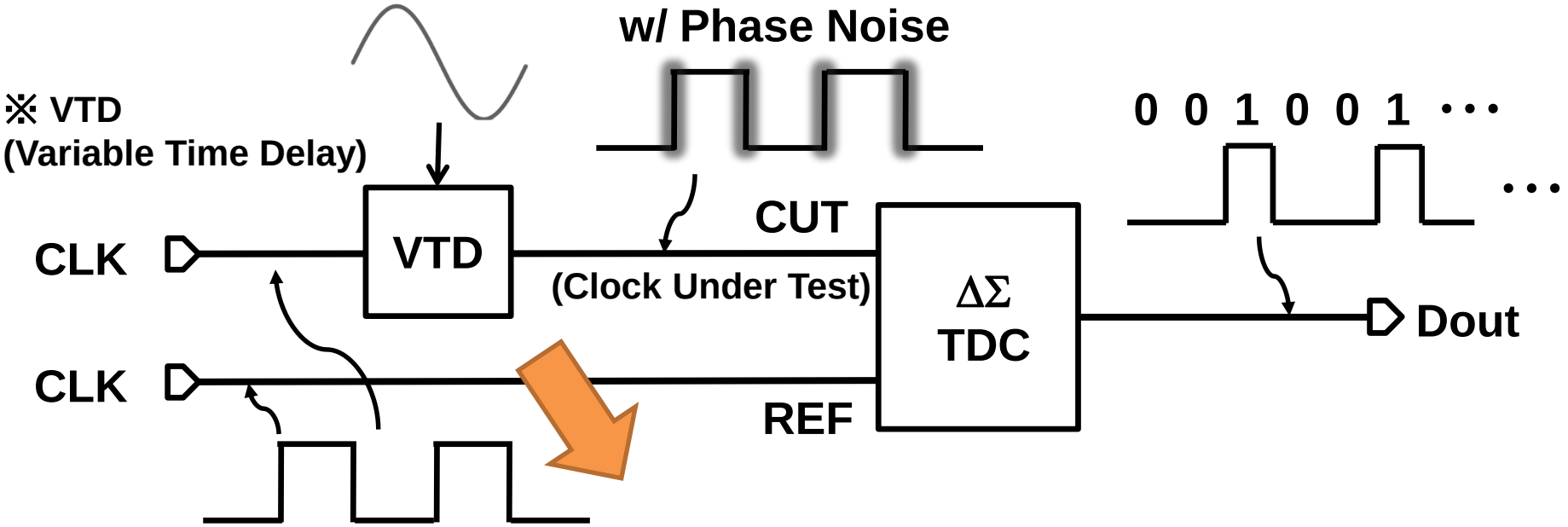
In case of sinusoidal phase fluctuation

$$\tau(m) = T \cdot \alpha_j \cdot \sin\left(\omega_j mT\right) \qquad 0 \le \alpha_j \le 1$$

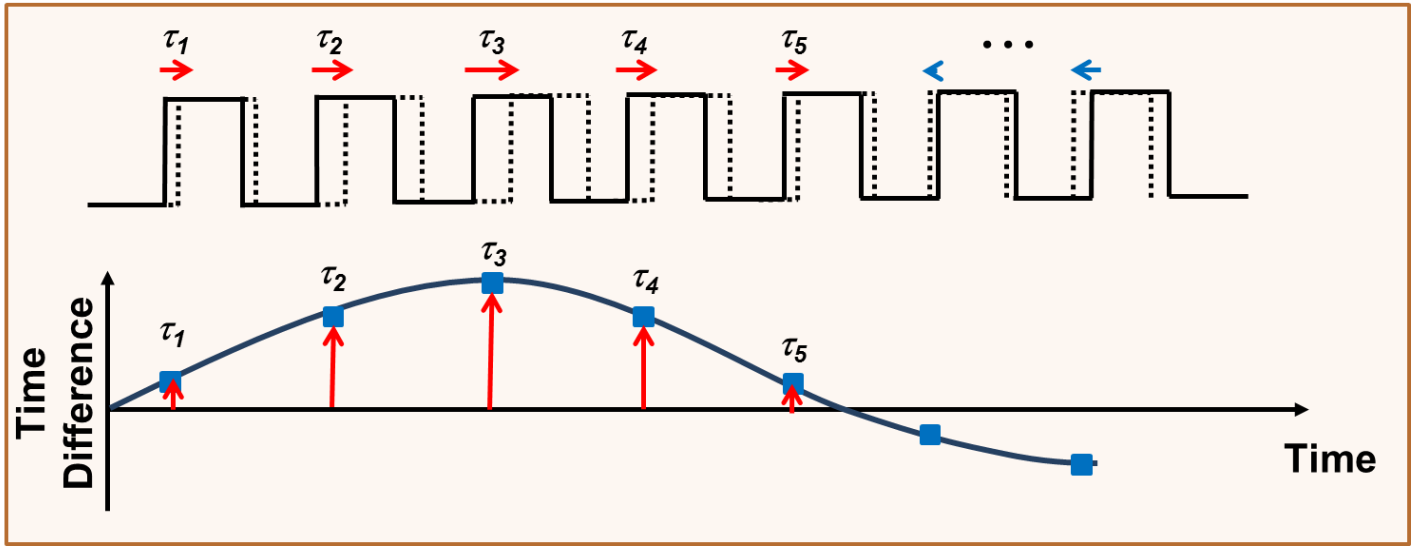
$$\phi(mT) = -2\pi\alpha_1 \cdot \sin(\omega_1 mT)$$: phase noise (time domain)

$$\Phi(\omega_1) = \frac{1}{2}(2\pi\alpha_1)^2$$: phase noise (freq. domain)

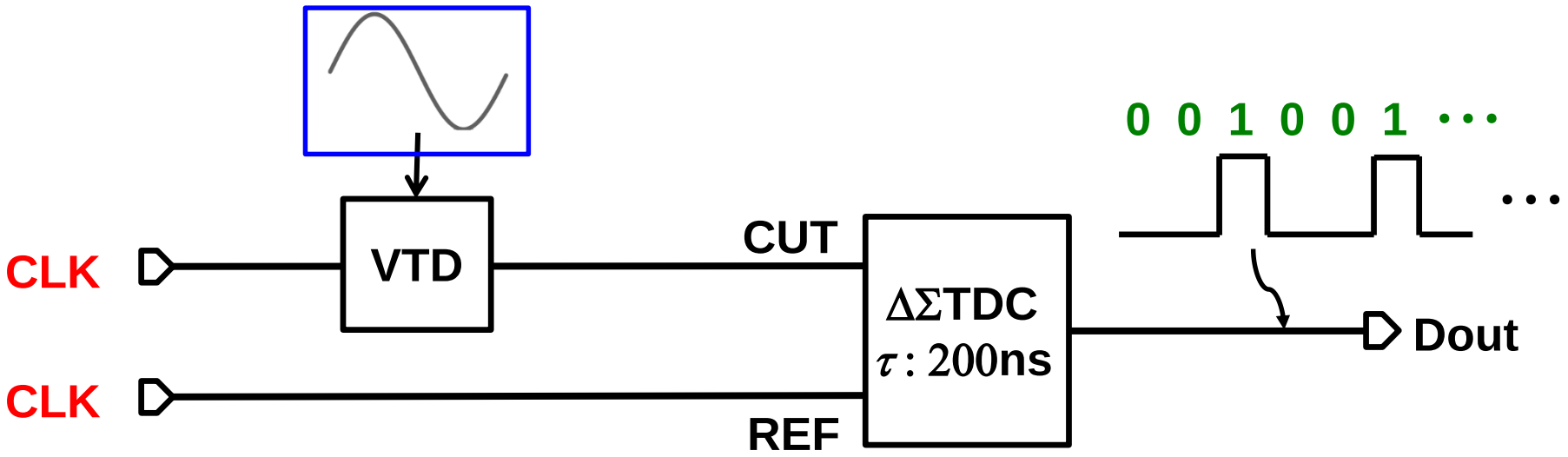
MATLAB Simulation



w/o Phase Noise



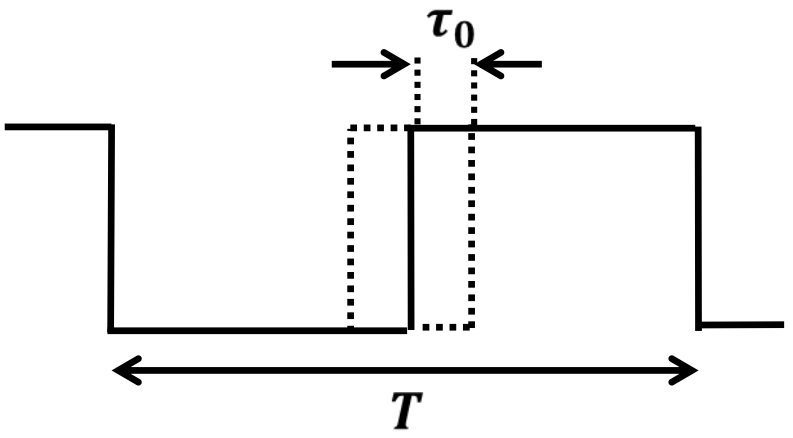
Simulation Conditions



- **CLK**:
  Input freq. = 1 MHz (T = 1 μs)

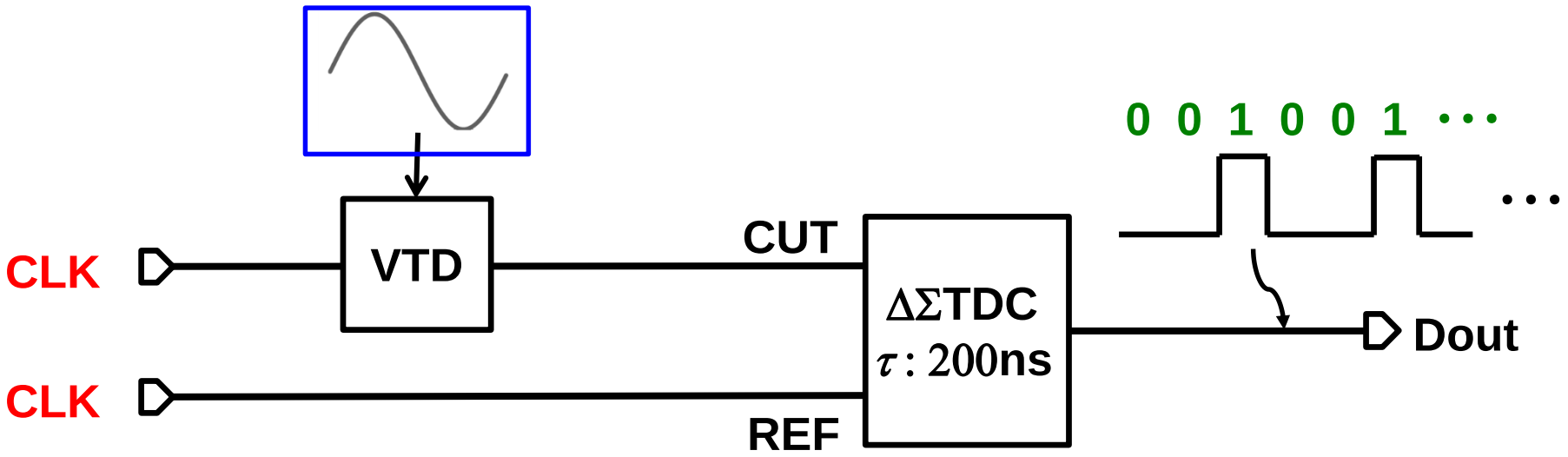
Phase variation（sinusoidal）

- Phase noise frequency :
  f_j ⇨ varied
- Jitter variation :
  $-0.1\mu s \leq \tau_0 \leq 0.1\mu s \left(= \frac{T}{10}\right)$



- **Number of data**:
  4096

Simulation Conditions



- **CLK**:
  Input freq. = 1 MHz (T = 1 μs)

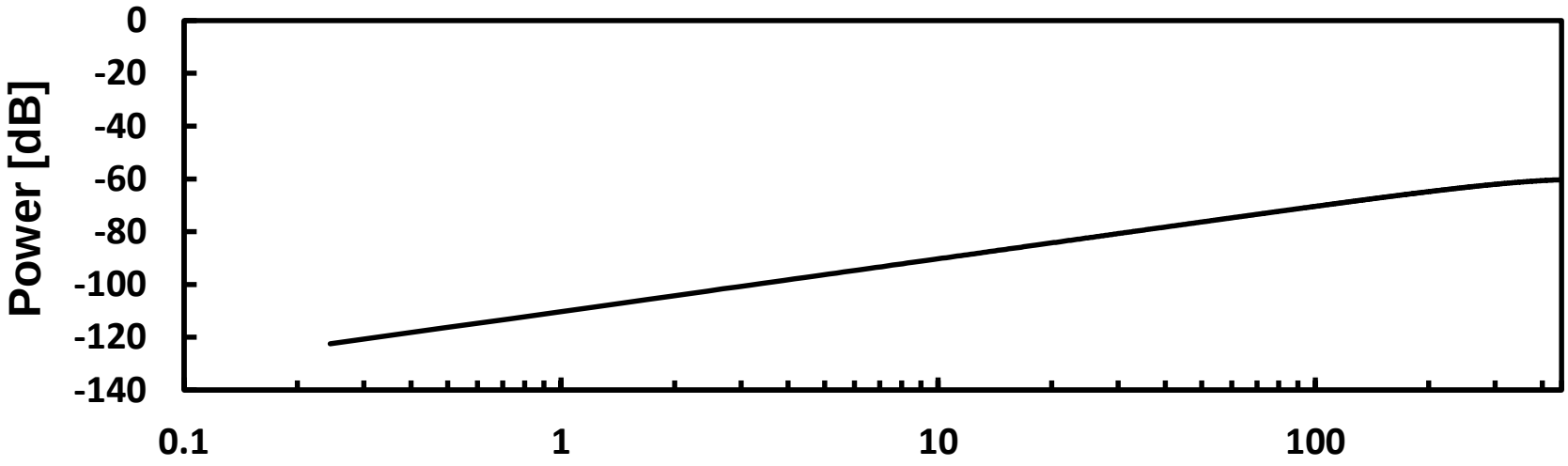
Phase variation (sinusoidal)

- Phase noise frequency :
  f_i = varied
- Jitter variation :
  $-0.1\mu s \leq \tau_0 \leq 0.1\mu s \left(= \frac{T}{10}\right)$
- **Number of data**:
  4096

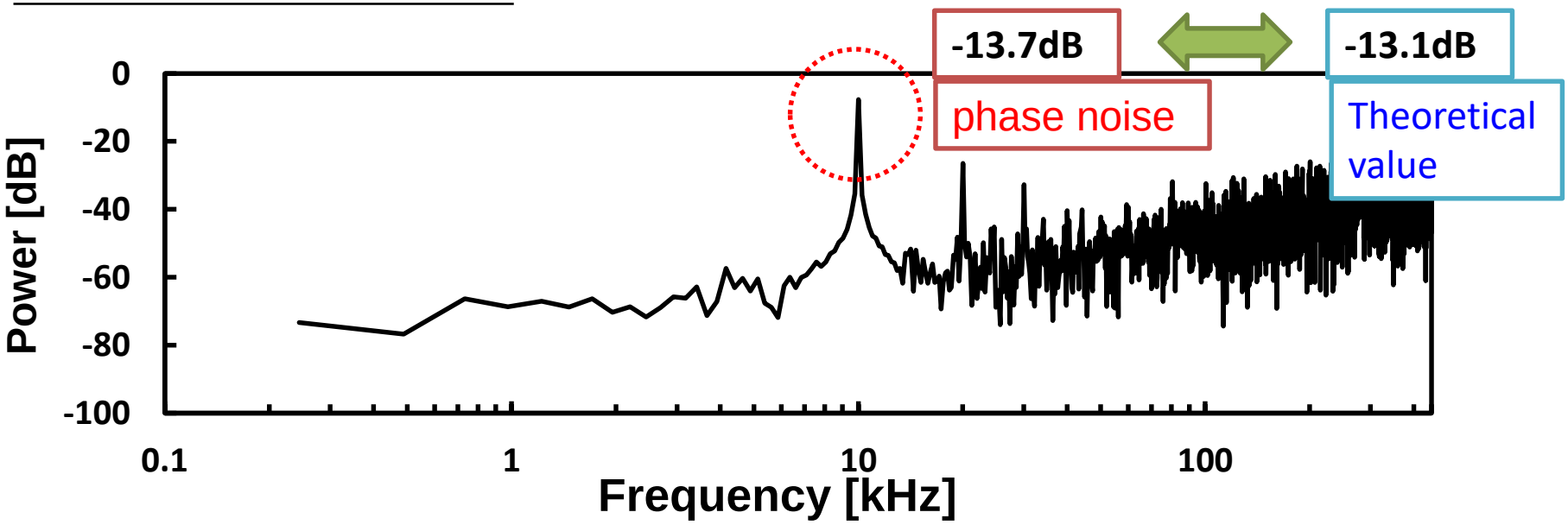
- Single sine wave
  ① $f_1 = 10$ kHz
  ② $f_1 = 50$ kHz
- Multiple sine waves
  ③ $f_1 = 10$ kHz
  $f_2 = 50$ kHz

Simulation Results ①

W/O Phase Noise

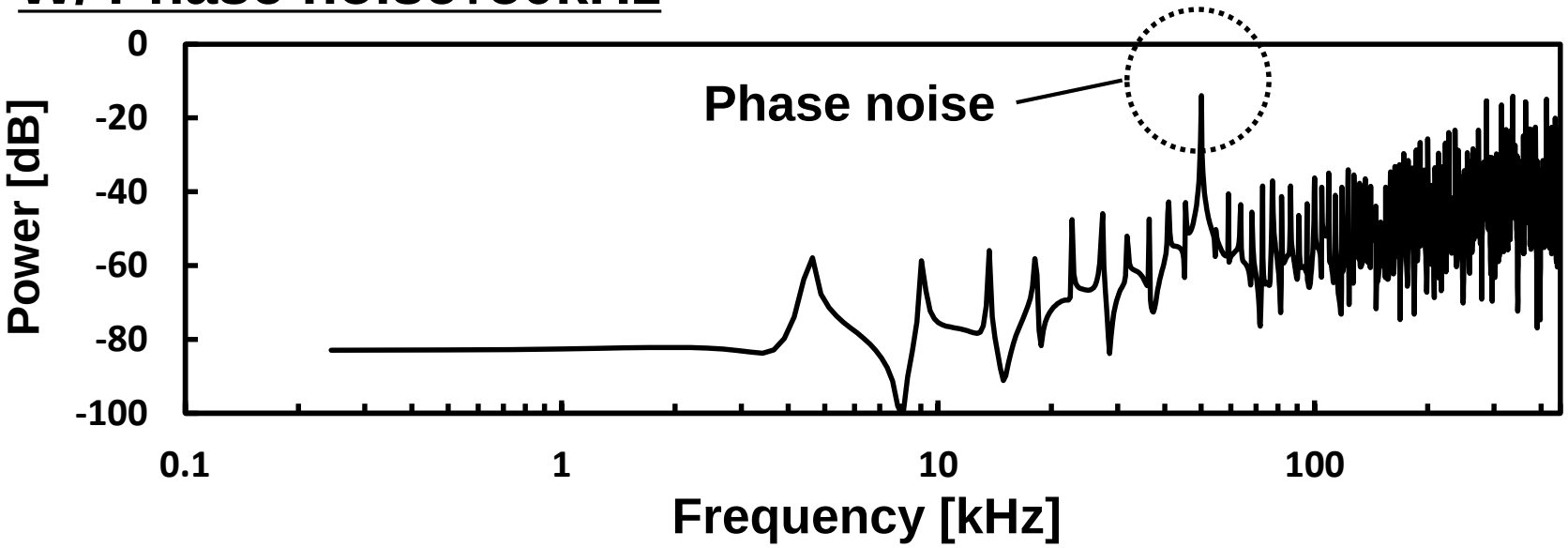


W/ Phase Noise：10kHz



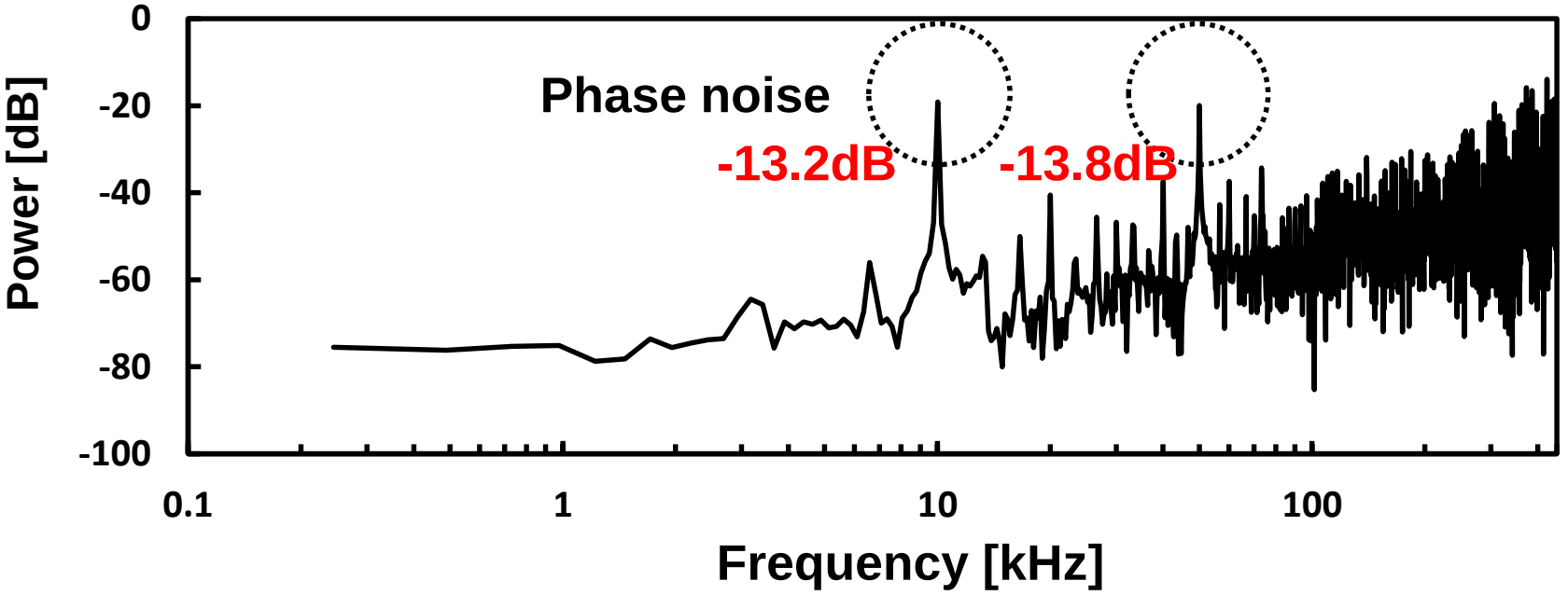
Simulation Results ②

W/ Phase noise：50kHz



Simulation Results ③

Phase noise：10kHz & 50kHz



Theoretical value

Power = -13.1[dB]

Outline

- Research Background & Objective
- Delta-Sigma TDC
- Phase Noise Measurement using ΔΣTDC with Reference Clock
- Phase Noise Measurement using ΔΣTDC without Reference Clock
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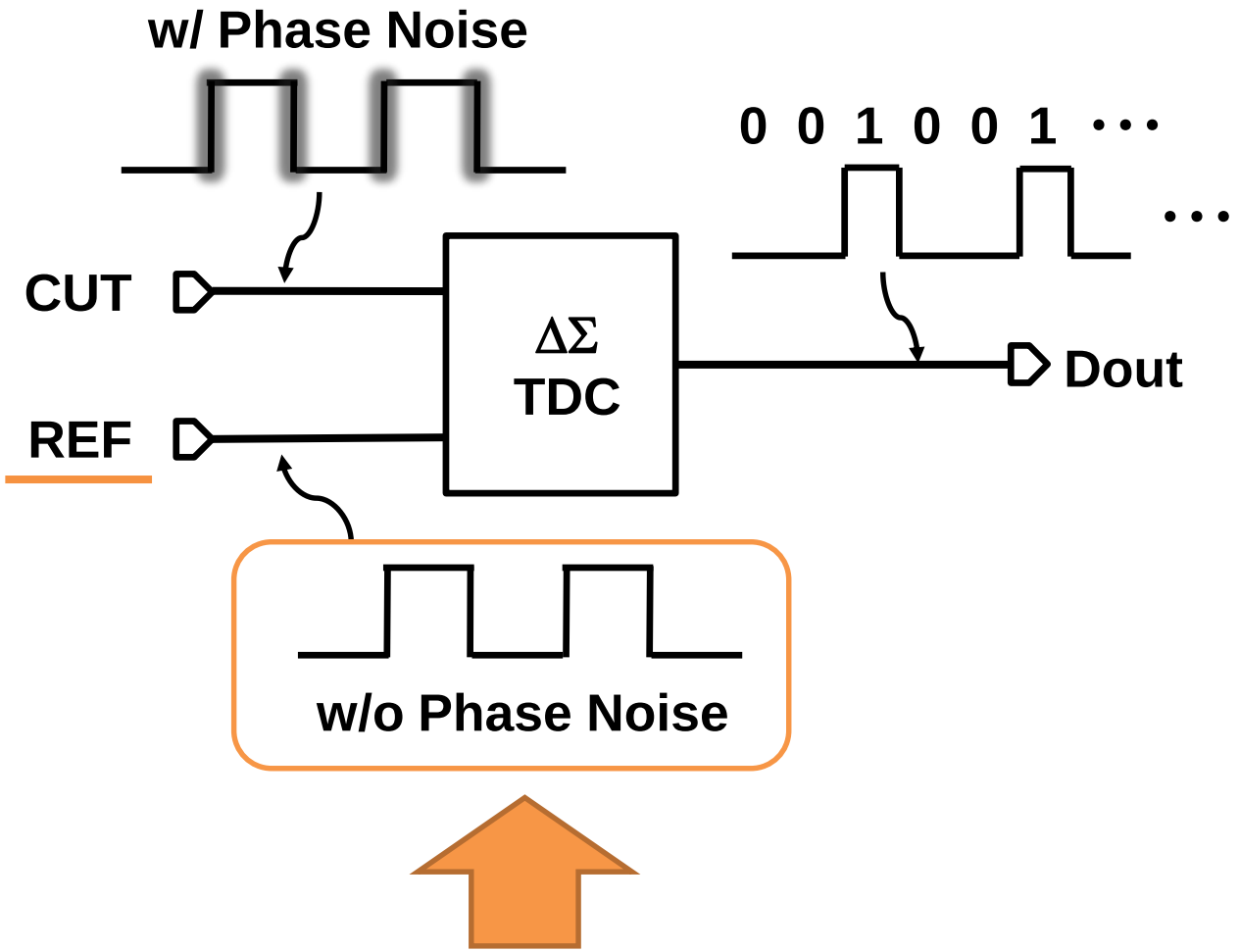
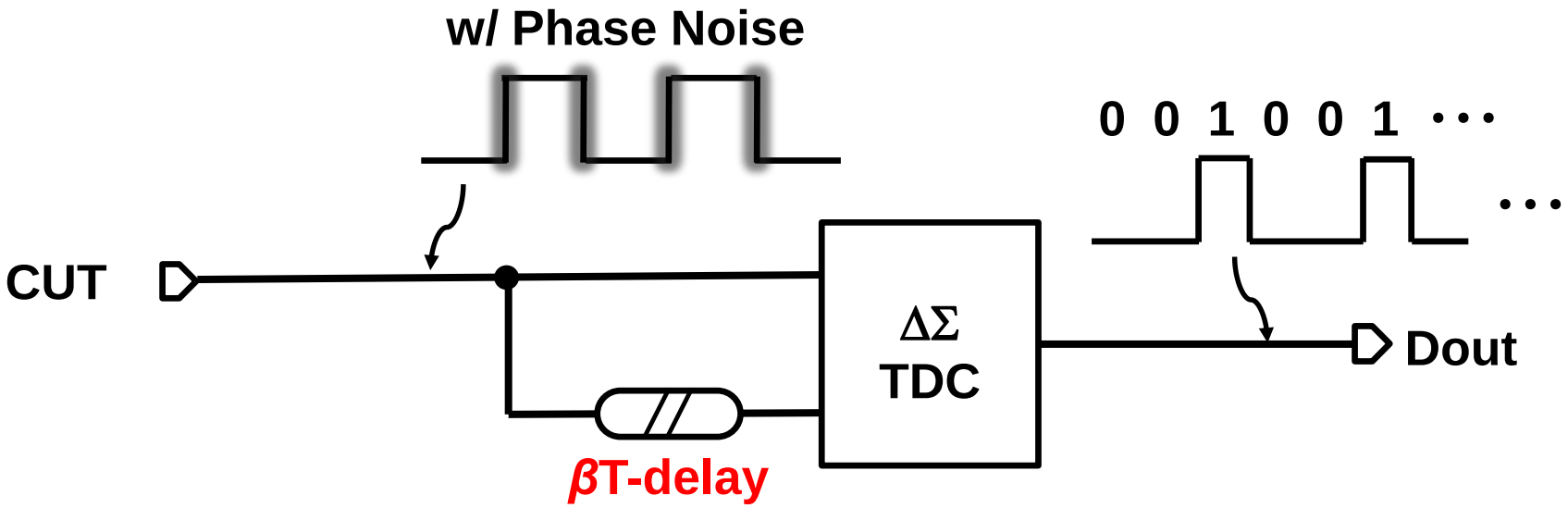
Problem of Proposed Method I



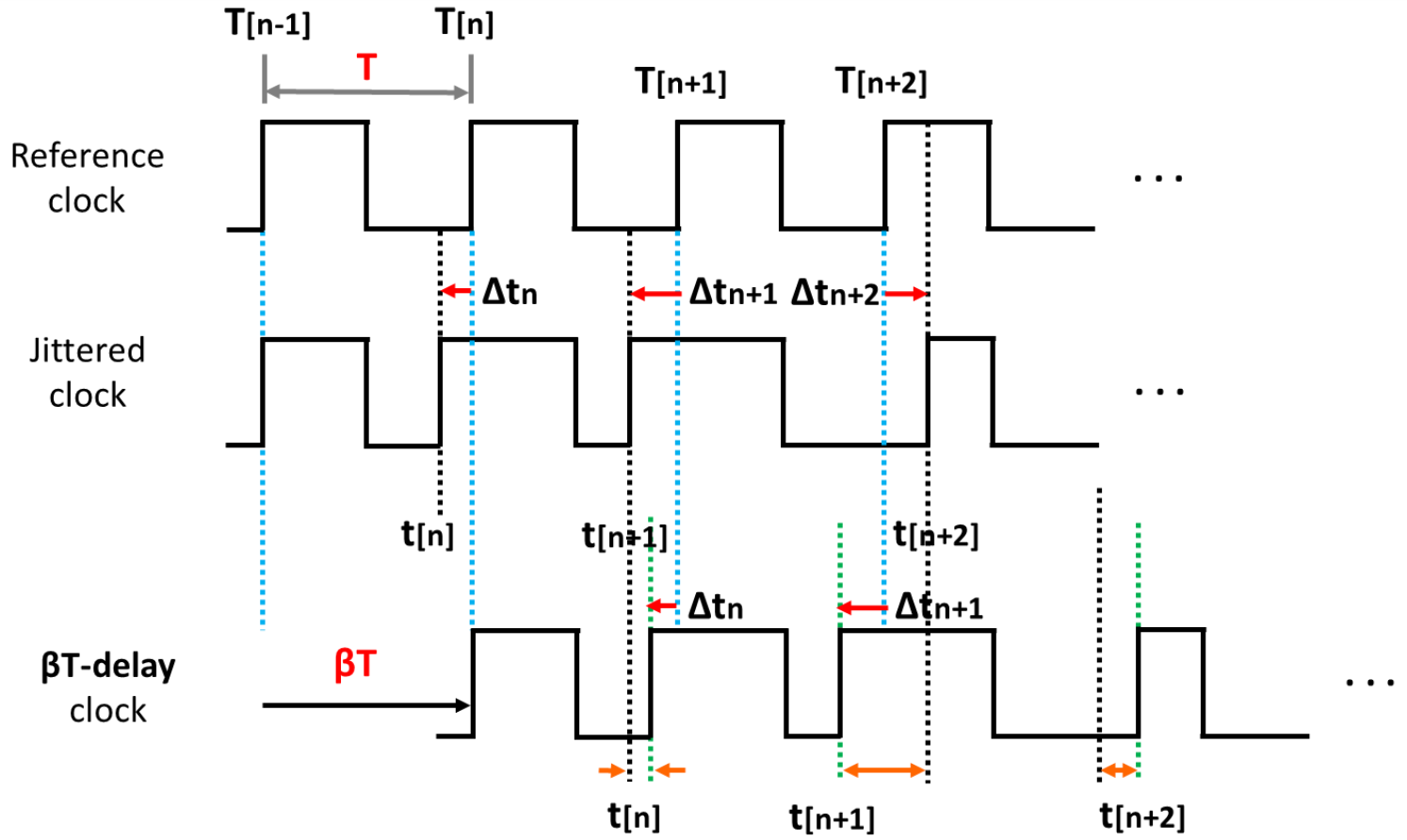
Difficult to implement

Self-Referenced Phase Noise Measurement Method



- No need for jitterless reference clock
- βT-delay: β is not required to be an integer.

Proposed Methods Ⅰ & Ⅱ



Method Ⅰ

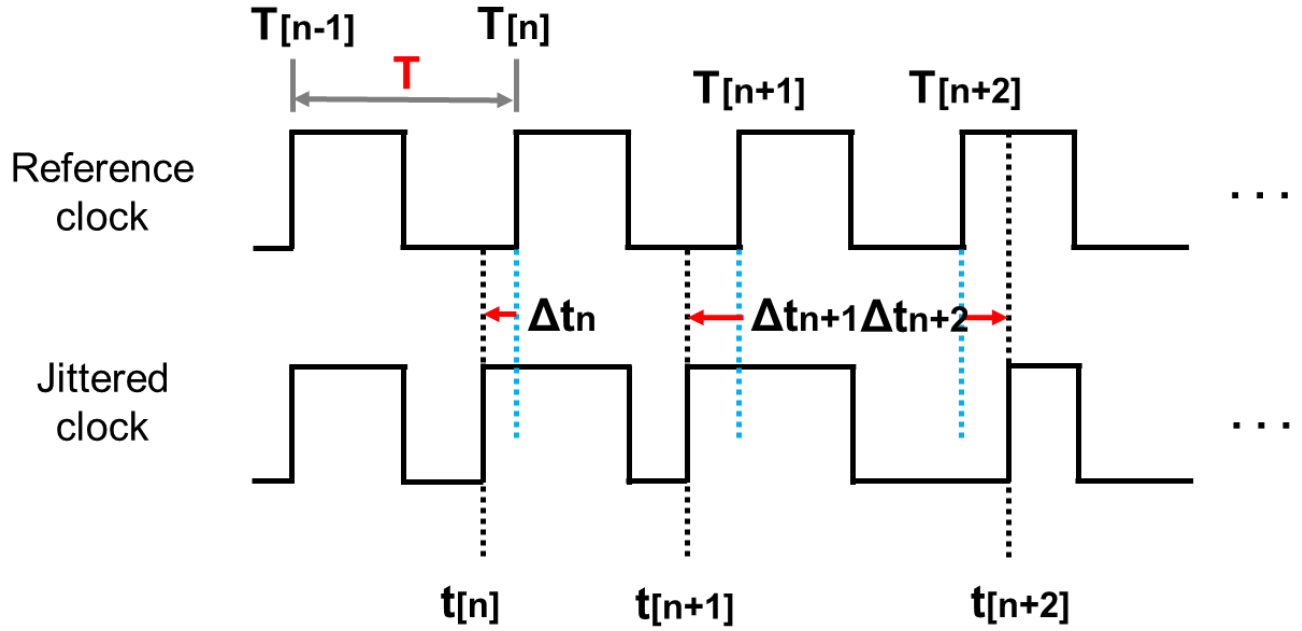
Method Ⅱ

Timing jitter measurement ⇨ Period jitter measurement

$$J_{PER}(n) = [\Delta t(n) - \Delta t(n-1)] - T_0$$

$$\therefore J_{PER}(n) = J(n) - J(n-1)$$

Mathematical Analysis



$\phi(mT) = -2\pi f_{in}\tau(m)$: **phase noise (time domain)**

① $\tau(m) = T \cdot \alpha_j \cdot \sin(\omega_j mT)$ In case of sinusoidal phase variation $0 \le \alpha_j \le 1$

Measurement of each period

$$\tau(m+1) - \tau(m) + (\beta - 1)\mathrm{T}$$
$$= T \cdot \alpha_1[sin(\omega_1 (m+1)T) - sin(\omega_1 \cdot mT)] + (\beta - 1)\mathrm{T}$$
$$= 2T \cdot \alpha_1 sin(\omega_1 T/2) cos(\omega_1 (m+1/2)T) + (\beta - 1)\mathrm{T}$$

Mathematical Analysis

① $\tau(m) = T \cdot \alpha_j \cdot \sin(\omega_j m T)$ In case of sinusoidal phase variation $0 \le \alpha_j \le 1$

phase noise (time domain)

$$\therefore \phi'(mT) = 2T \cdot \alpha_1 \, sin(\omega_1 T/2) \, cos(\omega_1 (m + 1/2)T)$$

phase noise (frequency domain)

$$\therefore \Phi'(\omega_1) = \frac{1}{2}(2\pi\alpha_1)^2 \, [2 \sin 2(\omega_1 T/2)]^2$$

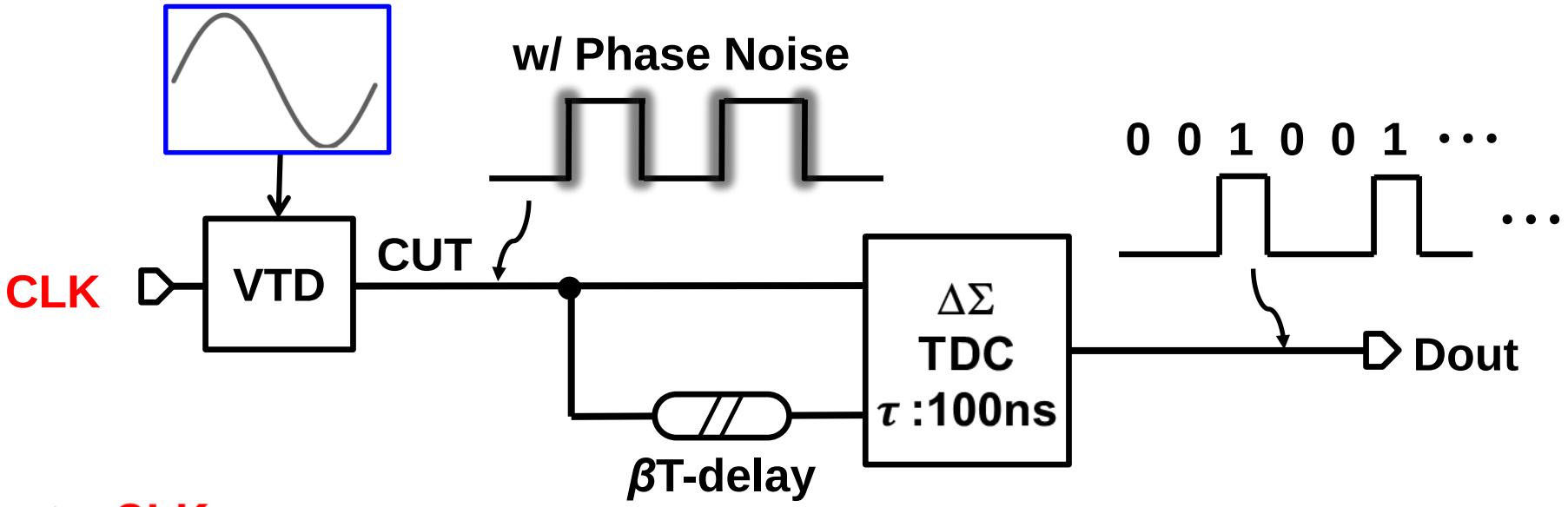
$$\cong \frac{1}{2}(2\pi\alpha_1)^2 \omega_1{}^2 T^2 \qquad (\because \omega_1 T/2 \ll 1)$$

ω1: phase noise freq. [low freq.]
T : input CLK period (=1/f)

phase noise power at ω1

$$\Phi(\omega_1) = \frac{1}{2}(2\pi\alpha_1)^2$$

Simulation Conditions



- **CLK**:
  Input freq. = 1 MHz (T = 1 μs)

Phase variation (sinusoidal)

- Phase noise frequency :
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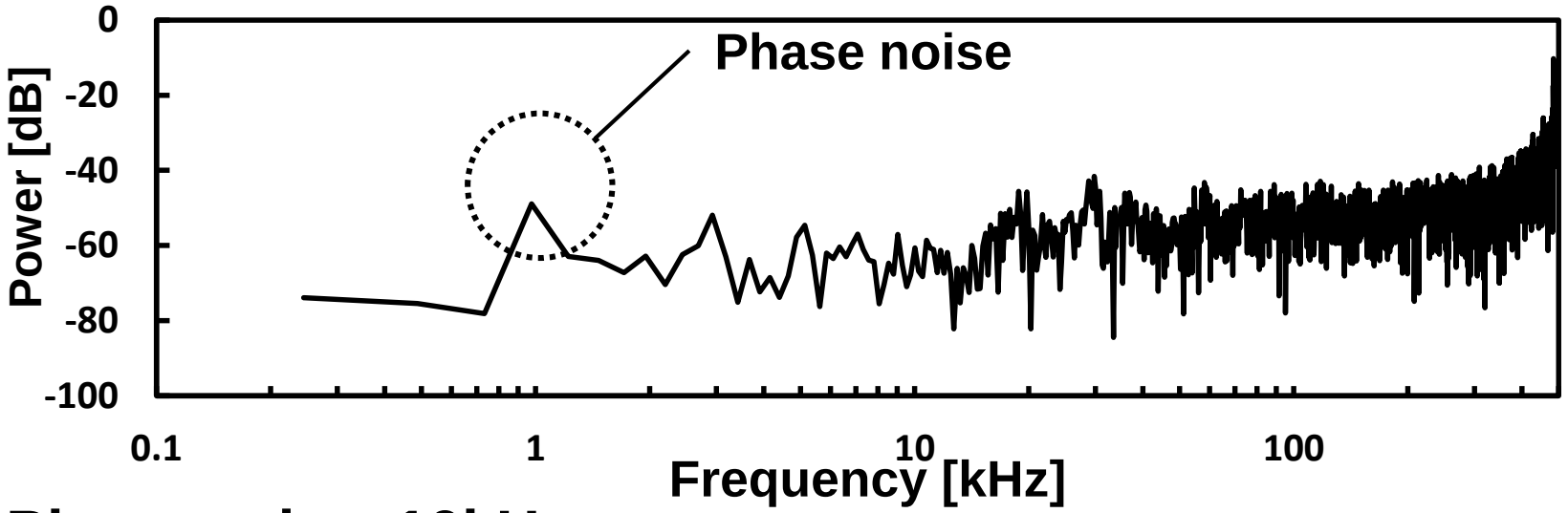
- Jitter variation :
  $-0.1\mu s \leq \tau_0 \leq 0.1\mu s \left(= \frac{T}{10}\right)$
- **Number of data**:
  4096

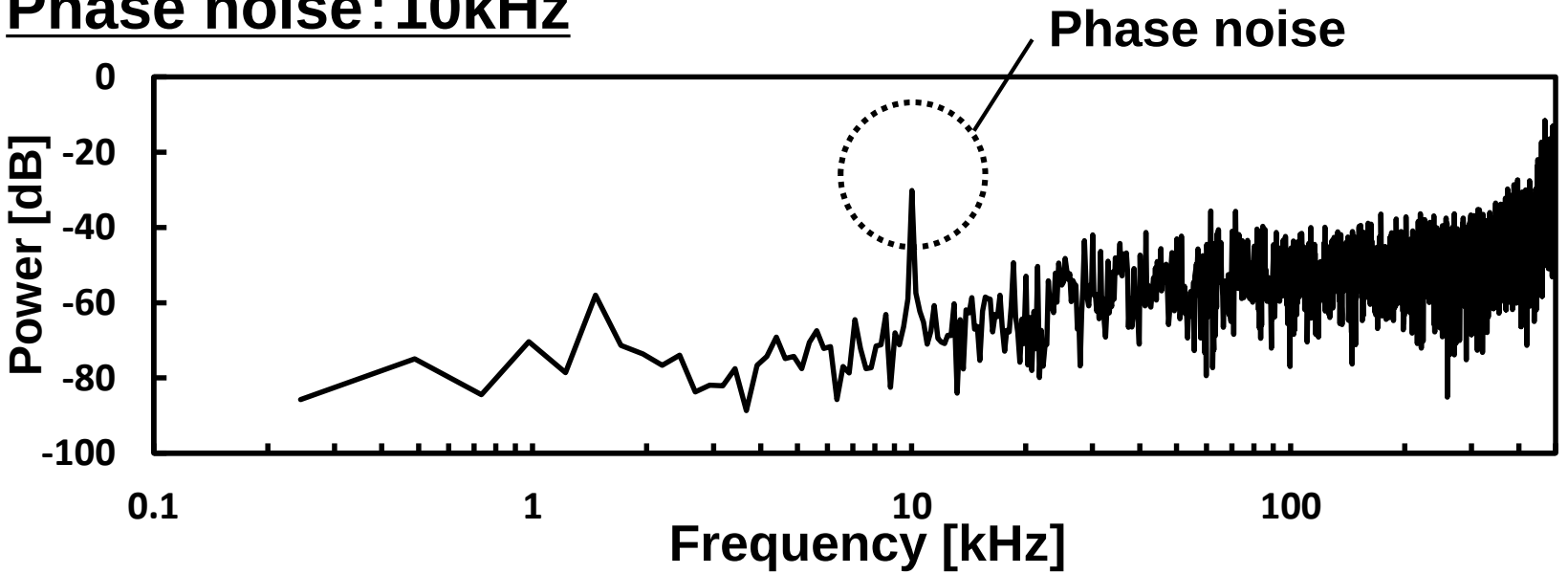
- Single sinusoidal
  ① $f_1 = 1$ kHz
  ② $f_1 = 10$ kHz
  ③ $f_1 = 100$ kHz
- Multiple sinusoidal
  ④ $f_1 = 10$ kHz
  $f_2 = 50$ kHz

Simulation Results ①&②

Phase noise：1kHz

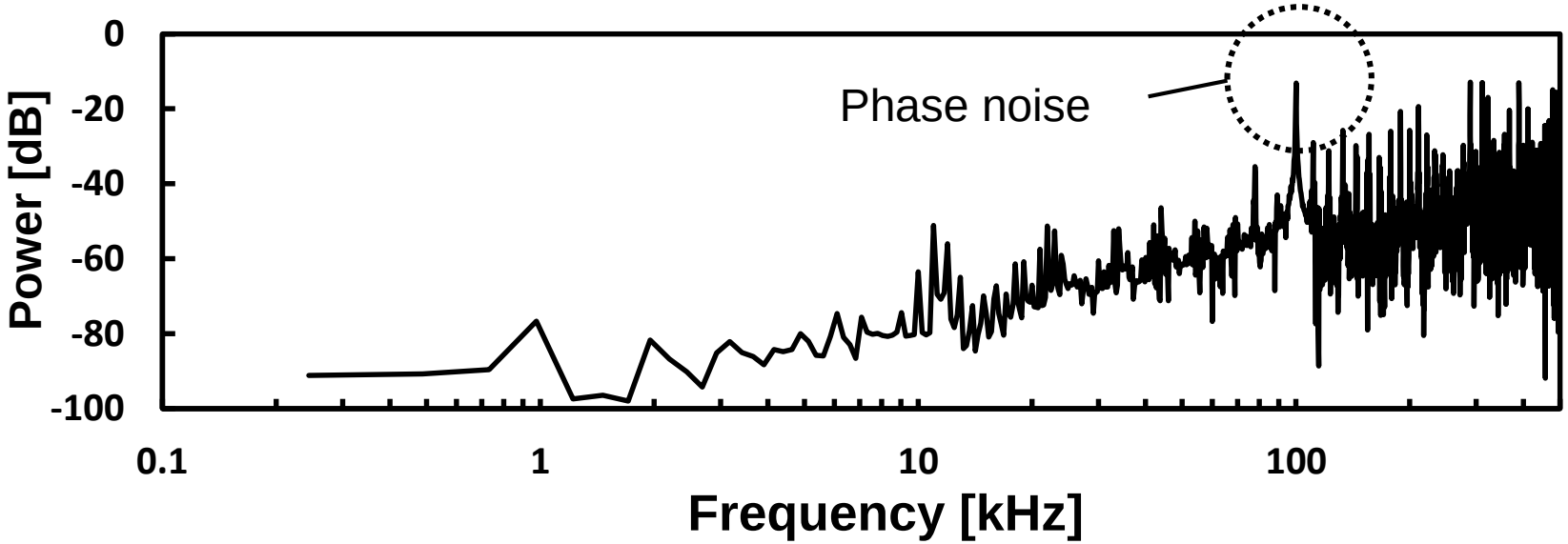


Phase noise：10kHz

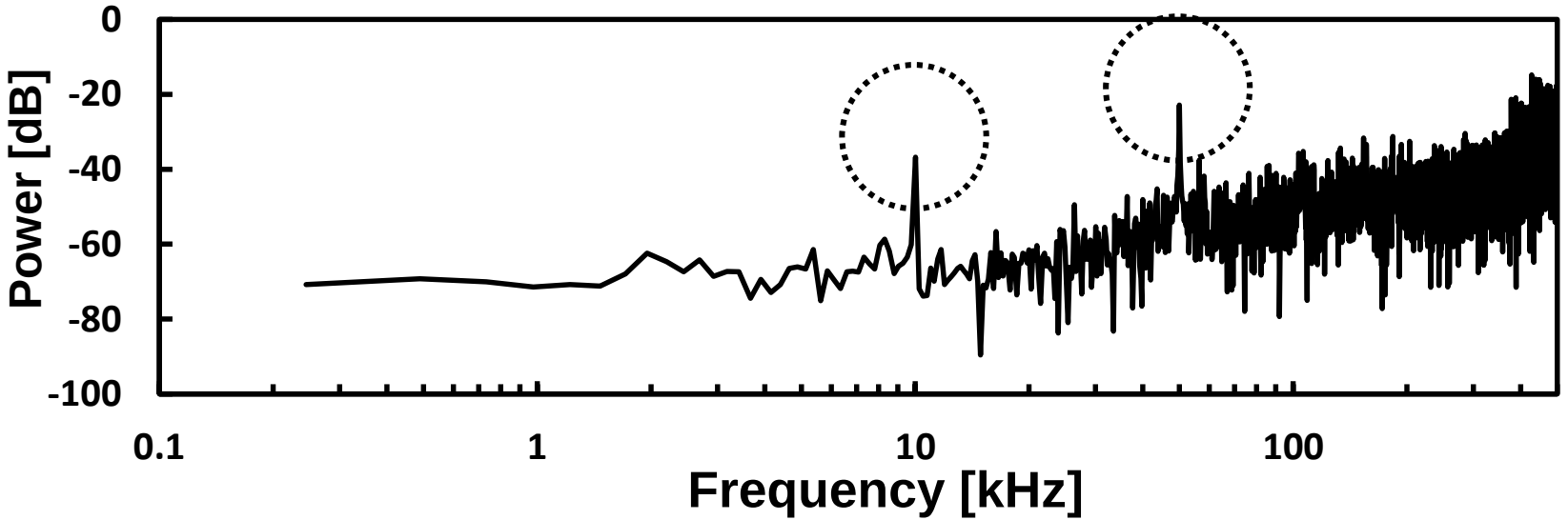


Simulation Results ③&④

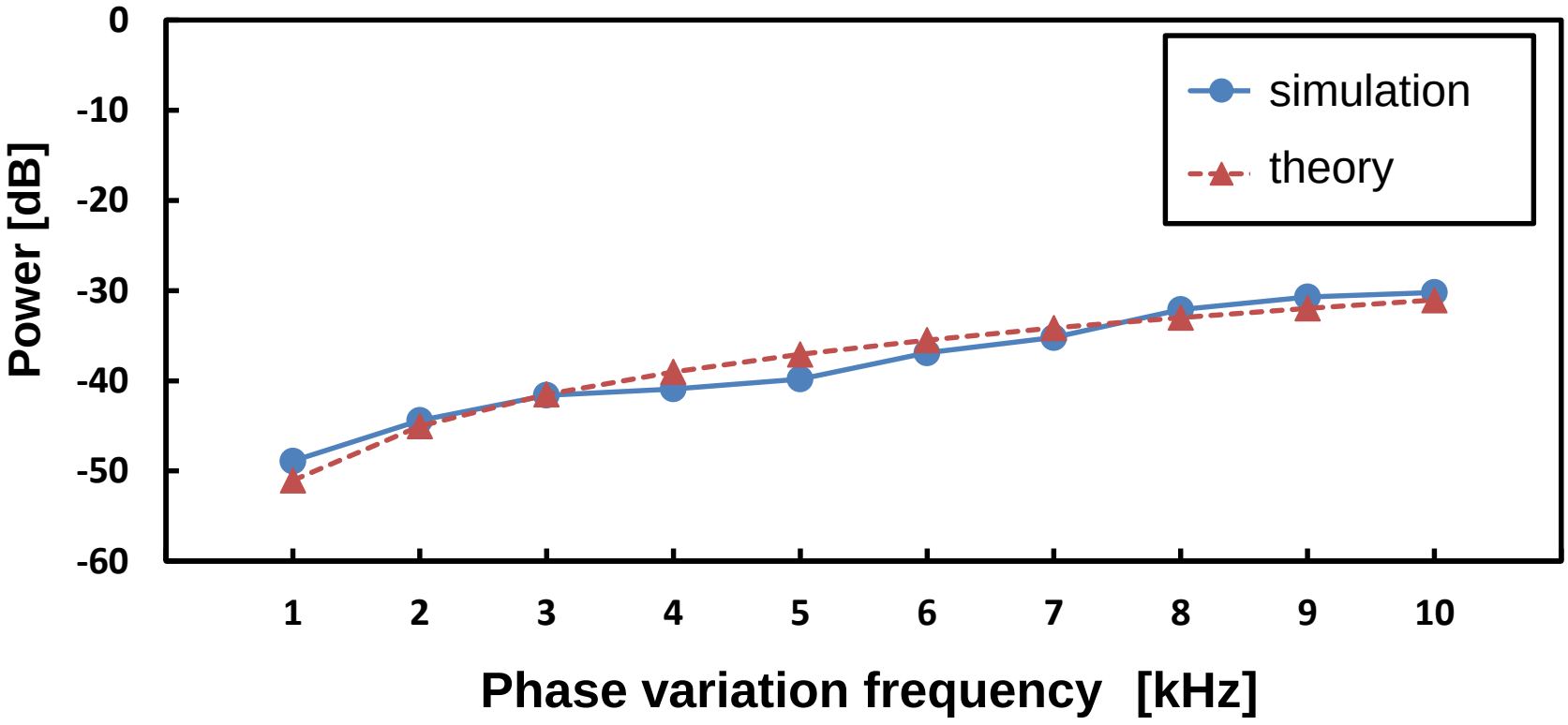
Phase noise：100kHz



Phase noise：10kHz＆50kHz

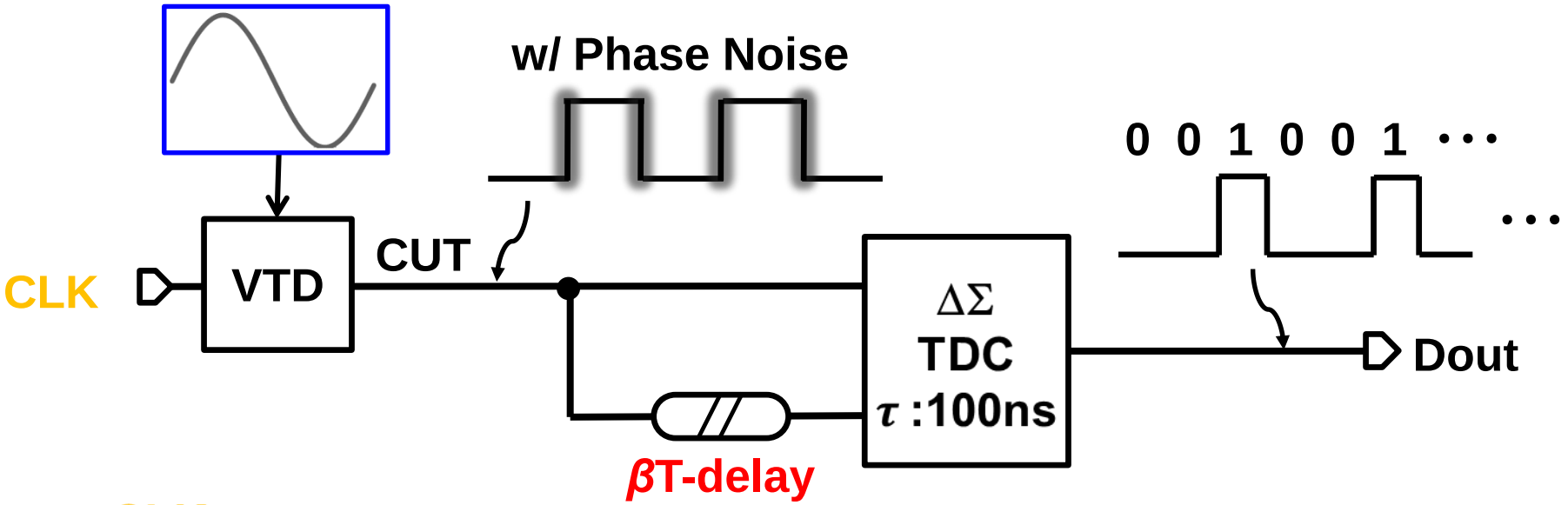


Comparison of Theory and Simulation Results



Theoretical expression $$\Phi'(\omega_1) = \frac{1}{2}(2\pi\alpha_1)^2\omega_1{}^2T^2$$

Simulation Conditiions



- **CLK**:
  Input freq. = 1 MHz (T = 1 μs)

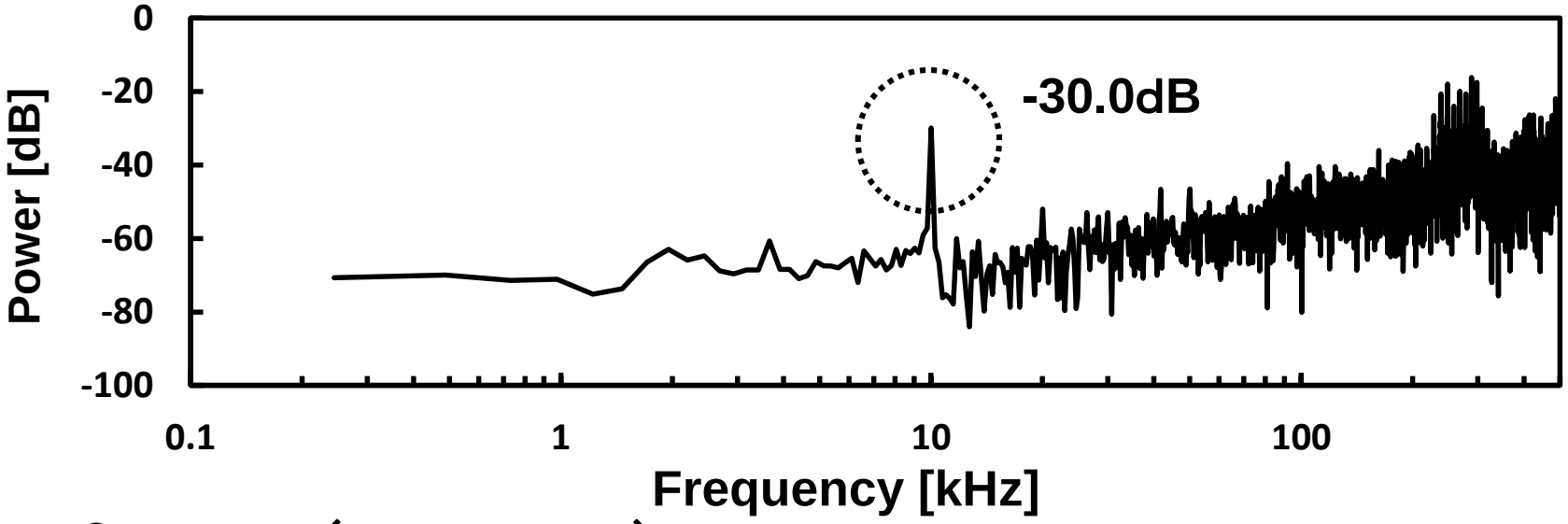
Phase variation（sinusoidal）

- Phase noise frequency :
  f_i = 10kHz
- Jitter variation :
  $-0.1\mu s \leq \tau_0 \leq 0.1\mu s \left(= \frac{T}{10}\right)$
- **Number of data**:
  4096

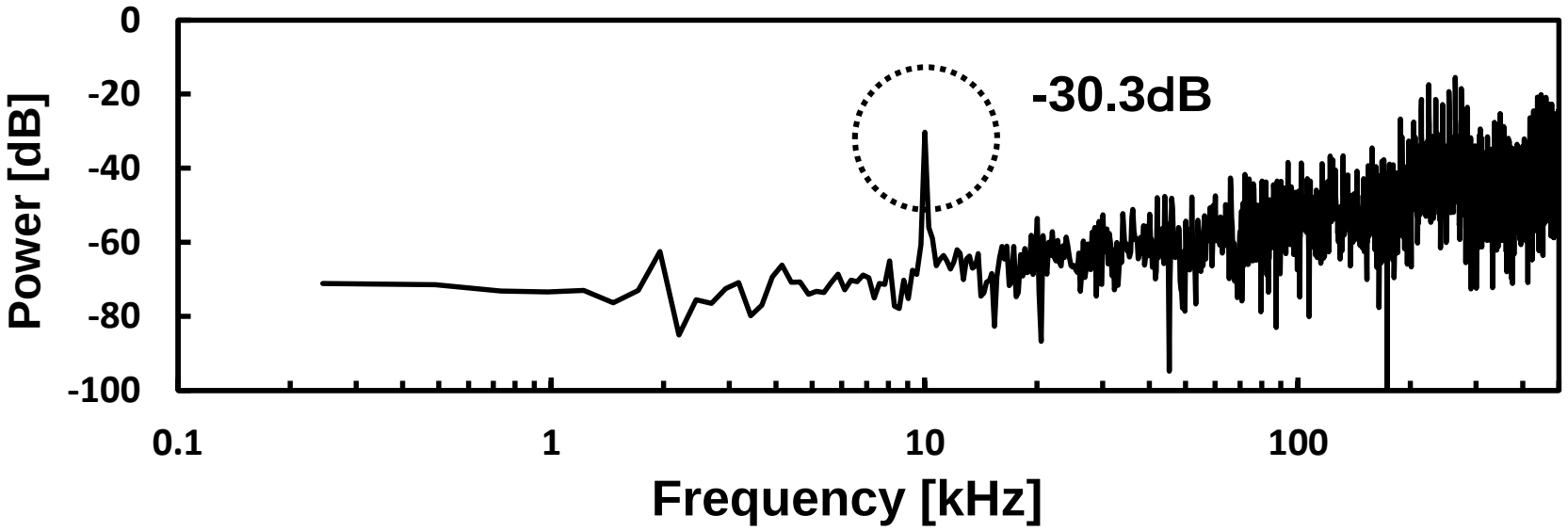
- β value deviation by ±5% from 1.0
  - β=0.95
  - β=1.05

Simulation Results（delay β variation）

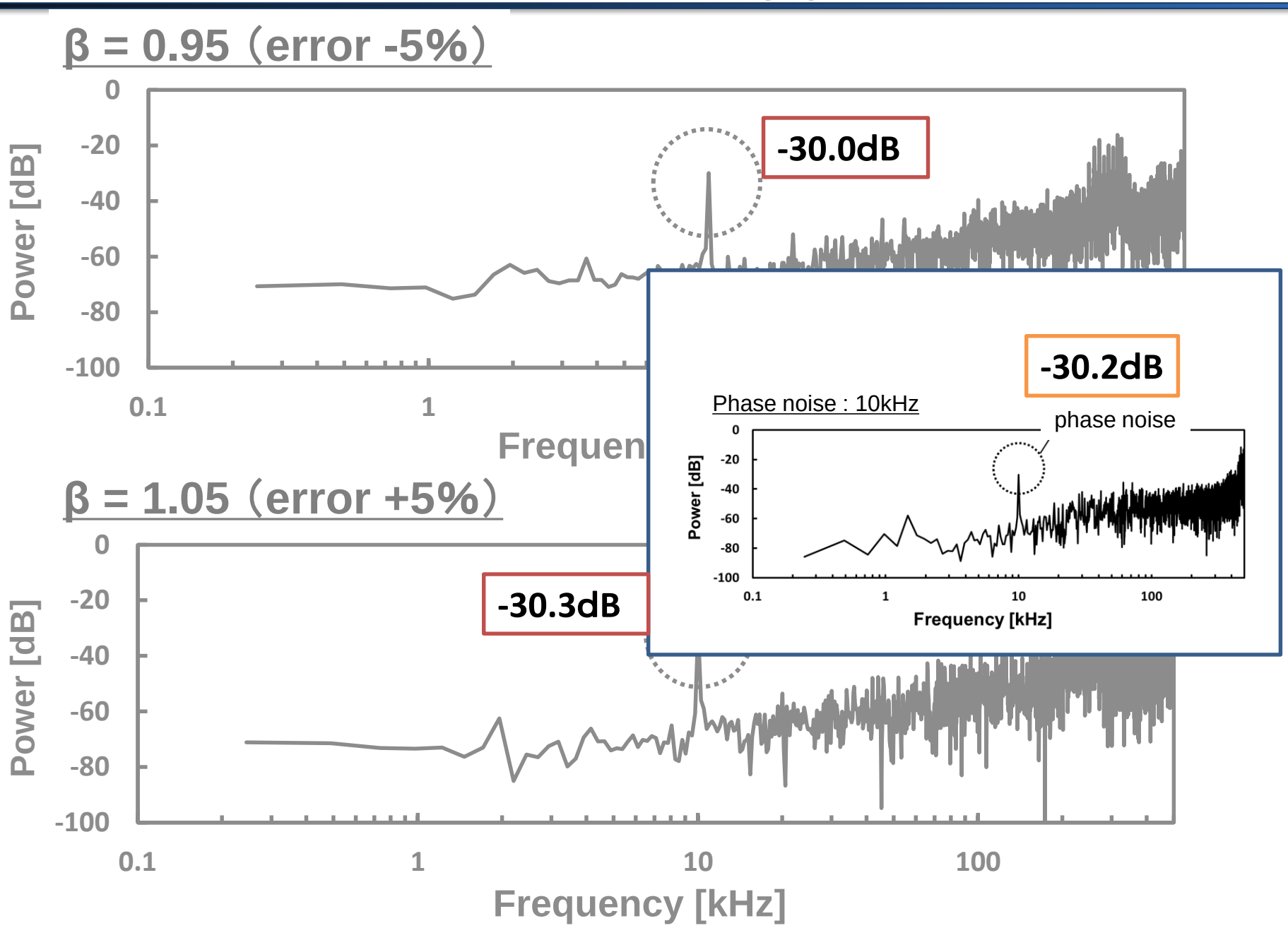
β = 0.95（error -5%）



β = 1.05（error +5%）



Simulation Results（delay β variation）



Outline

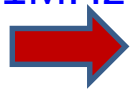
- Research Background & Objective
- Delta-Sigma TDC
- Phase Noise Measurement using ΔΣTDC with Reference Clock
- Phase Noise Measurement using ΔΣTDC without Reference Clock
  - Self-Referenced Clock Technique
- Conclusions

Conclusion

Proposal of two phase measurement techniques with ΔΣTDC

- Low cost testing without requiring spectrum analyzer
- On-chip high-precision phase noise measurement
- Fine time resolution measurement possible with ΔΣTDC
- Phase noise power spectrum obtained by FFT of TDC digital output

1MHz carrier (clock), 64K TDC output data



Phase noise power spectrum of 0 to 0.5MHz away from 1MHz with 15.2Hz resolution.

MATLAB simulation verification

- Verified by superimposing several sinusoidal phase variation components
- Compared theoretical analysis and simulation results
- Self-referenced clock method with several β delay coefficient values

Outline

- Research Background
- Integral-type TDC
  - Time Hold Circuit
  - Equivalent-Time Sampling
  - Integral TDC
  - Vernier Frequency TDC
- Delta-Sigma TDC
  for Phase Noise Measurement
- Conclusion

Conclusion

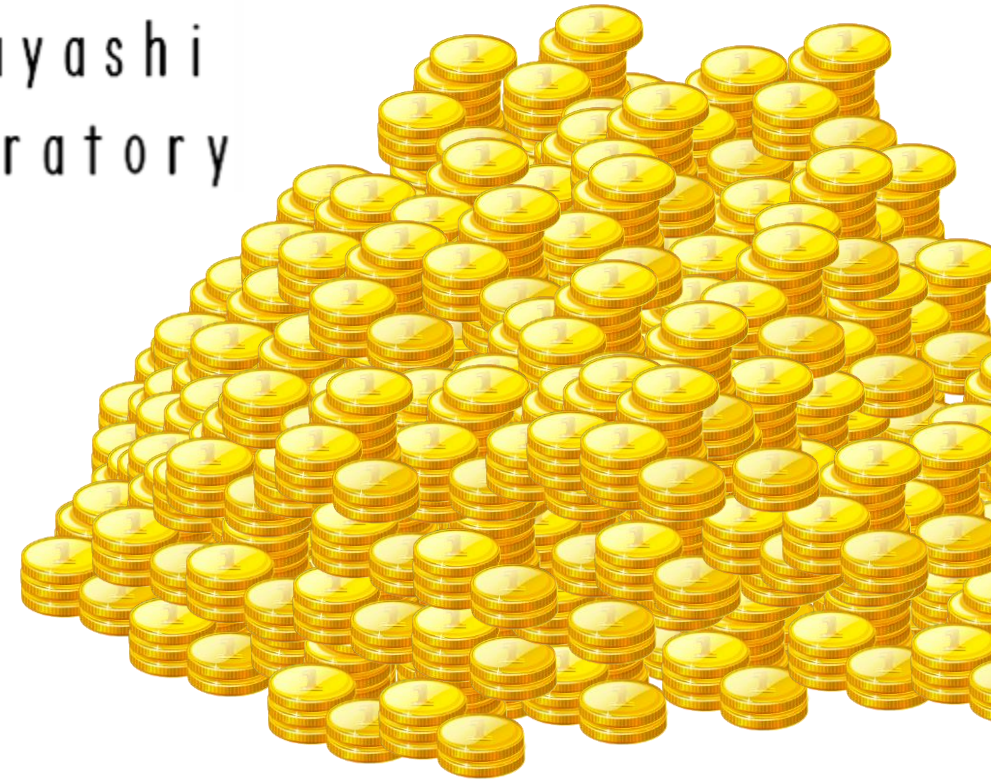
Time continues indefinitely

Dynamic range of time domain signal processing can be very wide.

Time is GOLD !!

一刻千金

Kobayashi Laboratory



TDC is the key.